

Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.063 @ $V_{GS} = -10$ V	-5.1
	0.110 @ $V_{GS} = -4.5$ V	-3.8

FEATURES

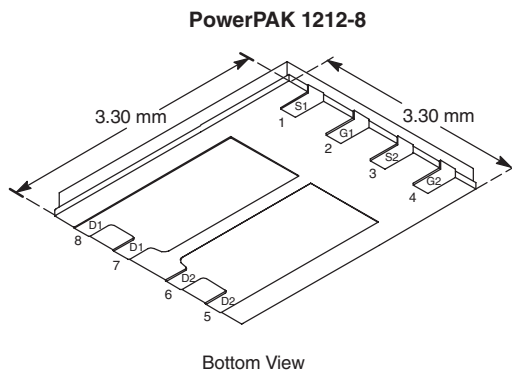
- TrenchFET[®] Power MOSFETS
- New Low Thermal Resistance PowerPAK[®] Package



RoHS*
COMPLIANT

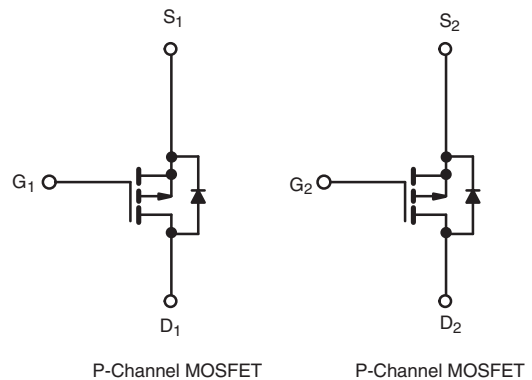
APPLICATIONS

- Portable
 - Battery Switch
 - Load Switch



Bottom View

Ordering Information: Si7921DN-T1
Si7921DN-T1-E3 (Lead (Pb)-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	-30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-5.1	-3.7
		$T_A = 85^\circ\text{C}$	-3.7	-2.7
Pulsed Drain Current	I_{DM}	-20		A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	-1.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5	1.3
		$T_A = 85^\circ\text{C}$	1.3	0.85
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b,c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	40	50
		Steady State	75	94
Maximum Junction-to-Case	R_{thJC}	5.6	7	$^\circ\text{C}/\text{W}$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply



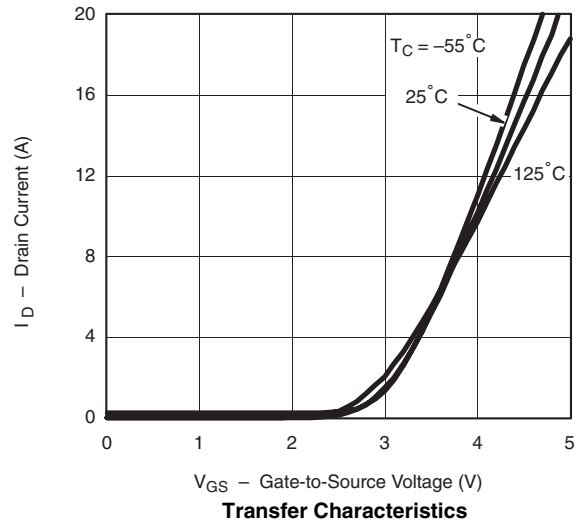
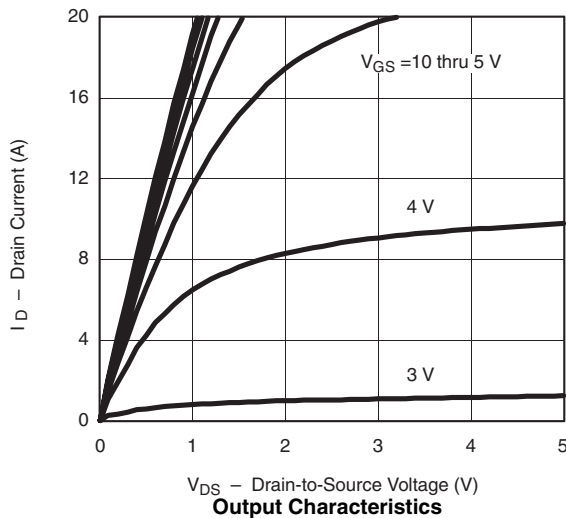
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1.0		-3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -5.1 \text{ A}$		0.050	0.063	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -3.8 \text{ A}$		0.085	0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -5.1 \text{ A}$		9		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5.1 \text{ A}$		10.5	16	nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			2.8		
Gate Resistance	R_g			8.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$		10	15	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			20	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		25	50	

Notes

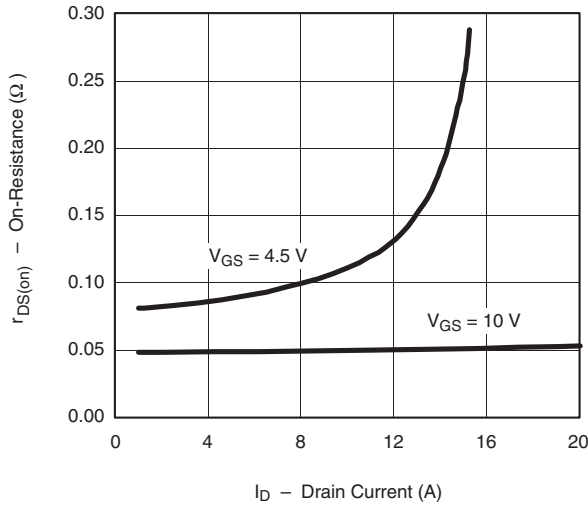
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

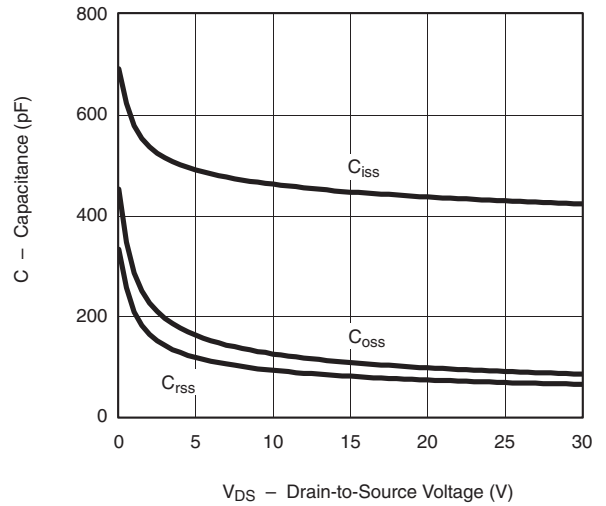
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



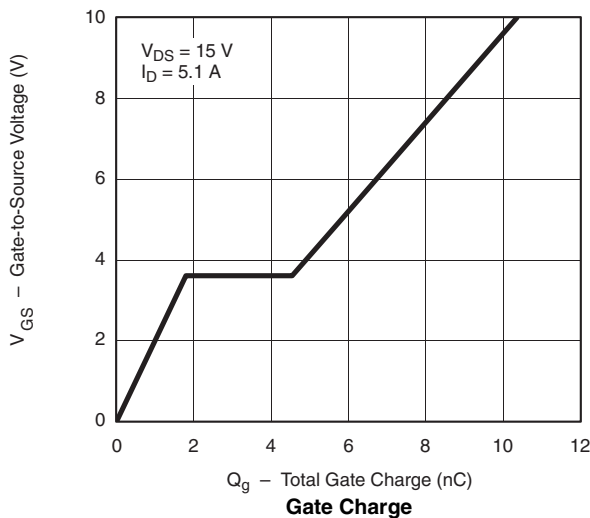
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



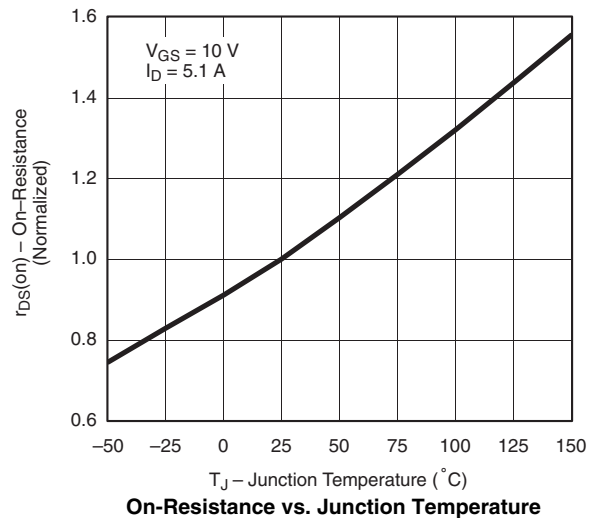
On-Resistance vs. Drain Current



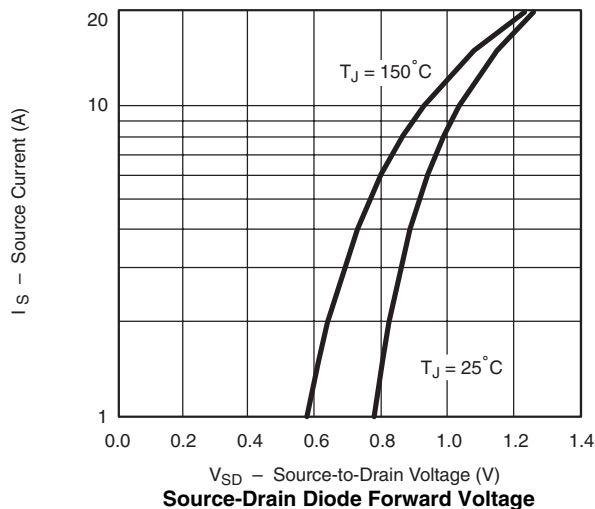
Capacitance



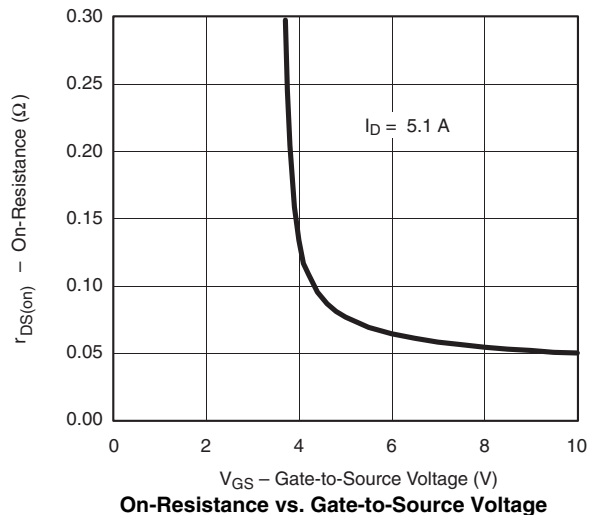
Gate Charge



On-Resistance vs. Junction Temperature



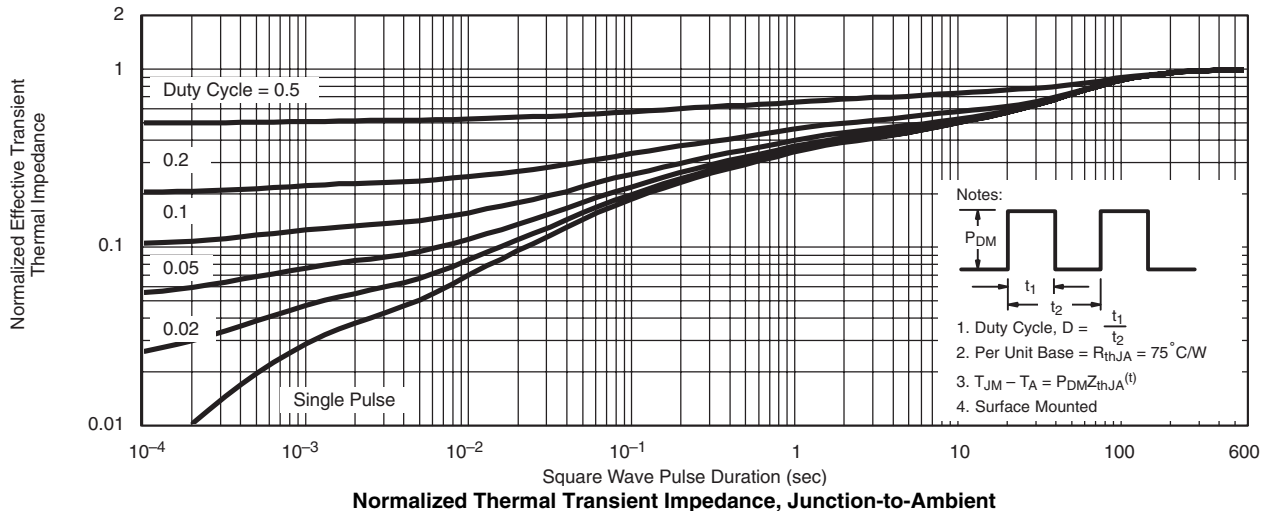
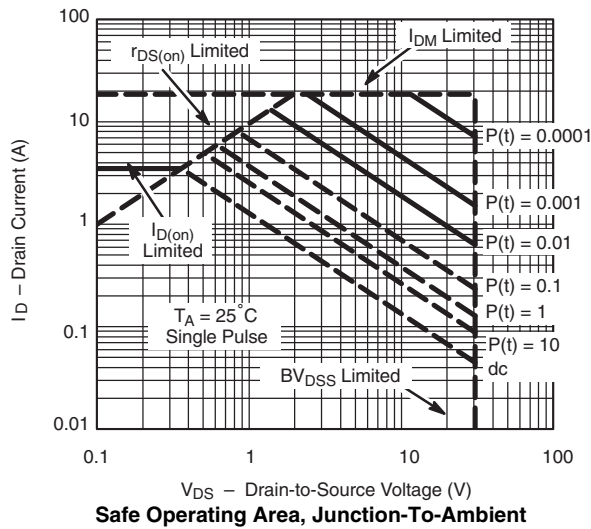
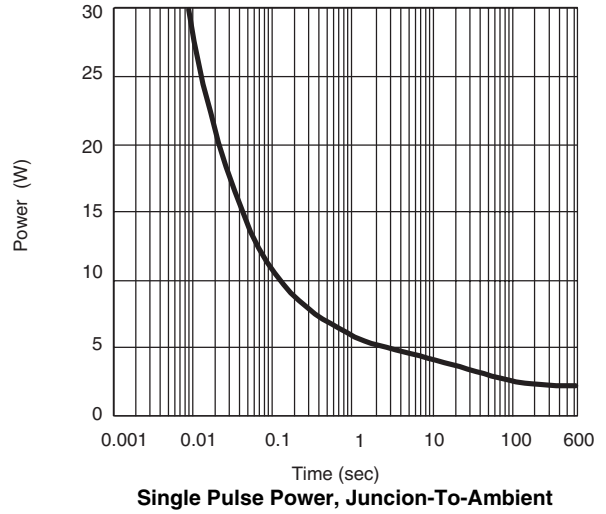
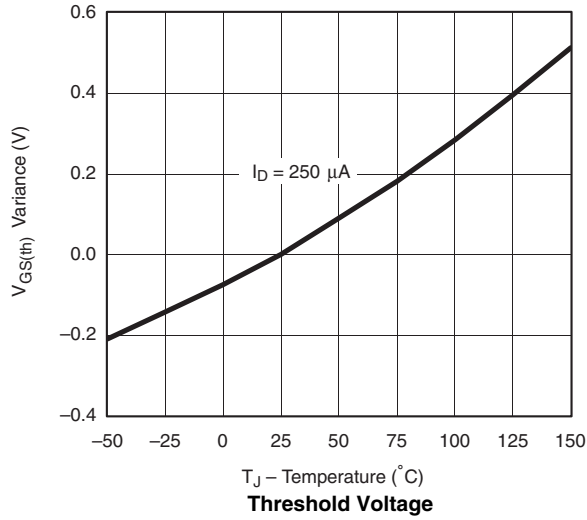
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

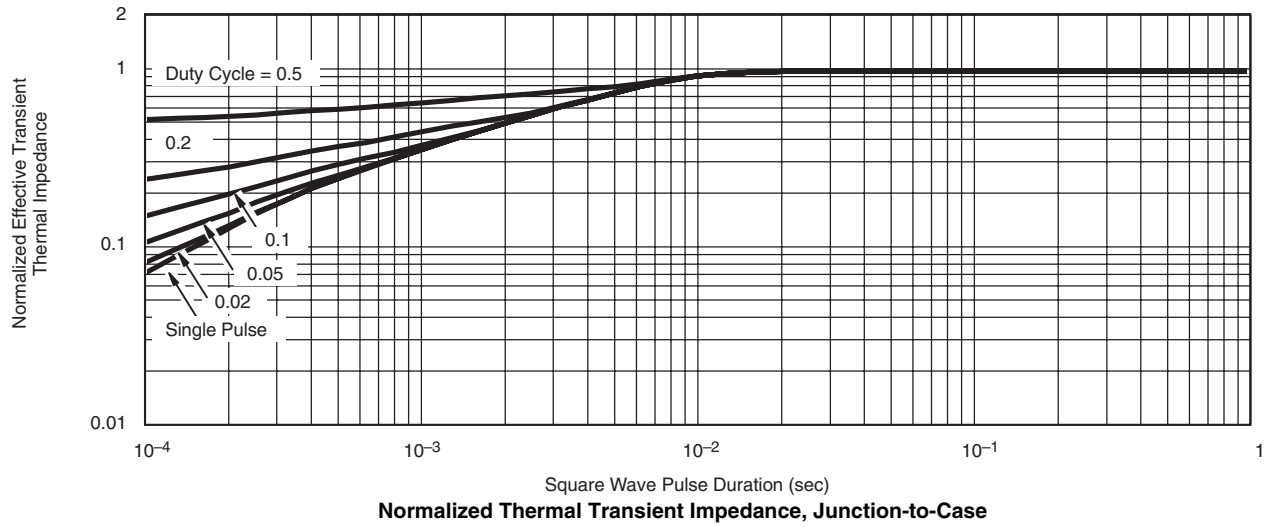


TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted





TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72341>.