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SL1700

T-77-07-13

MAC SIGNAL INPUT PROCESSOR AND DATA RECOVERY CIRCUIT

The SL1700 is a signal input processor and data recovery circuit for use in multistandard (D/D2-CMAC) MAC decoders. The SL1700 incorporates a video buffer with AGC and grey level clamping, an adaptive data slicer, and a 20.25MHz phase locked fundamental crystal oscillator. The output from the oscillator is buffered and divided to provide clock outputs of 20.25MHz and 10.125MHz.

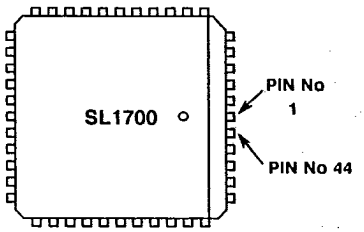
Associated GEC Plessey Semiconductors devices are MV1710, MV1720, MV1732, MV1733, MV1745, SP973T8, MV95338, VP101.

FEATURES

- Data and Clock Recovery for C-D-D2MAC Decoders
- Crystal Oscillator at 20.25MHz
- Video Amplifier with 6dB AGC Range
- Generates Voltage Reference Levels for the SP973T8 Video ADC
- Binary or Duo-binary Data Slicing
- 20.25MB/s and 10.125MB s Data Rate
- Buffered System Clock with Outputs of 20.25MHz and 10.125MHz
- 44-pin 'J' lead Plastic Chip Carrier Package

ABSOLUTE MAXIMUM RATINGS

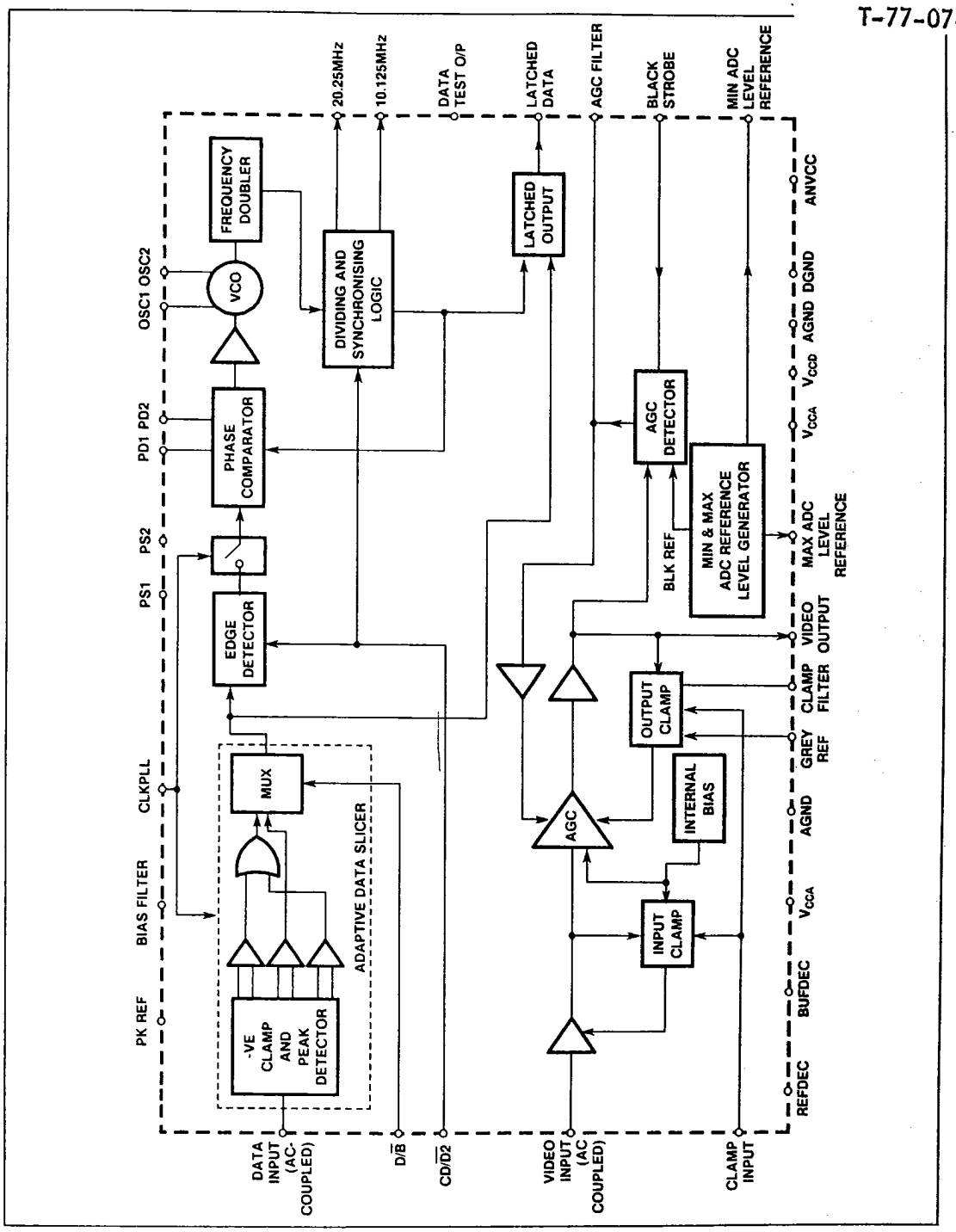
Analog supply voltage V_{CCA}	-0.3 to +12V
Digital supply voltage V_{CCD}	-0.3 to +6.5V
Storage temperature range	-55 to +125°C
Operating temperature range	0 to +70°C



HP44

Pin No.	Description	Pin No.	Description
1	OSC2	23	10MHz
2	N/C	24	20MHz
3	OSC1	25	CLAMP INPUT
4	ANALOG GND	26	BIAS FILTER
5	PD1	27	V_{CCA} (+10V)
6	PD2	28	VIDEO IN
7	N/C	29	N/C
8	PS1	30	DATA TEST O/P
9	PS2	31	O/P CLAMP FILTER
10	N/C	32	AGC FILTER
11	CD / $\overline{D2}$	33	GREY REF
12	D / $\overline{B}$	34	BLK STRB
13	N/C	35	N/C
14	DATA IN	36	N/C
15	PK REF	37	VIDEO OUT
16	REFDEC	38	ANALOG GND
17	ANVCC	39	N/C
18	N/C	40	ADC MIN. REF
19	V_{CCA} (+10V)	41	ADC MAX. REF
20	LATCHED DATA	42	N/C
21	CLK PLL	43	DIGITAL GND
22	V_{CCD} (+5V)	44	BUF DEC

Fig.1 Pin connections - top view
NOTE: N/C = No Internal Connection



Simplified block diagram of SL1700

FUNCTIONAL DESCRIPTION

The SL1700 provides the recovery of digital data, binary or duo-binary, and cancels the energy dispersal modulation. It also incorporates video processing with grey level clamping and AGC. The crystal oscillator is phase locked to the incoming data.

Data Slicer

The circuit incorporates an adaptive data slicer. The clamp circuits operate directly on the peak to peak excursions of the data input. The capacitors connected to the DATA and PK REF pins store the min and max data signal levels respectively. The data slicer operates at a 50% level for binary ($D/\overline{B}$ low) and at nominal 25% and 75% levels for duo-binary ($D/\overline{B}$ high).

Video Amplifier

The aim of the video circuitry is to pre-condition the MAC video signal (to a nominal level of 1.6Vp-p and 3.3V grey level) which is then input to the system ADC. The AGC circuitry utilises the internally generated black level reference. After the MAC control chip (MV1720) has achieved lock, correctly positioned CLAMP pulses are supplied to the SL1700 from the MV1720 and BLKSTRB pulses are supplied from the MV1710.

The CLAMP pulse gates the video clamp circuits when grey level occurs in the video waveform. Similarly, BLKSTRB gates the video AGC circuit when black level occurs in the video signal. The video amplifer is non-inverting with a minimum AGC range of 6dB.

ADC Minimum and Maximum Level References

Both minimum and maximum level references are generated on-chip. These references are used to drive each end of the external video ADC potential divider chain. The most suitable ADC for MAC is the SP973T8. The divider chain of the SP973T8 is centre tapped to provide a grey level reference used by the video clamp circuits. The black level reference (derived from the minimum level) is inset internally by approximately 15% to reduce the probability of clipping the video signal in the presence of overshoot.

Oscillator and Phase Comparator

A 20.252MHz crystal oscillator is connected to pin 1. A transition detector ensures that the oscillator is correctly phase locked to the incoming data stream which, via dividers and buffers provides the 20.25MHz and 10.125MHz system clock outputs.

Data Recovery

The latched data is re-synchronised with respect to the selected clock output (either 20.25MHz or 10.125MHz by means of the $CD/\overline{D2}$ input) as shown in Fig. 3. This ensures that adequate setup and hold times are available for the MV1720 control chip. The data output changes on the falling edge of the clock and is latched into the MV1720 on the rising edge of the clock.

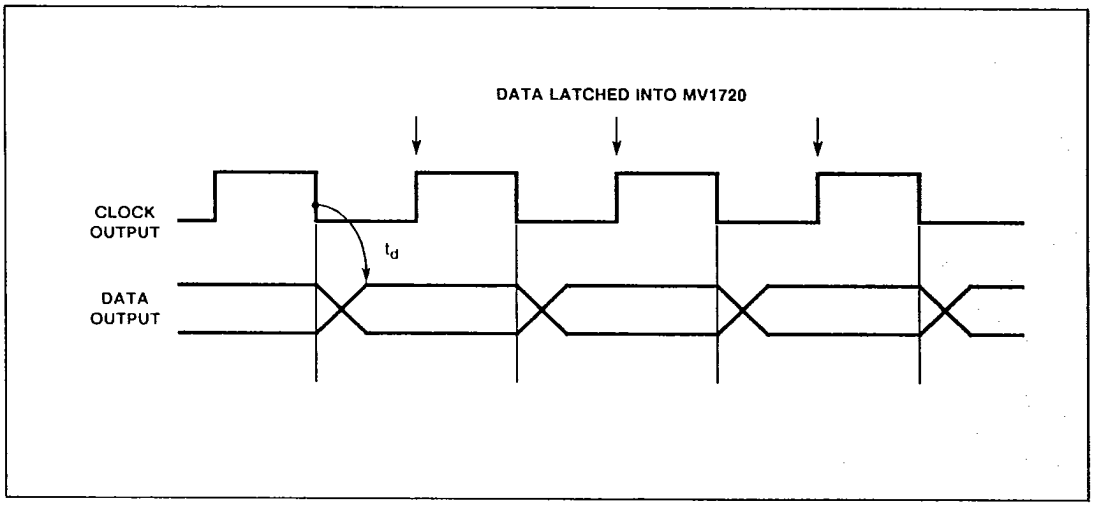


Fig.3 Data sampling

ELECTRICAL CHARACTERISTICS

Test Conditions (unless other wise stated)

T_{amb} = 25°C. V_{CCA} = 10V ± 5% on pins 27,19. V_{CCD} = 5V ± 5% on pin 22

Characteristic	Pins	Symbol	Value			Units	Conditions
			Min.	Typ.	Max.		
Total analog supply current	27,19	I_{CCA}			90	mA	Inputs and outputs floating
Digital supply current	43	I_{CCD}			63	mA	
CD/D2 input	11	I_{IH}			± 10	μA	
		I_{IL}		-1.08	-1.54	mA	
BLK STRB input and CLAMP input	34,25	I_{IH}		583	833	μA	$V_{IH} = V_{CCD}$
		I_{IL}			± 10	μA	V_{IL} = 0V
CLK PLL input	21	I_{IH}		7.5	11	μA	
		I_{IL}			± 10	μA	
D/B input	12	I_{IH}		-43	-61	μA	
		I_{IL}		-575	-821	μA	
TTL outputs	23,24, 20,30	V_{OH}	V_{CCD}-1V			V	I_{OH} = -5.0μA
		V_{OL}			0.5	V	I_{OL} = 1.6mA
Data input voltage (p-p)	14	V_D			1.2	V	
		Input Z	1			MΩ	
Video input voltage (p-p)	28	V_V	0.44		1.2	V	
		Input Z	1			MΩ	
Grey level input voltage (p-p)	33	V_G		3.3		V	
ADC max. ref O/P	41	V_W		4	4.3	V	I_{source} = 8mA Max. measured at DC
ADC min. ref O/P	40	V_B	2.0	2.3		V	I_{sink} = 8mA Max. measured at DC
Video Output	37						C_{LOAD} = 40pF
Amplitude (p-p)				1.4		V	
Source Z					20	Ω	
AGC range			6	8.9		dB	V_{IN} = 0.44Vp-p
Max. gain (Note 1)				3.2			V_{IN} = 1.2Vp-p
Min. gain (Note 1)				1.2			V_G = 3.3V
TILT (Note 2)				0.1			V_{IN} = 0.6Vp-p
Integral LIN (Note 3)				1			
VCO							See Table 1
Temperature coefficient		Δfo/ΔT		-2.3		ppm/°C	Note 4
VCO gain		KO		7		ppm/mV	Note 5
Phase Locked Loop							See Table 1
Total capture range				300		ppm	Note 6
Total hold range				600		ppm	Note 6
Clock output to data valid		t_d		10		ns	Measured from mid point on active edge of clock to mid point of data edge.
Rise time	20,	t_r		7		ns	10-90% C_{LOAD} = 15pF
Fall time	23,24	t_f		5		ns	90-10% C_{LOAD} = 15pF

NOTES

1. The gain is measured between VIDEO IN and VIDEO OUT with grey reference input = 3.3V.
2. Tilt refers to the degree of droop during one line period of a constant white level which is specified as a percentage of the black to white swing. Tilt is measured at VIDEO OUT.
3. Integral LIN is the peak deviation from a linear ramp between black and white during one line period and is specified as a percentage of the black to white magnitude.
4. The specified temperature coefficient includes the crystal, load capacitor and device effects.
5. Measured using a 20.252MHz series resonant crystal.
6. Measured with loop filter as shown in Fig. 4 on pins 4 and 5 with 1Vp-p MAC composite signal applied to the data input using the mid grey pattern from a Schlumberger SI7765 MAC signal generator, DMAC selected and CLKPLL held high.

Parameter	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Series Resonant fs = 20.2520MHz Series resistance at resonance Motional L Motional C			 10	 2 0.06	 Ω mH F	No Load Cap

Table 1 Crystal specification

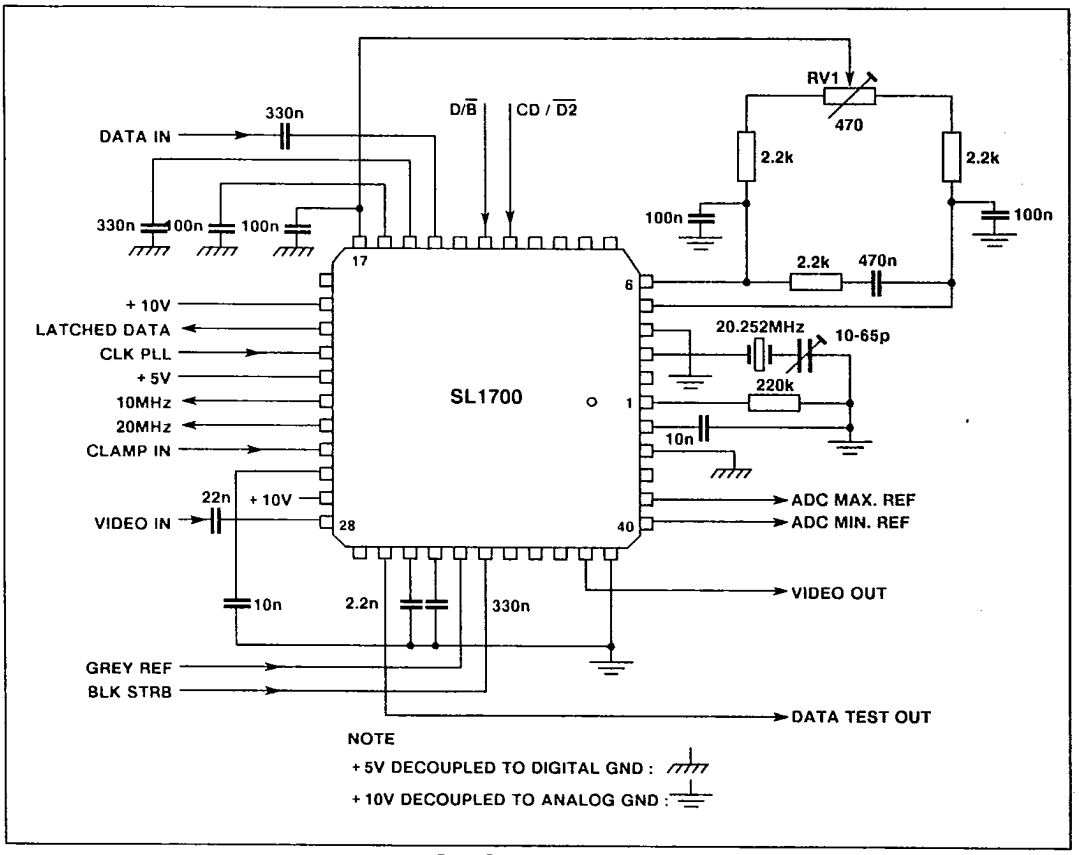


Fig.4 SL1700 test circuit

Power Supplies
Pins 19 and 27 are the analog V_{CC} pins (10V ± 5%) and pin 22 the digital V_{CC} pin (5V ± 5%). Pins 4,38 are the analog GND pins and pin 43 the digital GND. Separate analog and digital ground planes should be used, with the analog circuitry decoupled to the analog GNDs.

Voltage Controlled Oscillator (Pin 3)
The oscillator is designed to operate with a series fundamental resonant crystal. The crystal specification is detailed in Table 1.

To adjust the free running frequency of the oscillator, first short pins 5 and 6 together and adjust the trimmer capacitor for a frequency of 20.253MHz. Remove short on pins 5 and 6, then short together pins 8 and 9 and adjust RV1 (shown in Fig. 4) for a frequency of 20.253MHz.

PHASE SHIFT (Pins 8 and 9)
These pins should be shorted together when setting up the free running frequency of the oscillator no components are connected to these pins.

PHASE DETECTOR (Pins 5 and 6)
A low pass filter is connected at pins 5 and 6. Selection of the filter components will determine the capture and hold in range of the phase locked loop.

CD/D2 (Pin 11)
This TTL input is set high for CMAC or DMAC (20.25MBS) and low for D2MAC (10.0125MBS) operation.

D/B (Pin 12)
This TTL input is set high for duo-binary operation and low for binary operation.

Data In (Pin 14)
The MAC input signal is AC coupled to this pin via a 330nF capacitor.

PK REF (Pin 15)
A 330nF capacitor should be connected from PK REF to digital GND. The capacitor is required for the MAC data clamp circuitry.

Latched Data (Pin 20)
The latched data is TTL compatible using a totem pole output circuit.

CLKPLL (Pin 21)
The CLK PLL pulse from the MV1720 gates the PLL and the adaptive data slicer so that both sections of the SL1700 are active only during the data packet portion of the MAC signal.

10MHz Output (Pin 23)
The 10MHz system clock is TTL and CMOS compatible.

20MHz Output (Pin 24)
The 20MHz system clock is TTL and CMOS compatible.

ANVCC (Pin 17)
A decoupling capacitor from this pin to analog GND is required to decouple the on chip regulated supply a 100nF capacitor should be used.

REFDEC (Pin 16)
A decoupling capacitor from this an to analog GND is required to decouple the on chip reference generator. A 100nF capacitor should be used.

Clamp Input (Pin 25)
When clamp input is high, the SL1700 clamps the video to the grey level. See the MV1720 data sheet for timing information.

Video In (Pin 28)
The MAC input signal is AC coupled to this pin, via a 22nF capacitor with a minimum p-p value of 600mV.

Clamp Filter (Pin 31)
A 2.2nF capacitor should be connected from this pin to analog ground.

AGC Filter (Pin 32)
A 22nF capacitor should be connected from this pin to analog ground. This capacitor holds the video AGC levels between samples. It is recommended that a low leakage ceramic capacitor is used.

ADC Minimum Level Reference (Pin 40)
A buffered reference voltage (2.3V min) is provided for the SP973T8 ADC potential divider chain. This reference voltage is also used internally by the video AGC circuitry.

BLKSTRB (Pin 34)
When BLKSTRB is high, the SL1700 enables the AGC detector. See the MV1710 data sheet for timing information.

Video Output (Pin 37)
The signal output at pin 37 is an amplified version of the signal input at pin 28. The grey level of the video output is controlled by the grey level reference input at pin 33. The amplitude is controlled (via the AGC loop) by the internally generated black reference.

Grey Reference Input (Pin 33)
A reference voltage (3.3V nom) as derived from the ADC potential divider chain provides the reference to which the video output clamp adjusts the DC level of the MAC signal output.

ADC Maximum Reference (Pin 41)
A buffered reference voltage (4.3V max) is provided for the SP973T8 ADC potential divider chain.

BIAS FILTER (Pin 26)
A decoupling capacitor from this pin to analog GND is required to decouple the on-chip bias generator. A 10nF capacitor should be used.

BUF DEC (PIN44)
A decoupling capacitor from this pin to analog GND is required to decouple the supply to the oscillator circuit. A 10nF capacitor should be used.

DATA TEST OUTPUT (Pin 30)
This is a test pin providing access to the unlatched data output. The pin is TTL compatble using a totem pole output circuit.