SMH4812

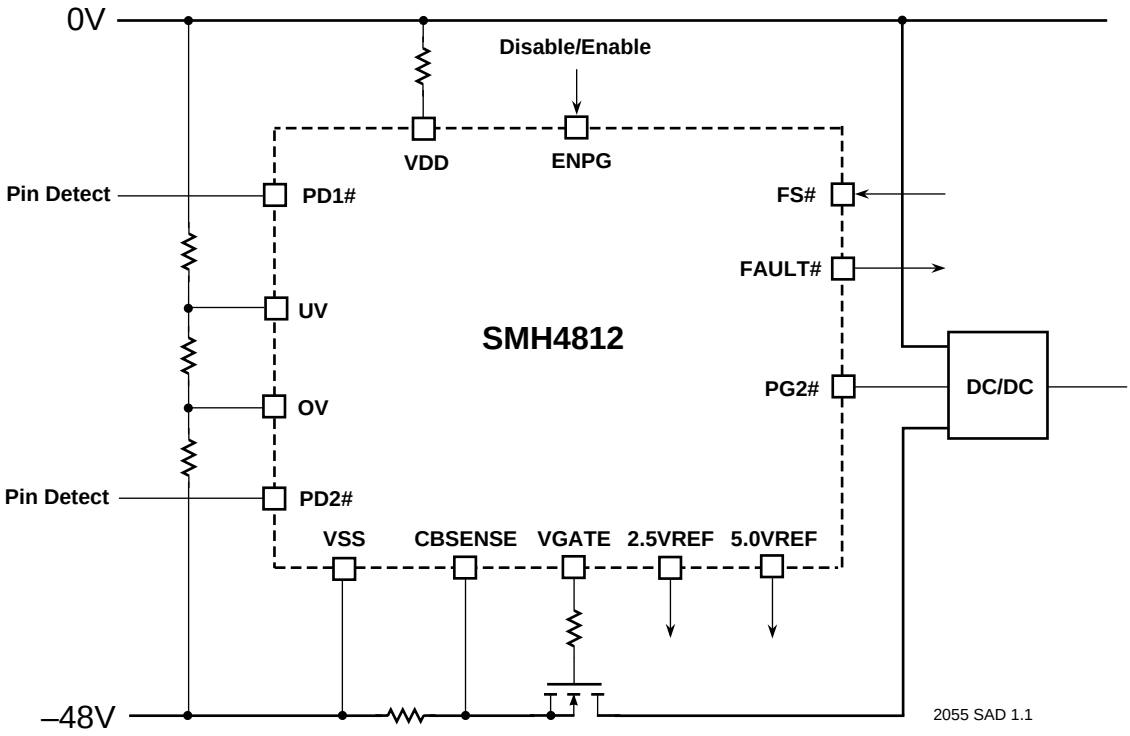
Distributed Power Hot-Swap Controller

Preliminary

FEATURES

- Soft Starts Main Power Supply on Card Insertion or System Power Up
- Senses Card Insertion via Short Pins or Ejector Switches
- Master Enable to Allow System Control of Power Up or Down
  - Can be used as a Temperature Sense Input
- Programmable Independent Controls of a DC/DC Converter
  - Not Enabled until Host Supply Fully Soft Started
  - Programmable Time Delay
  - Available Input to hold off Dependant Enables until Conditions are Satisfied
- Highly Programmable Circuit Breaker
  - Programmable Quick-Trip™ Values
  - Programmable Current Limiting
  - Programmable Duty Cycle Times
  - Programmable Over-current Filter
- Programmable Host Voltage Fault Monitoring
  - Programmable Under-Voltage Hysteresis
  - Programmable UV/OV Voltage Filter
  - Programmable Fault Mode: Latched or Duty Cycle
- Programmable Forced Shutdown Timer
- 2.5V and 5.0V Reference Outputs
  - Eliminates the Need for Other Primary Voltages
  - Easy Expansion of External Monitor Functions
- Supply Range ±20VDC to >±500VDC

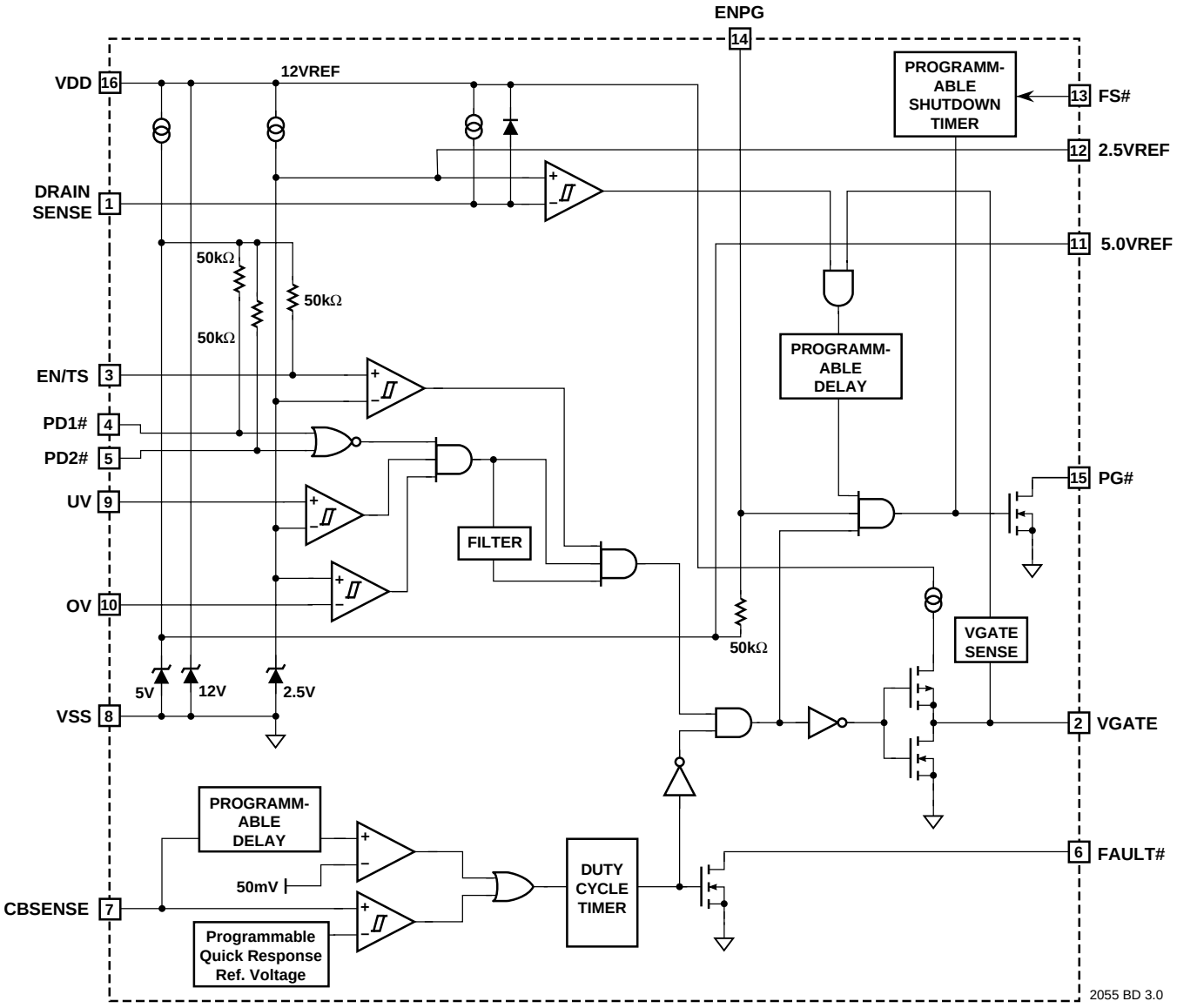
SIMPLIFIED APPLICATION DRAWING



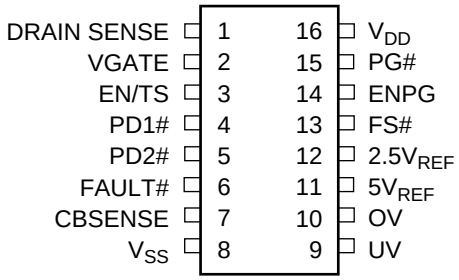
DESCRIPTION

The SMH4812 is designed to control hot swapping of plug-in cards operating from a single supply, which can have an output range from 20V to 500V. The SMH4812 hot-swap controller provides under-voltage and over-voltage monitoring of the host power supply, it drives an external power MOSFET switch that connects the supply to the load, and it protects against over-current conditions that might disrupt the host supply. When the input and output voltages to the SMH4812 controller are within specification it provides a Power Good logic output that may be used to enable a DC-DC converter. Additional features of the device include: temperature sense or master enable input, 2.5V and 5V reference outputs for expanding monitor functions, two Pin-Detect enable inputs for fault protection, and duty-cycle or latched over-current protection modes. All of these features can be programmed by the factory according to the user's requirements.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2055 PCon 2.0

PIN DESCRIPTIONS

DRAIN SENSE (1)

The DRAIN SENSE input monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. An internal 10µA source pulls the DRAIN SENSE signal towards the 5V reference level. DRAIN SENSE must be held below 2.5V to enable the PG outputs.

EN/TS (3)

The Enable/Temperature Sense input is the master enable input. If EN/TS is less than 2.5V, VGATE will be disabled. This pin has an internal 200kW pull-up to 5V.

PD1#, PD2# (4, 5)

These are logic level active low inputs that can optionally be employed to enable VGATE and the PG outputs when they are at V_{SS}. These pins each have an internal 50kW pull-up to 5V.

CBSENSE (7)

The circuit breaker sense input is used to detect overcurrent conditions across an external, low value sense resistor (R_S) tied in series with the Power MOSFET. A voltage drop of greater than 50mV across the resistor for longer than t_{CBD} will trip the circuit breaker. A programmable Quick-Trip sense point is also available.

UV (9)

The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if UV is less than 2.5V. Programmable internal hysteresis is available on the UV input, adjustable in increments of 62.5mV. Also available is a filter delay on the UV input.

OV (10)

The OV pin is used as an over-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if OV is greater than 2.5V. A filter delay is available on the OV input.

VGATE (2)

The VGATE output activates an external power MOSFET switch. This signal supplies a constant current output (100µA typical), which allows easy adjustment of the MOSFET turn on slew rate.

FAULT# (6)

FAULT# is an open-drain, active-low output that indicates the fault status of the device.

5VREF (11)

This is a precision 5V output reference voltage that may be used to expand the logic input functions on the SMH4812. The reference output is with respect to V_{SS}.

2.5VREF (12)

This is a precision 2.5V output reference voltage that may be used to expand the logic input functions on the SMH4812. The reference output is with respect to V_{SS}.

FS# (13)

The Forced Shutdown (FS#) pin is an active low input that causes VGATE and PG outputs to be shut down at any time after an internal hold-off timer has expired. The hold-off timer allows supervisory circuits on the secondary side (which are not powered up initially) to control shut down of the SMH4812 via an opto-isolator. This input has no pull-up resistor.

ENPG (14)

The ENPG input controls the PG# output. When ENPG is pulled low the PG# output is immediately placed in a high impedance state. If ENPG is driven high then the PG# output will immediately be driven low.

PG# (15)

PG# is an open-drain, active-low output with no internal pull-up resistor. It can be used to switch a load or enable a DC/DC converter. PG# is enabled immediately after VGATE reaches V_{DD} – V_{GT} and the DRAIN SENSE voltage is less than 2.5V. Voltage on these pins cannot exceed 12V, as referenced to V_{SS}.

V_{DD} (16)

V_{DD} is the positive supply connection. An internal shunt regulator connected between V_{DD} and V_{SS} develops approximately 12V that supplies the SMH4812. A resistor must be placed in series with the V_{DD} pin to limit the regulator current (RD in the application illustrations).

V_{SS} (8)

V_{SS} is connected to the negative side of the supply.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C
Terminal Voltage with Respect to V_{SS}:
V_{DD} ..... –0.5V to V_{DD}
OV, UV, DRAIN SENSE,
FS#, CBSENSE ..... –0.5V to V_{DD}+0.5V
PD1#, PD2#, ENPG, EN/TS 10V
FAULT#, PG# ..... –0.5V to V_{DD}+0.5V
VGATE ..... V_{DD}+0.5V

*COMMENT

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

AC OPERATING CHARACTERISTICS

Symbol	Description	Min.	Typ.	Max.	Units
t_{CBD}	Programmable 50mV Circuit Breaker delay (filter)		5		µs
			50 *		µs
			150		µs
			400		µs
t_{VGD}	Programmable Power Good delay		50		µs
			250		µs
			500		µs
			1500		µs
			5 *		ms
			20		ms
			80		ms
			160		ms
$t_{FSTSHTDN}$	Fast shutdown delay from Fault to V_{GATE} off		200		ns
t_{CYC}	Circuit breaker cycle time		2.5		s
t_{CBRST}	CB_{RESET} pulse width	200			ns
t_{PUVF}	Programmable Under-Voltage filter		OFF *		—
			5		ms
			80		ms
			160		ms
t_{PDD}	Programmable Pin Detect		0.5		ms
			5		ms
			80 *		ms
			160		ms

2055 Prog Table

* = Default value

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to** V_{SS}**, except** V_{GT})

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	I_{DD} = 3mA	11	12	13	V
$5V_{REF}$	5V reference output	I_{DD} = 3mA	4.75	5.00	5.25	V
I_{LOAD5}	5V reference output current	I_{DD} = 3mA	–1		1	mA
$2.5V_{REF}$	2.5V reference output	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
$I_{LOAD2.5}$	2.5V reference output current	I_{DD} = 3mA	–0.2		1	mA
I_{DD}	Power supply current				10	mA
V_{UV}	Under-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
V_{UVHYST}	Under-Voltage hysteresis	I_{DD} = 3mA		63		mV
V_{OV}	Over-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
V_{OVHYST}	Over-Voltage hysteresis	I_{DD} = 3mA		10		mV
V_{GATE}	V_{GATE} output voltage				V_{DD}	V
I_{GATE}	V_{GATE} current output			100		µA
V_{SENSE}	DRAIN SENSE threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
I_{SENSE}	DRAIN SENSE current output	$V_{SENSE} = V_{SS}$ (1)	9	10	11	µA
V_{CB}	Circuit breaker threshold	I_{DD} = 3mA	40	50	60	mV
V_{QCB}	Programmable Quick Trip circuit breaker threshold			200		mV
				100		mV
				60		mV
			Off			—
V_{ENTS}	EN/TS threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
$V_{ENTSHYST}$	EN/TS hysteresis	I_{DD} = 3mA		10		mV
V_{IH}	Input high voltage: ENPG		3		$5V_{REF}$	V
V_{IL}			0		2	V
V_{OL}	Output low voltage: FAULT#	I_{OL} = 3mA	0		0.4	V
	Output low voltage: PG#	I_{OL} = 3mA	0		0.4	V
I_{IL}	Input current: PD1#, PD2#, EN/TS	$V_{IL} = V_{SS}$		100		µA
V_{GT}	Gate threshold		0.7	1.8	3.0	V

2055 Elect Table

(1) TA = 25ºC.

RECOMMENDED OPERATING CONDITIONS

Temperature –40°C to 85°C.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The SMH4812 is an integrated power controller for hot swappable add-in cards. The device operates from a wide supply range and generates the signals necessary to drive an isolated output DC/DC converter. As a typical add-in board is inserted into the powered backplane physical connections must first be made with the chassis to discharge any electrostatic voltage potentials. The board then contacts the long pins on the backplane that provide power and ground. As soon as power is applied the device starts up, but does not immediately apply power to the output load. Under-voltage and over-voltage circuits inside the controller check to see that the input voltage is within a user-specified range, and pin detection signals determine whether the card is seated properly.

These requirements must be met for a Pin Detect Delay period of t_{PDD}, after which time the hot-swap controller enables VGATE to turn on the external power MOSFET switch. The VGATE output is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the drain sense input. When drain sense drops below 2.5V, and VGATE gets above $V_{DD} – V_{GT}$, the power good output can begin turning on the DC/DC controller. The Power Good Enable input may be used to activate or deactivate the output load.

Steady state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controller by shutting down the power MOSFET: an under-voltage or over-voltage condition on the host power supply; an over-current event detected on the CBSENSE input; a failure of the power MOSFET sensed via the DRAIN SENSE pin; the pin detect signals becoming invalid; the master enable (EN/TS) falling below 2.5V; the FS# input being driven low by events on the secondary side of the DC/DC controller. The SMH4812 may be configured so that after any of these events occur the VGATE output shuts off and either latches into an off state or recycles power after a cooling down period, t_{CYC}.

Powering V_{DD}

The SMH4812 contains a shunt regulator on the V_{DD} pin that prevents the voltage from exceeding 12V. It is necessary to use a dropper resistor (R_D) between the host power supply and the V_{DD} pin in order to limit current into the device and prevent possible damage. The dropper resistor allows the device to operate across a wide range of system supply voltages, and also helps protect the device against common-mode power surges. Refer to the Applications Section for help on calculating the R_D resistance value.

System Enables

There are several enabling inputs, which allow a host system to control the SMH4812. The Pin Detect pins (PD1# & PD2#) are two active low enables that are generally used to indicate that the add-in circuit card is properly seated. This is typically done by clamping the inputs to V_{SS} through the implementation of an injector switch, or alternatively through the use of a staggered pins at the card-cage interface. Two shorter pins arrayed at opposite ends of the connector force the card to be fully seated (not canted) before both pin detects are enabled. Care must be taken not to exceed the maximum voltage rating of these pins during the insertion process. Refer to details in the Applications Section for proper circuit implementation.

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input. These inputs must be held low for a period of t_{PDD} before a power-up sequence may be initiated.

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistive divider ladder to sense when the host supply voltage exceeds the user defined limits. If the input to the UV pin rises above 2.5V, or the input to the OV pin falls below 2.5V for a period of t_{PDD}, the power-up sequence may be initiated. The t_{PDD} filter helps prevent spurious start-up sequences while the card is being inserted. If UV falls below 2.5V or OV rises above 2.5V, the PG and VGATE outputs will be shut down immediately.

Under-/Over-Voltage Filtering

The SMH4812 may also be configured so that an out of tolerance condition on UV/OV will not shut off the output immediately. Instead, a filter delay may be inserted so that only sustained under-voltage or over-voltage conditions will shut off the output. When the UV/OV filter option is enabled an out of tolerance condition on UV/OV for longer than the filter delay time, t_{UOFLTR}, activates the FAULT# output, and the VGATE and PG outputs will be latched in the off state. See Figure 1. To initiate another power-up sequence the FAULT# output must first be reset. Refer to the appropriate section on resetting the FAULT# output. The Under-/Over-Voltage Filtering feature is disabled in the default configuration of the device.

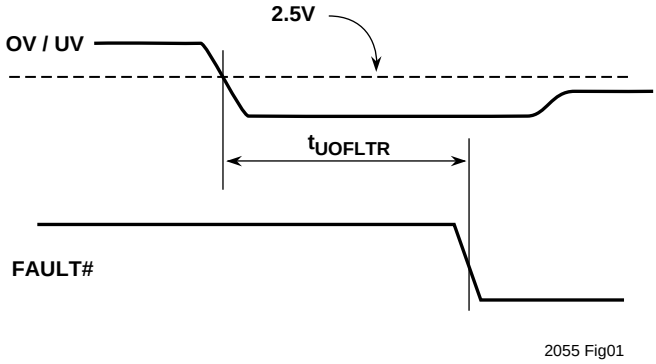


Figure 1. Under-/Over-Voltage Filter Timing

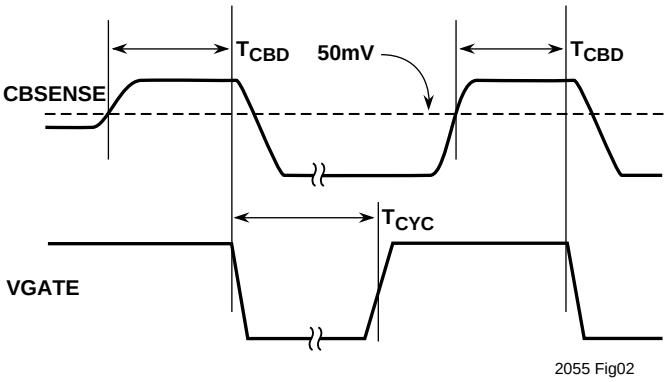


Figure 2. Circuit Breaker Cycle Mode

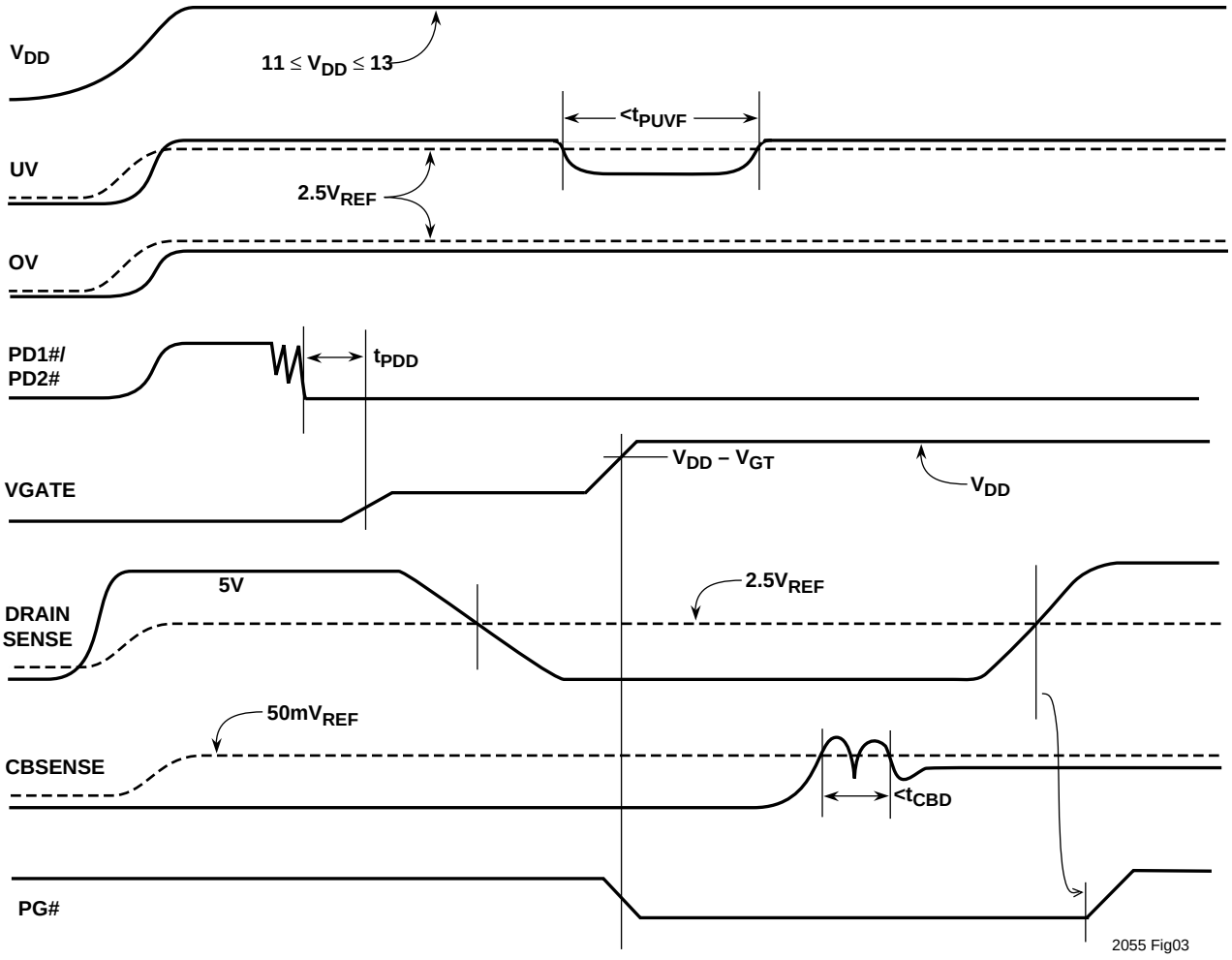


Figure 3. Power On Timing Sequence

Under-Voltage Hysteresis

The Under-Voltage comparator input may be configured with a programmable level of hysteresis. The compare level may be set in steps (up to 15) of 62.5mV below 2.5V. The default under-voltage hysteresis level is set to 62.5mV.

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC controllers have been met, the SMH4812 provides a means to soft start the external power FET. It is important to limit in-rush current to prevent damage to the add-in card or disruptions to the host power supply. For example, charging the filter capacitance (normally required at the input of the DC/DC controllers) too quickly may generate very high current. The VGATE output of the SMH4812 is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. The slew rate may be found by dividing I_{VGATE} by the gate-to-drain capacitance placed on the external FET. A complete design example is given in the Applications Section.

Load Control — Sequencing the Secondary Supplies

Once power has been ramped to the DC/DC controllers, two conditions must be met before the PG# output can be enabled: the Drain Sense voltage must be below 2.5V, and the VGATE voltage must be greater than $V_{DD} - V_{GT}$. The Drain Sense input helps ensure that the power MOSFET is not absorbing too much steady state power from operating at a high V_{DS}. This sensor remains active at all times (except during the current regulation period). The VGATE sensor makes sure that the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches $V_{DD} - V_{GT}$ this sensor is latched.

When the external MOSFET is properly switched on the PG# output may be enabled (if ENPG is high). Output PG# is activated after a t_{PGD} delay. The delay time is programmable from 50µs to 160ms.

The PG# output has a 12V withstand capability, so high voltages must not be connected to this pin. A bipolar transistor or an opto-isolator can be used to boost the withstand voltage to that of the host supply. See Figure 9 for connections.

Forced Shutdown — Secondary Feedback

The Forced Shutdown signal (FS#) is an active low input that provides a method of receiving feedback from the secondary side of the DC/DC controllers. A built-in holdoff timer allows the SMH4812 to ignore the state of the FS# input until the timer period expires. The FS# input must be driven high by the end of this timer period. A low level on this input will cause a Fault condition, driving FAULT# low and shutting off the VGATE and PG# outputs.

The purpose of the holdoff timer is to allow enough time for devices on the secondary side of the DC/DC controllers to power up and stabilize. This unique feature of the SMH4812 allows supervisory circuits such as an SMS44 to control the shutdown of the primary side soft start circuit, even though the secondary side initially has no power.

The FS# input can be programmed to act as a second ENPG input controlling the PG# output.

Circuit Breaker Operation

The SMH4812 provides a number of circuit breaker functions to protect against over current conditions. A sustained over-current event could damage the host supply and/or the load circuitry. The board's load current passes through a series resistor (R_S) connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}. The breaker trips whenever the voltage drop across R_S is greater than 50mV for more than t_{CBD} (a programmable filter delay ranging from 10µs to 500µs).

Quick-Trip™ Circuit Breaker

Additionally, the SMH4812 provides a Quick-Trip feature that will cause the circuit breaker to trip immediately if the voltage drop across R_S exceeds V_{QCB}. The Quick-Trip level may be set to 60mV, 100mV (default), 200mV, or the feature may be disabled.

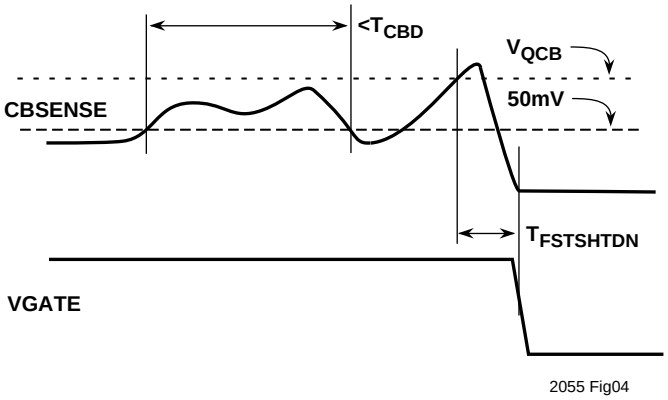


Figure 4. Circuit Breaker Quick Trip Response

Current Regulation

The current regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time. See Figures 5a and 5b. If enabled the device will start the internal timer when the voltage at CBSENSE exceeds 50mV (A & G, H). Also, it attempts to limit the voltage at CBSENSE to 60mV by regulating the VGATE output (B & C vs. I). The circuit breaker will trip if the over-current condition remains after the time-out (D, E, F; & J, K, L). However, if CBSENSE drops below 50mV before the timer ends, the timer is reset and VGATE resumes normal operation. If the Quick-Trip level is exceeded then the device will bypass the current regulation timer and shut down immediately. The Current Regulation feature is disabled in the default configuration.

Non-Volatile Fault Latch

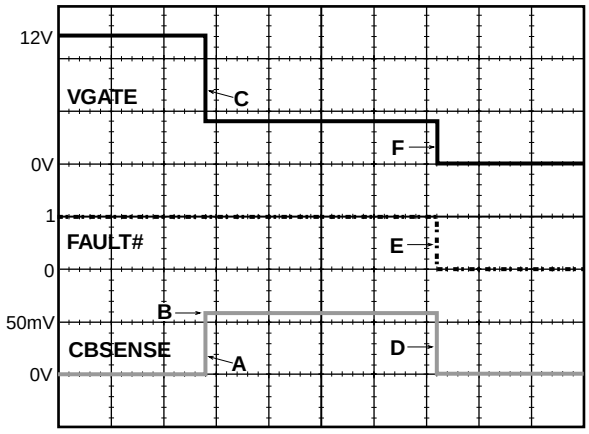
The SMH4812 also provides an optional nonvolatile fault latch (NVFL) circuit breaker feature. The nonvolatile fault latch essentially provides a programmable fuse on the circuit breaker. When enabled the nonvolatile fault latch will be set whenever the circuit breaker trips. Once set, it cannot be reset by cycling power.

NOTE: THE DEVICE REMAINS PERMANENTLY DISABLED UNTIL IT IS REPROGRAMMED AT THE FACTORY.

As long as the NVFL is set, the FAULT# output will be driven active. The Non-Volatile Fault Latch feature is disabled in the default configuration.

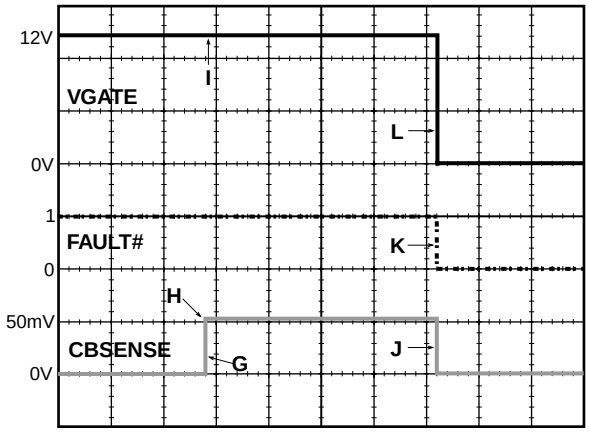
Resetting FAULT#

When the circuit breaker trips the VGATE output is turned off and FAULT# is driven low. In the default condition the breaker resets automatically after a time of t_{CYC}. In the latched condition cycling power to the board or toggling the EN/TS input will also reset the circuit breaker. If the over current condition still exists after the MOSFET switches back on, the circuit breaker will re-trip.



2055 Fig05a

Figure 5.a. Current Regulation & Shutdown



2055 Fig05b

Figure 5.b. Current Regulation & Shutdown

APPLICATIONS

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4812 hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

Over-Voltage and Under-Voltage Resistors

In the following examples, the three resistors, R1, R2, and R3, connected to the OV and UV inputs, must be capable of withstanding the maximum supply voltage of several hundred volts. The trip voltage of the UV and OV inputs is 2.5V relative to V_{SS}. As the input impedance of UV and OV is very high, large value resistors can be used in the resistive divider. The divider resistors should be high stability, 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (*i.e.*, the 48V supply can vary from 36V to 72V). The formulae for calculating R1, R2, and R3 follow.

First a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it can't be to high (self-heating in R3 will become a problem), or too low (the value of R3 becomes very large, and R3 becomes very expensive). To set the calculations a nominal value of 250µA will be assumed.

With V_{OV} (2.5V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}.$$

Substituting:

$$R1 = \frac{2.5V}{250\mu A} = 10k\Omega.$$

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}.$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{72V} = 125\mu A.$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} - V_{UV}}{ID_{MIN}}.$$

V_{UV} is the under-voltage trip point, also 2.5V. Substituting:

$$R3 = \frac{36V - 2.5V}{125\mu A} = 268k\Omega.$$

The closest standard 1% resistor value is 267kΩ

Then R2 is calculated:

$$(R1 + R2) = \frac{V_{UV}}{ID_{MIN}},$$

or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1.$$

Substituting:

$$R2 = \frac{2.5V}{125\mu A} - 10k\Omega = 20k\Omega - 10k\Omega = 10k\Omega.$$

Dropper Resistor Selection

The SMH4812 is powered from the high-voltage supply via a dropper resistor, R_D. The dropper resistor must provide the SMH4812 (and its loads) with sufficient operating current under minimum supply voltage conditions, but must not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - V_{DD_{MAX}}}{I_{DD} + I_{LOAD}},$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4812 supply voltage, I_{DD} is minimum current required for the SMH4812 to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

The min/max current limits are easily met using the dropper resistor, except in circumstances where the input voltage may swing over a very wide range (*e.g.*, input varies between 20V and 100V). In these circumstances it may be necessary to add an 11V zener diode between V_{DD} and V_{SS} to handle the wide current range. The zener voltage should be below the nominal regulation voltage of the SMH4812 so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4812 monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor, R_T, in series with the drain sense protection diode. This protection, or blocking, diode prevents high voltage breakdown of the drain sense input when the MOSFET switch is OFF. A low leakage MMBD1401 diode offers protection up to 100V. For high voltage applications (up to 500V) the Central Semiconductor CMR1F-10M diode should be used. The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} \times R_T) - V_{DIODE},$$

where V_{DIODE} is the forward voltage drop of the protection diode. The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of V_{DIODE} and I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 68kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 68k\Omega) - 0.5V = 1V.$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D (R_S + R_{ON}),$$

where I_D is the MOSFET drain current, R_S is the circuit breaker sense resistor and R_{ON} is the MOSFET on resistance.

The dropper resistor value should be chosen such that the minimum and maximum I_{DD} and V_{DD} specifications of the SMH4812 are maintained across the host supply's valid operating voltage range. First, subtract the minimum V_{DD} of the SMH4812 from the low end of the voltage, and divide by the minimum I_{DD} value. Using this value of resistance as R_D find the operating current that would result from running at the high end of the supply voltage to verify that the resulting current is less than the maximum I_{DD} current allowed. If some range of supply voltage is chosen that would cause the maximum I_{DD} specification to be violated, then an external zener diode with a breakdown voltage of ≈12V should be used across V_{DD}.

As an example of choosing the proper R_D value, assume the host supply voltage will range from 36 to 72V. The largest dropper resistor that can be used is: (36V-11V)/3mA = 8.3kΩ. Next, confirm that this value of R_D also works at the high end: (72V-13V)/8.3kΩ = 7.08mA, which is less than 10mA.

The FS# input can also be used in conjunction with a secondary-side supervisory circuit providing a positive feedback loop during the power up sequence. As an example, assume the SMH4812 is configured to turn on –48V to a DC/DC converter with a 1.6ms delay. Further assume all of the enable inputs are true and PG# has just been sequenced on. If FS# option 4 (100_{BIN} in register 5) has been selected, then FS# must be driven high within 1.6ms after PG# goes low, otherwise the PG output will be disabled. Ideally, there would be a secondary-side supervisor similar to the SMS44 that would have its reset timeout period programmed to be less than 1.6ms. After the supply turns on the RESET# output of the SMS44 would be released and FS# pulled high. However, if for any reason the supply doesn't turn on, the RESET# will not be released and the SMH4812 will disable the PG output.

APPLICATIONS CIRCUITS

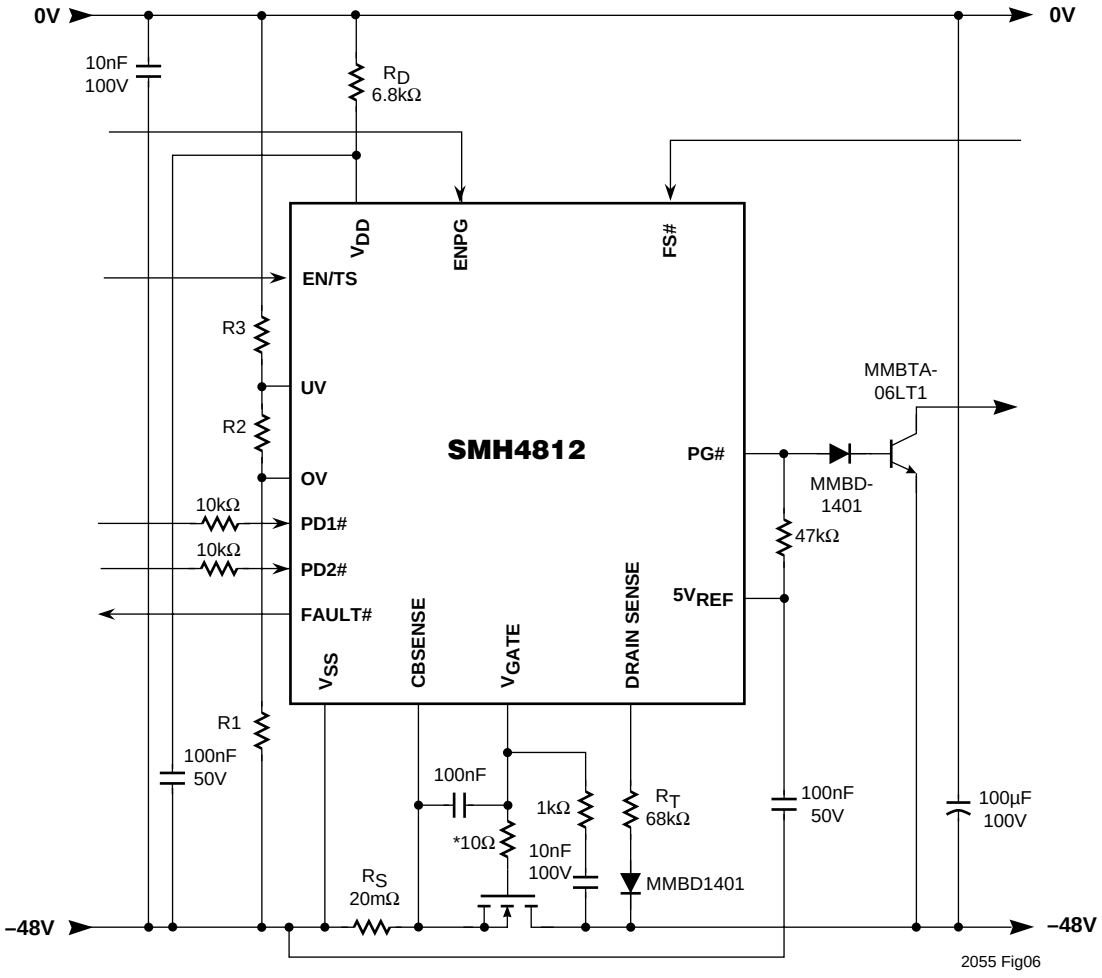


Figure 6. Changing Polarity of Power Good Output (PG#)

Note: Figures 6 through 9 — the *10Ω resistor must be located as close as possible to the MOSFET

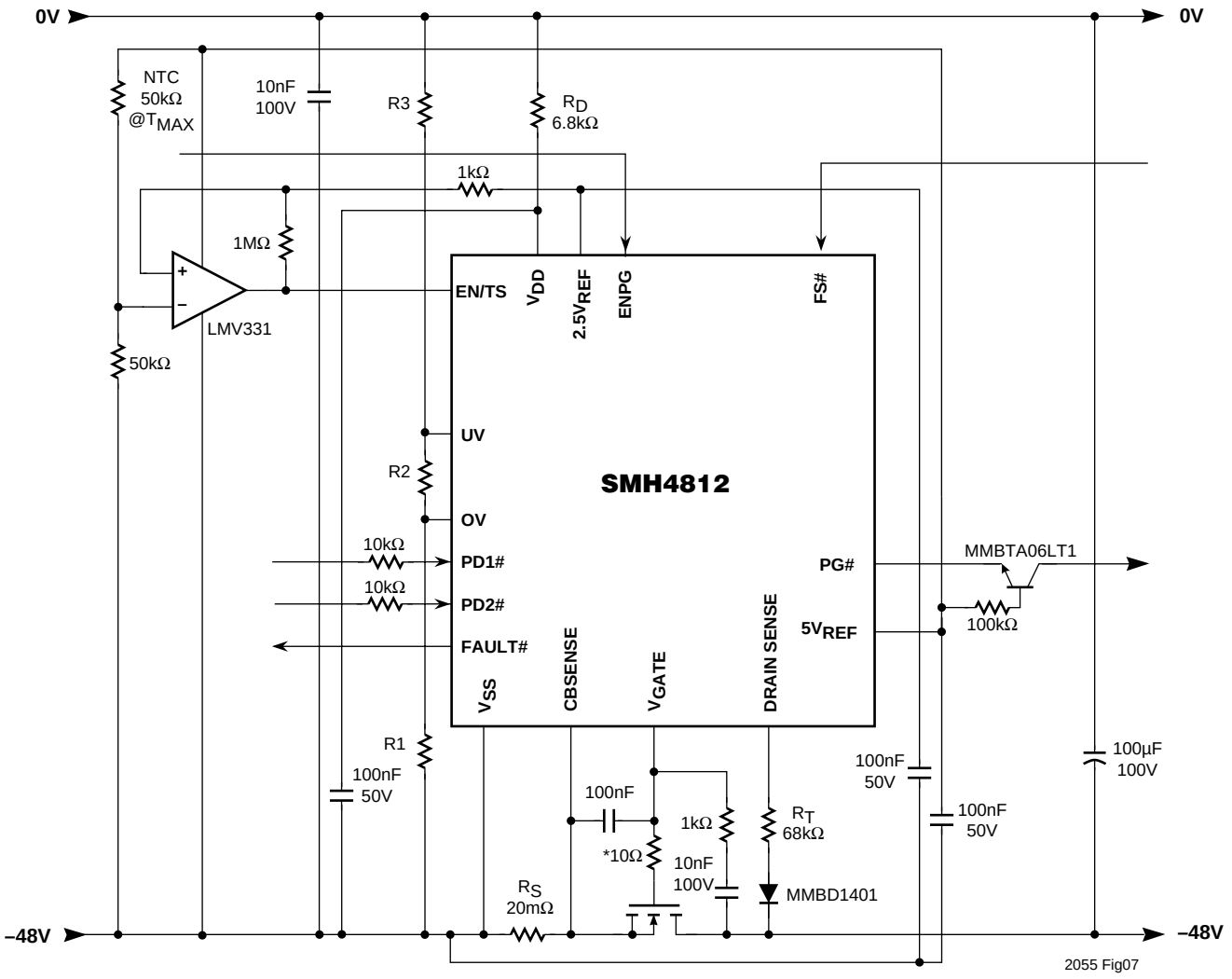


Figure 7. Overtemperature Shutdown

Note: Figures 6 through 9 — the *10Ω resistor must be located as close as possible to the MOSFET

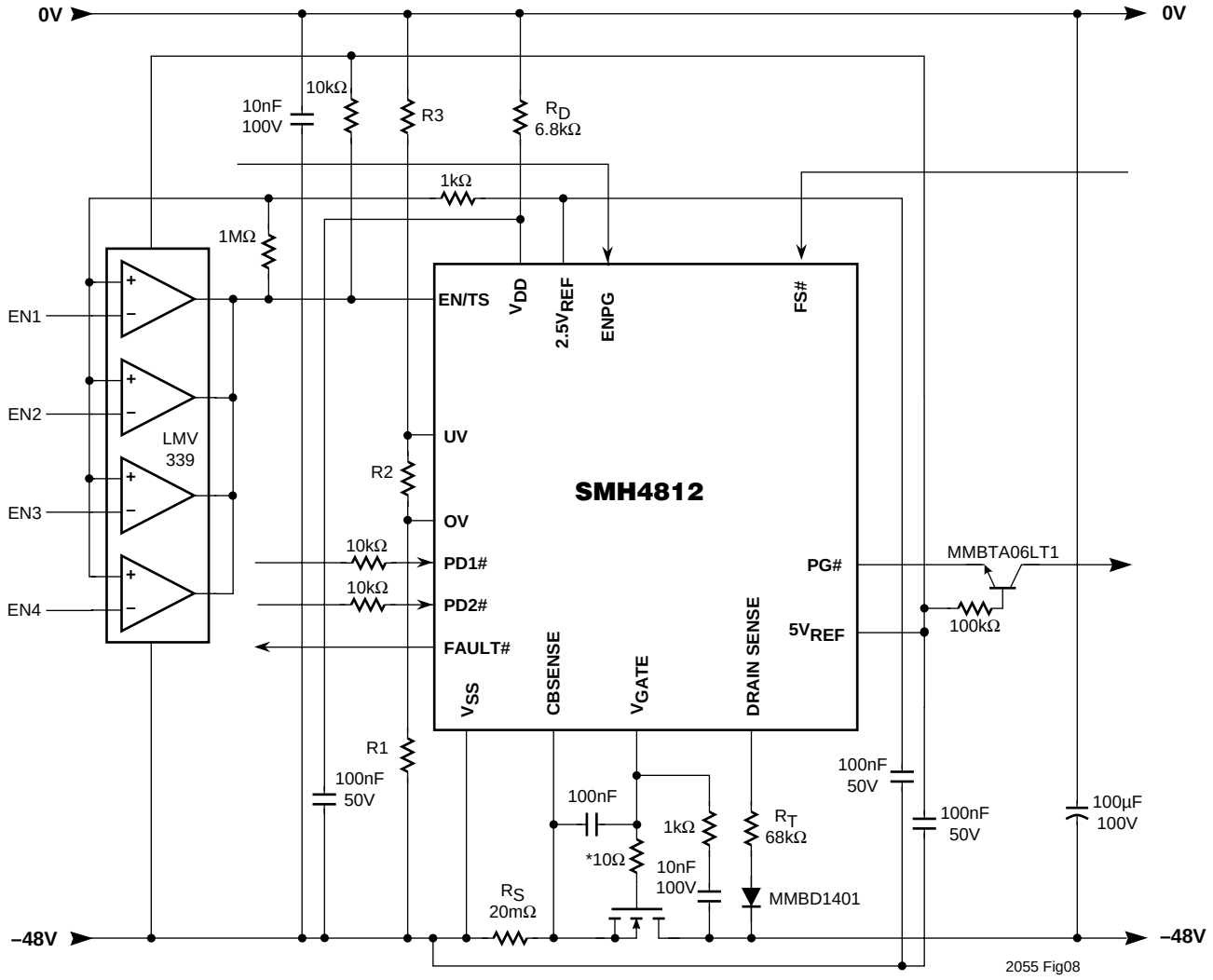


Figure 8. Expanding Input Monitoring Capability

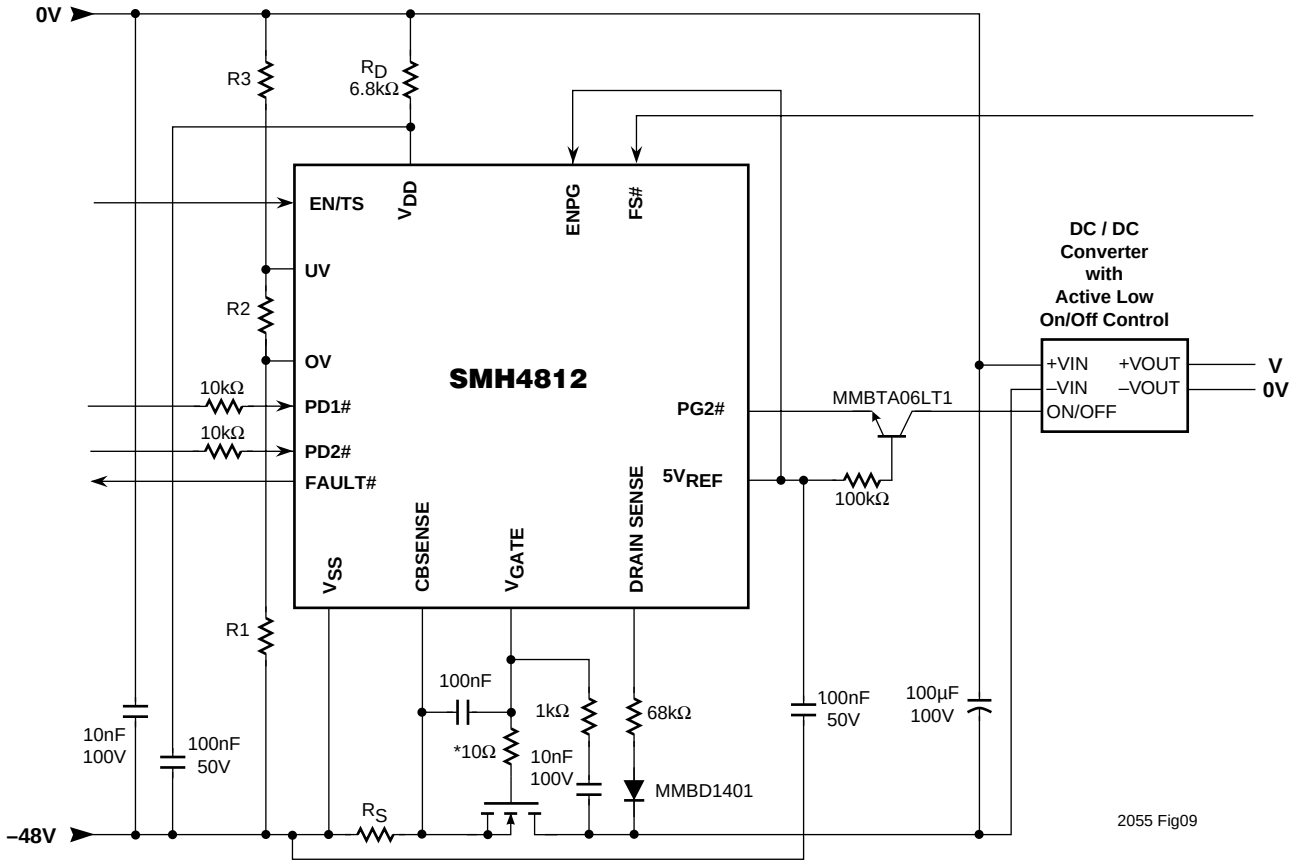


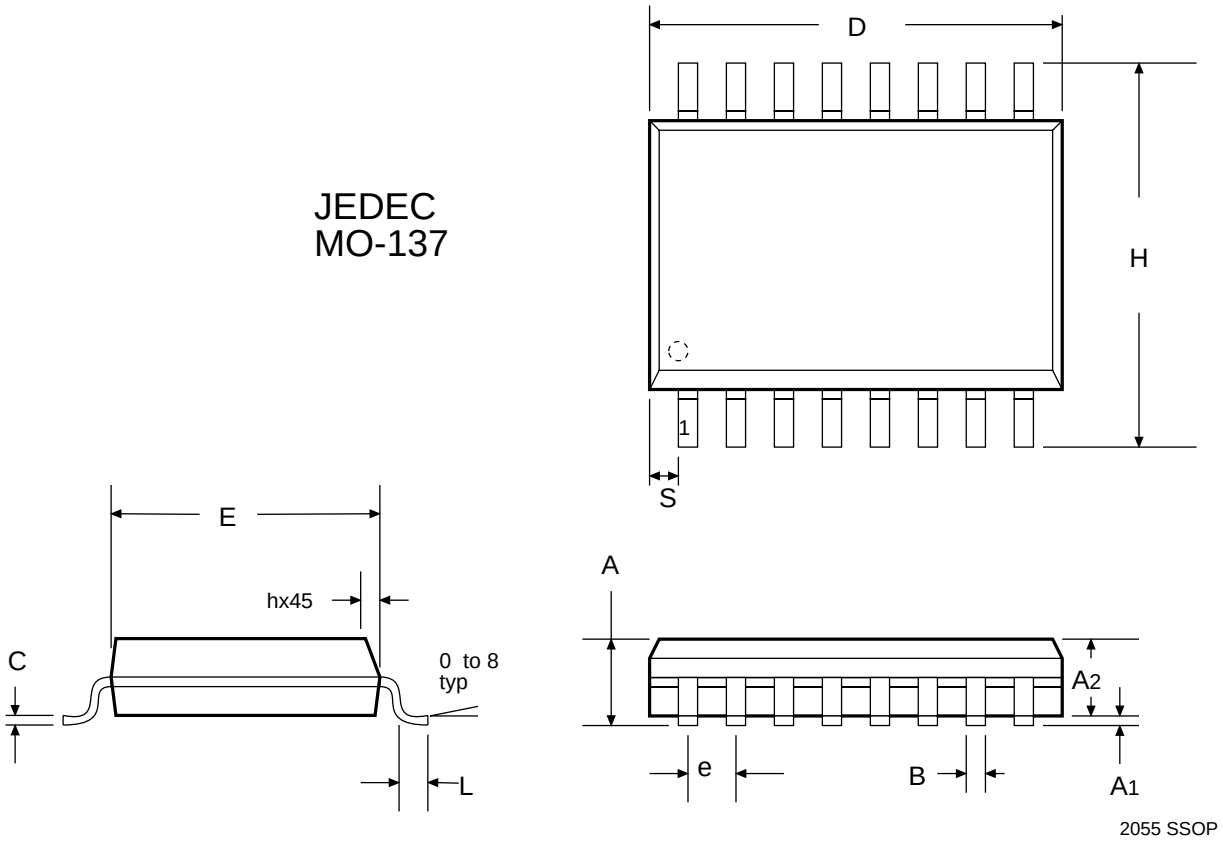
Figure 9. Typical Application for DC/DC Converter

Note: Figures 6 through 9 — the *10Ω resistor must be located as close as possible to the MOSFET

PACKAGES

SSOP PACKAGE

JEDEC
MO-137

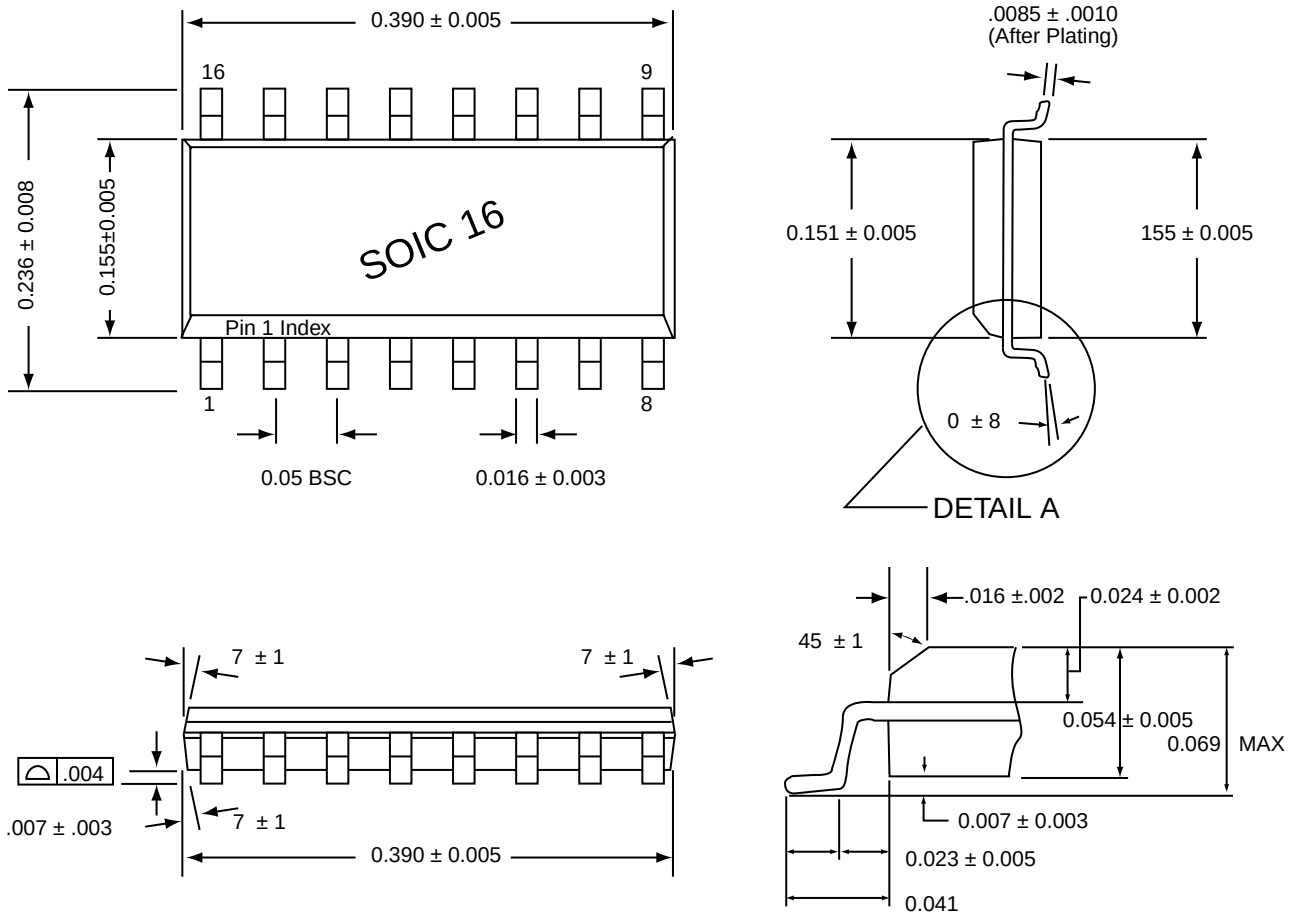


2055 SSOP

Dimension	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.061	0.064	0.068	1.55	1.63	1.73
A1	0.004	0.006	0.0098	0.12	0.15	0.25
A2	0.055	0.058	0.061	1.4	1.47	1.55
B	0.008	0.010	0.012	0.20	0.25	0.31
C	0.0075	0.008	0.0098	0.19	0.20	0.25
D	0.337	0.342	0.344	8.56	8.69	8.74
E	0.150	0.155	0.157	3.81	3.94	3.99
e	0.025BSC			0.635BSC		
H	0.230	0.236	0.244	5.84	5.99	6.20
h	0.010	0.013	0.016	0.25	0.33	0.41
L	0.016	0.025	0.035	0.41	0.64	0.89
S	0.0500	0.0525	0.0550	1.27	1.33	1.40

2055 SSOP Dim

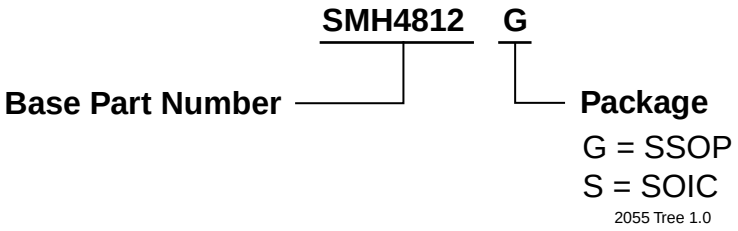
16 PIN SOIC PACKAGE



Note: 1. Reference: JEDEC publication MS-012 PTX 360-120
2. Unit: Inches
3. Mold flash, protrusion & gate burr shall not exceed 0.006 inch per side.

2055 SOIC 1.0

ORDERING INFORMATION



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