

Quad Programmable Precision Supervisory Controller With Independent Resets

FEATURES

- Operational from any of four Voltage Monitoring Inputs
- Four Independent Programmable Reset Outputs
- Programmability allows monitoring any voltage between 0.6V and 5.6V with no external components
- Programmable 5mV steps in the low range
- Programmable Watchdog Timer
- Programmable Reset Pulse Width
- Fault Status Register

APPLICATIONS

- Desktop/Notebook/Tablet Computers
- Multi-voltage Systems
- Telecom/Network Servers
- Portable Battery-powered Equipment
- Set-top Boxes
- Data-storage Equipment

INTRODUCTION

The SMS48 is a highly programmable voltage supply controller and supervisory circuit designed specifically for advanced systems that need to monitor multiple voltages. The SMS48 can monitor four separate voltages without the need of any external voltage divider circuitry. This alleviates the need for factory-trimmed threshold voltages and the use of external components to accommodate different supply voltages and tolerances.

The SMS48 has four programmable independent reset outputs to control different devices for varying reset conditions such as UV, OV, watchdog and user pushbutton applications.

The SMS48 watchdog timer has a user programmable time-out period and it can be placed in an idle mode for system initialization or system debug. All of the functions are user accessible through an industry standard I²C serial interface.

Programming of configuration, control and calibration values by the user is simplified with the SMX3200 interface adapter and Windows GUI software obtainable from Summit Microelectronics.

SIMPLIFIED APPLICATION DRAWING

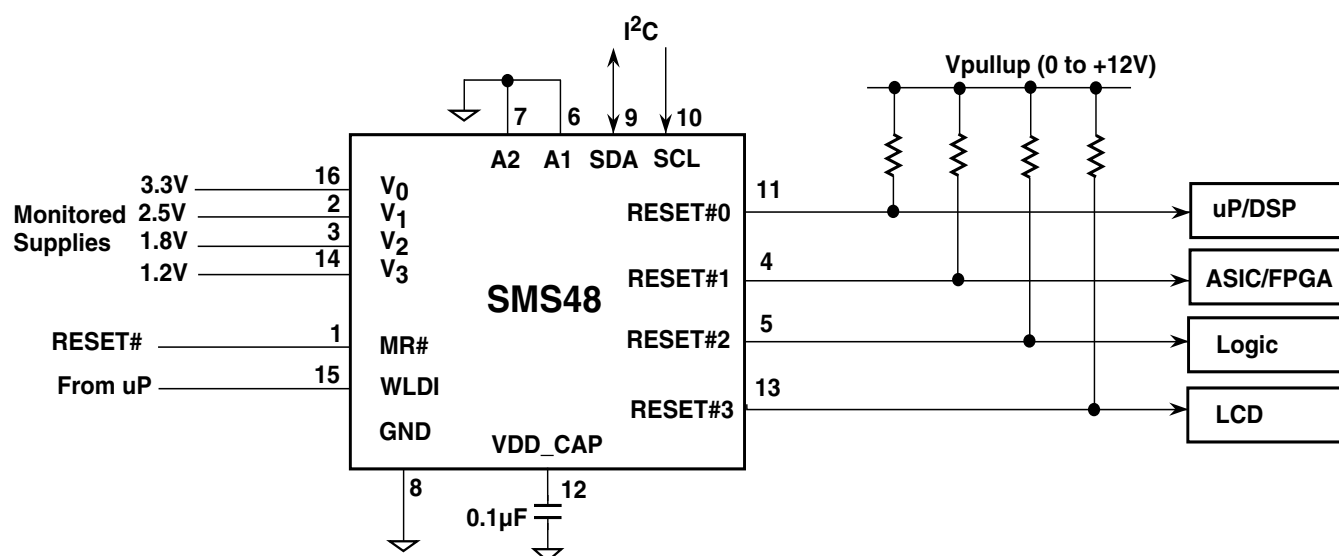
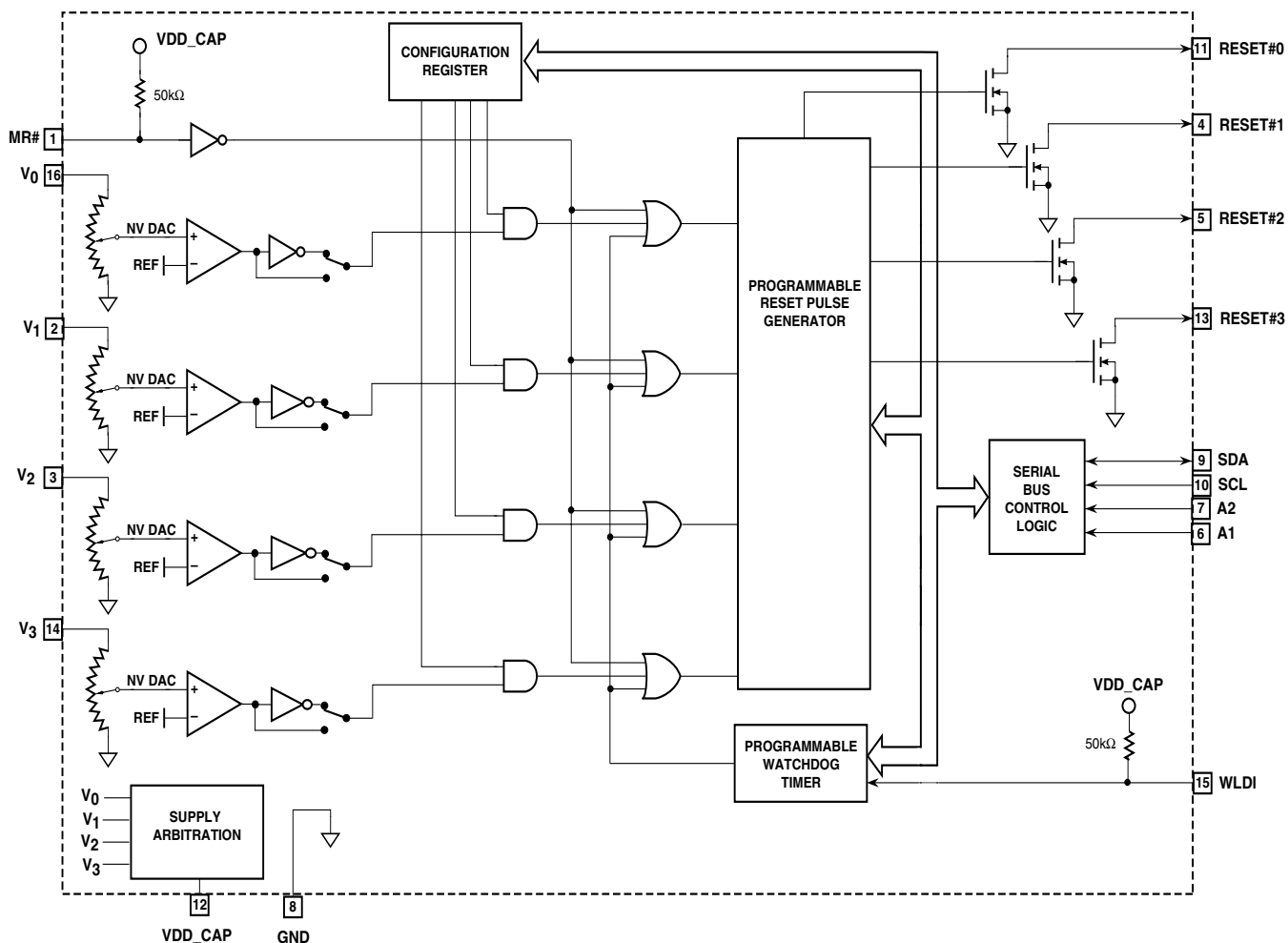


Figure 1 - Precision Quad Power Supply Monitor can monitor any voltage over the range of 0.6V to 5.6V. One of the four supplies must be above 2.7V to power the SMS48.



FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATION**

MR#	1	16	V ₀
V ₁	2	15	WLDI
V ₂	3	14	V ₃
RESET#1	4	13	RESET#3
RESET#2	5	12	VDD_CAP
A1	6	11	RESET#0
A2	7	10	SCL
GND	8	9	SDA

PIN NAMES

Pin	Name	Function
1	MR#	Manual reset input
2	V ₁	Voltage supply and monitor input
3	V ₂	Voltage supply and monitor input
4	RESET#1	Reset#1 output
5	RESET#2	Reset#2 output
6	A1	Address input
7	A2	Address input
8	GND	Power supply return
9	SDA	Serial data I/O
10	SCL	Serial data clock
11	RESET#0	Reset#0 output
12	VDD_CAP	Power supply output
13	RESET#3	Reset#3 output
14	V ₃	Voltage supply and monitor input
15	WLDI	Watchdog timer interrupt
16	V ₀	Voltage supply and monitor input

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	–55°C to 125°C
Storage Temperature	–65°C to 150°C
Lead Solder Temperature (10s)	300 °C
Terminal Voltage with Respect to GND:	
V ₀ , V ₁ , V ₂ , and V ₃	–0.3V to 6.0V
RESET#0-3	–0.3V to 15V
All Others	–0.3V to 6.0V
Junction Temperature.....	150°C
ESD Rating per JEDEC.....	2000V
Latch-Up testing per JEDEC.....	±100mA

*Note - Stresses beyond the listed Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Industrial Temperature Range.....	–40°C to +85°C.
Commercial Temperature Range.....	–5°C to +70°C.
V _{SUPPLY} Supply Voltage.....	2.7V to 5.5V
V _{SUPPLY} = Device supply voltage provided by the highest V _X input.	
Package Thermal Resistance (θJA)	
16 Lead SSOP.....	23°C/W
Moisture Classification Level 1 (MSL 1) per J-STD- 020	

RELIABILITY CHARACTERISTICS

Data Retention.....	100 Years
Endurance.....	100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
VDD	Operating supply voltage	1V min. refers to a valid reset output being generated	1.0		5.5	V
		Read/Write operations: at least one of the V inputs must be at or above VDD min.	2.7		5.5	V
IDD	Supply current	VDD ≤ 5.5V; V ₀ trip point 4.7V; V ₁ , V ₂ , V ₃ = GND; MR# = VDD; all outputs floating		200	400	μA
		Configuration register access			3	mA
V _{PTH} Range	Programmable threshold (low range)	Reset threshold voltage range V ₀ to V ₃ (5mV increments)	0.6		1.875	V
V _{PTH} Range	Programmable threshold (high range)	Reset threshold voltage range V ₀ to V ₃ (15mV increments)	1.8		5.625	V
V _{PTHACC}	Programmable threshold Accuracy	V _{PTH} is the programmed threshold setpoint within the V _{PTH} Range	–1.0	V _{PTH}	1.0	%
V _{HYST}	V _{RST} hysteresis	See Note 1 below		TBD		mV
R _{PU}	Pull-up resistance	MR# and WLDI pins		50		kΩ
V _{OL}	Low voltage output	I _{SINK} = 1mA, V _{VDD_CAP} ≥ 2.7V			0.3	V
		I _{SINK} = 200μA, V _{VDD_CAP} = 1.0V			0.3	V
V _{IL}	Input threshold				0.6	V
V _{IH}			0.7 × V _{DD}			V

Note 1: Low Range Hysteresis = 4.2 X (Vtrip - 0.5 volts) mV. For Vtrip = 1.0 volts, Hysteresis = 2.1 mV (0.21 %),
High Range Hysteresis = 12.6 X (Vtrip - 0.5 volts) mV. For Vtrip = 5.0 volts, Hysteresis = 56.7 mV (1.13%).

**AC OPERATING CHARACTERISTICS****(Over Recommended Operating Conditions; Voltages are relative to GND)**

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
t_{PRTO}	Programmable reset pulse width		19	25	31	ms
			38	50	63	ms
			75	100	125	ms
			150	200	250	ms
t_{DRST}	Vin to RESET# delay	100mV overdrive		20		μs
t_{PWDTO}	Programmable Watchdog timer period			OFF		—
			300	400	500	ms
			600	800	1000	ms
			1200	1600	2000	ms
			2400	3200	4000	
			4800	6400	8000	ms
T_{MR}	MR# input pulse width	Minimum pulse required to bring Reset active		300		ns
T_{DMRRST}	Delay from MR# low to RESET# low			200		ns

**PIN DESCRIPTIONS****V₀, V₁, V₂, V₃ (16, 2, 3, 14)**

These inputs are used as the voltage monitor inputs and as the voltage supply for the SMS48. Internally they are actively diode ORed and the input with the highest voltage potential will be the default supply voltage (VDD_CAP).

The RESET# outputs will be valid if any one of the four inputs is above 1V. However, for full device operation at least one of the inputs must be at 2.7V or higher.

The sensing threshold for each input is independently programmable in 5mV increments from 0.6V to 1.875V or 15mV increments from 1.8V to 5.625V. Also, the occurrence of an under- or over-voltage condition that is detected as a result of the threshold setting can be used to generate a RESET#0-3. The programmable nature of the threshold voltage eliminates the need for external voltage divider networks.

GND

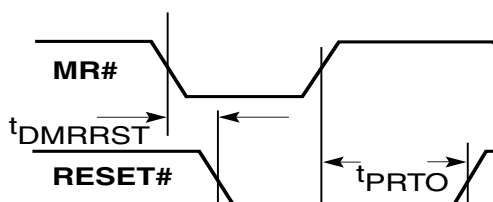
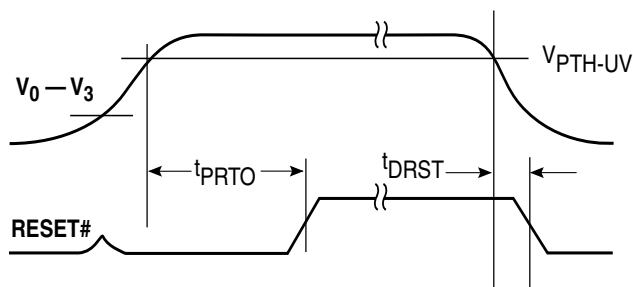
Power supply return.

MR# (1)

The manual reset input always generates a RESET#0-3 output whenever it is driven low. The duration of the RESET# output pulse will be initiated when MR# goes low and it will stay low for the duration of MR# low pulse plus the programmed reset time-out period (t_{PRT0}). MR# must be held low during a configuration register write or read. This signal is pulled up internally through a 50k Ω resistor.

RESET#0-3 (11, 4, 5, 13)

The reset outputs are active low open drain outputs. They are driven low whenever the MR# input is low or whenever a triggering under-voltage or over-voltage condition exists on the corresponding input channel or when the Watchdog timer expires. The four voltage monitor inputs are always functioning, but their ability to generate a reset is programmable (**configuration register 4**). Refer to Figures 2, 3 and 5 for a detailed illustration of the relationship between MR#, RESET#0-3 and the V_{IN} levels.

**Figure 2 - RESET# Timing with MR#****Figure 3 - RESET# Timing****VDD_CAP (12)**

The VDD_CAP pin connects to the internal supply voltage for the SMS48. A capacitor is placed on this pin to filter supply noise as well as hold up the device in the event of power failure. The voltage on this node is determined by the highest input voltage. Loading of this pin should be minimized to prevent excessive power dissipation in the part.

WLDI (15)

Watchdog input. A low to high transition on the WLDI input will clear the watchdog timer, effectively starting a new time-out period. This signal is pulled up internally through a 50k Ω resistor.

If WLDI is stuck low and no low-to-high transition is received within the programmed t_{PWDT0} period (programmed watchdog time-out) the RESET#0-3 outputs will be driven low.

Holding WLDI high will not block the Watchdog from timing out and generating a reset. Refer to Figure 4 for a detailed illustration of the relationship between RESET#0-3 and WLDI.

A1, A2 (6, 7)

A1 and A2 are the address inputs. When addressing the SMS48 configuration registers, the address inputs distinguish which one of four possible devices sharing the common bus is being addressed.

SDA (9)

SDA is the serial data input/output pin. It should be tied to VDD_CAP through a pull-up resistor.

**PIN DESCRIPTIONS (CONTINUED)****SCL(10)**

SCL is the serial clock input. It should be tied to V_{DD_CAP} through a pull-up resistor.

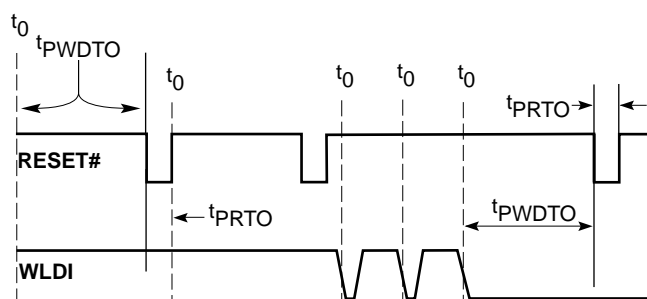


Figure 4 - Watchdog and WLDI Timing

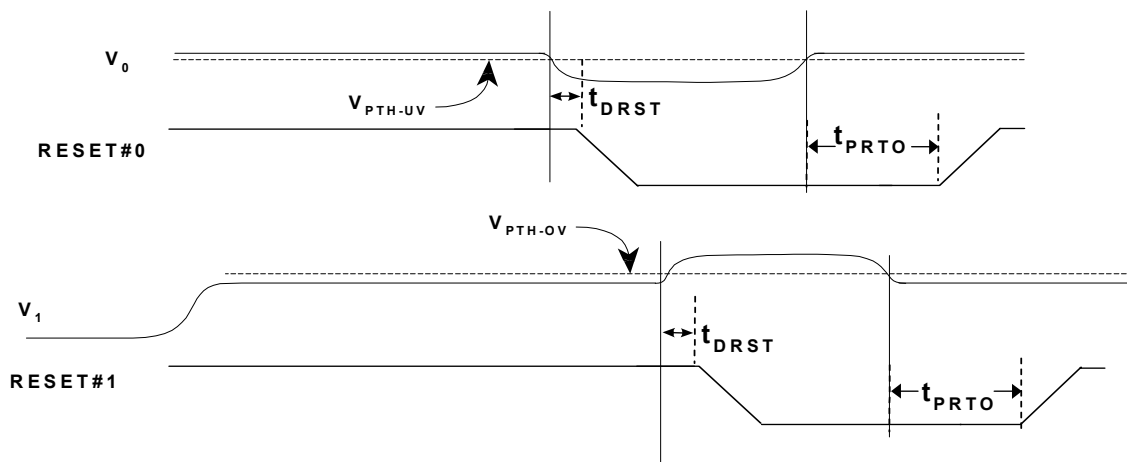


Figure 5 - V_{0-1} Inputs and Resulting RESET# Behavior with V_0 set to UV and V_1 set to OV sensing.



DEVICE OPERATION AND CONFIGURATION REGISTERS

SUPPLY AND MONITOR FUNCTIONS

The V_0 , V_1 , V_2 , and V_3 inputs are internally ORed so that any one of the four can act as the device supply. The RESET# outputs will be guaranteed true so long as one of the four pins is at or above 1V.

Note: for performing a Read or Write operation and to have the ability to change configuration register contents at least one supply input must be above 2.7V.

Read/Write operations require a 0.1 μ F capacitor from the VDD_CAP node to GND. For optimum performance connect capacitors from each of the V_x inputs to GND. Locate the capacitors as physically close to the SMS48 as possible.

Associated with each input is a comparator with a programmable threshold for detection of under-voltage or over-voltage conditions on any of the four supply inputs. The threshold can be programmed in 5mV increments anywhere within the range of 0.6V to 1.875V or 15mV increments within the range of 1.8V to 5.625V. Configuration registers 0, 1, 2, and 3 adjust the thresholds for V_0 , V_1 , V_2 , and V_3 respectively.

If the value contained in any register is all zeroes, the corresponding threshold will be 0.6V. If the contents were low range 05_{HEX} the threshold would then be 0.625V [0.6V + (5 \times 0.005V)]. All four registers are configured as 8-Bit registers.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Action
1	1	1	1	1	1	1	1	Highest threshold adjustment = 5.625V (High Range)
0	0	0	0	0	0	0	0	Lowest threshold adjustment = 0.6V (Low Range)
0	0	0	0	0	1	1	0	Threshold = 0.6V + (6 \times 0.005V) = 0.625V (e.g.)

Table 1. Configuration Registers 0, 1, 2, and 3

RESET# FUNCTION

Each RESET# output has a programmable source for activation. Configuration register 4 is used for enabling the activation source. A monitor input can be programmed to activate on either an under-voltage or over-voltage condition, but not both conditions. When this condition ceases, each individual RESET# output will remain active for t_{PRT0} (programmable reset time-out). The reset threshold voltage range for V_0 to V_3 can be set for 5mV increments below 1.875V (low Range = "0") or for 15mV increments above 1.8V (high range = "1") using Bits D3:0.

The RESET#0-3 outputs have two hardwired sources for activation: the MR# input and Watchdog timer. All

RESET# outputs will remain active so long as MR# is low, and will continue driving the RESET# outputs for t_{PRT0} (programmable reset time out) after MR# returns high. The MR# input cannot be bypassed or disabled.

Refer to Figures 1, 2 and 3 for a detailed illustration of the relationships among the affected signals.

The SMS48 provides the option of the monitors triggering on either an under-voltage or over-voltage condition. The low-order four bits of configuration register 5 program these options.

WATCHDOG TIMER

The SMS48 contains an independent timer that can be programmed. The Watchdog generates all RESET#s if it times out. The timer is cleared by a low to high transition on WLDI and will reset all four RESET#.

If the watchdog should time-out the device status can be monitored in the status register (Table 4). Refer to Figure 3 which illustrates the action of RESET#0-3 with respect to the Watchdog timer and the WLDI input.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Action
X	X	X	X	V_3	V_2	V_1	V_0	
RESET Trigger Enable				Voltage Threshold Range Select				
				0	0	0	0	Low Range
				1	1	1	1	High Range

Table 2. Configuration Register 4



DEVICE OPERATION AND CONFIGURATION REGISTERS (CONTINUED)

Action	D3 MSB	D2	D1	D0 LSB
	V ₃	V ₂	V ₁	V ₀
Writing a 0 enables undervoltage detection for the selected V input	0	0	0	0
Writing a 1 enables overvoltage detection for the selected V input	1	1	1	1

Table 3. Configuration Register 5 (D0 through D3)

If WLDI is held low the timer will free-run generating a series of resets. When RESET# returns high (after t_{PRTO}) the timer is reset to time zero. Register 6 is also used to set the programmable reset time-out period (t_{PRTO}).

D7 MSB	D6	D5	D4 LSB	Action
V ₃	V ₂	V ₁	V ₀	
0	0	0	0	Reading a 1 indicates the source of out of limit fault
1	1	1	1	

Table 4. Status Register 5 (D4 through D7)

D7 MSB	D6	D5	D4	D3	Action
Read ¹ Only	RTO1	RTO0	Read Only	Read Only	
1	0	0	x	x	t _{PRTO} = 25ms
1	0	1	x	x	t _{PRTO} = 50ms
1	1	0	x	x	t _{PRTO} = 100ms
1	1	1	x	x	t _{PRTO} = 200ms

Table 5. Configuration Register 6 (D3 through D7)

Note 1 - Read Only bit D7 is set to a 1. Read only bits D4 and D3 are revision control and the value indicates the status code of the device (ie. 01 is status code 1).

Action	D2	D1	D0 LSB
	WD2	WD1	WD0
OFF	0	0	0
400ms	0	1	1
800ms	1	0	0
1600ms	1	0	1
3200ms	1	1	0
6400ms	1	1	1

Table 6. Configuration Register 6 (D0, D1, D2)

D7 MSB	D6	Action
Lock	AS0	
x	x	
0	x	Config. Reg. Read/Write enabled
1	x	Config. Reg. Read/Write locked out ¹

Note 1 - Setting this bit will cause a permanent Read/Write Lock out.

Table 7. Configuration Register 7 (D7, D6) Bits D5 through D0 are not used.



DEVELOPMENT HARDWARE & SOFTWARE

SMX3200 PROGRAMMER

The end user can use the summit SMX3200 programming cable and software that have been developed to operate with a standard personal computer. The programming cable interfaces directly between a PC's parallel port and the target application. The application's values are entered via an intuitive graphical user interface employing drop-down menus.

The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMS48 via the programming Dongle and cable. An example of the connection interface is shown in Figure 6.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

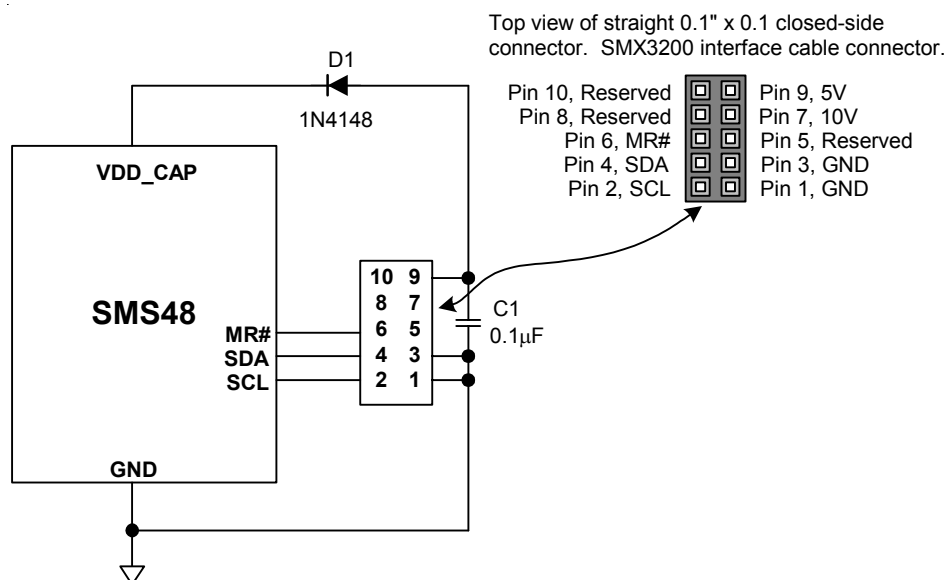


Figure 6 - SMX3200 Programmer I²C serial bus connections to program the SMS48.

**I²C INTERFACE****CONFIGURATION REGISTER OPERATION**

Data for the configuration registers are read and written via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. See Operating Characteristics: Table 8 and Figure 7.

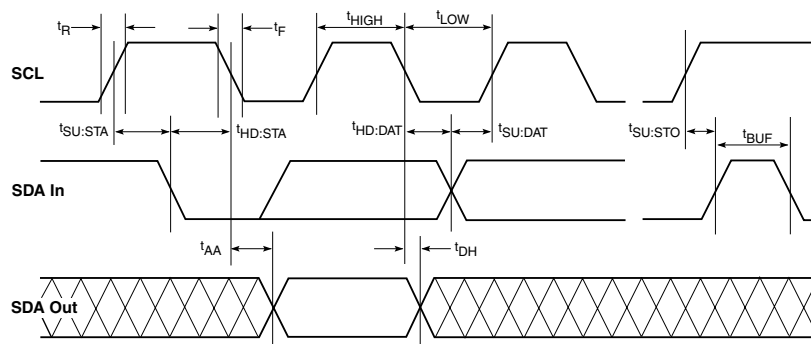
Input Data Protocol

The protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. In all cases the SMS48 will be a Slave device, since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time because changes on the data line while SCL is high will be interpreted as start or stop condition.

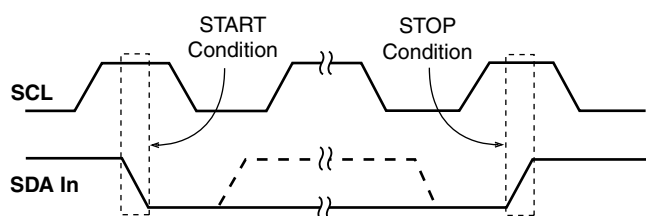
Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
f_{SCL}	SCL clock frequency		0		100	kHz
t_{LOW}	Clock low period		4.7			μ s
t_{HIGH}	Clock high period		4.0			μ s
t_{BUF}	Bus free time (1)	Before new transmission	4.7			μ s
$t_{SU:STA}$	Start condition setup time		4.7			μ s
$t_{HD:STA}$	Start condition hold time		4.0			μ s
$t_{SU:STO}$	Stop condition setup time		4.7			μ s
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.2		3.5	μ s
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.2			μ s
t_R	SCL and SDA rise time (1)				1000	ns
t_F	SCL and SDA fall time (1)				300	ns
$t_{SU:DAT}$	Data In setup time		250			ns
$t_{HD:DAT}$	Data In hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t_{WR}	Write cycle time				5	ms

Note (1): These values are guaranteed by design.

Table 8. I²C Operating Characteristics**Figure 7 - I²C Operating Characteristics**

**I²C INTERFACE (CONTINUED)****START and STOP Conditions**

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the Start condition. A low-to-high transition on the data line, while the clock is high, is defined as the Stop condition. See Figure 8.

**Figure 8 - START and STOP Conditions****Acknowledge (ACK)**

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the Master or the Slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to Acknowledge that it received the eight bits of data. The Master will leave the SDA line high (NACK) when it terminates a read function.

The SMS48 will respond with an Acknowledge after recognition of a Start condition and its slave address byte. If both the device and a write operation are selected the SMS48 will respond with an Acknowledge after the receipt of each subsequent 8-Bit word. In the READ mode the SMS48 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected and no Stop condition is generated by the Master, the SMS48 will continue to transmit data. If a NACK is detected the SMS48 will terminate further data transmissions and await a Stop condition before returning to the standby power mode.

Device Addressing

Following a Start condition the Master must output the address of the Slave it is accessing. The most significant four bits of the Slave address are the device type identifier/address. For the SMS48 the default is 1001_{BIN}. The next two bits are the Bus Address. The next bit (the 7th) is the MSB of the configuration address.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
Address Bits							
Device Type				Bus		MSB	R/W
SMS48				x	x	x	x
1	0	0	1	⇐ Configuration Register			

Table 9. Slave Addresses**Read/Write Bit**

The last bit of the data stream defines the operation to be performed. When set to 1 a Read operation is selected; when set to 0 a Write operation is selected.

WRITE OPERATIONS

The SMS48 uses byte Write operations. A byte Write operation writes a single byte during the nonvolatile write period (t_{WR}).

Byte Write

After the Slave address is sent (to identify the Slave device and select either a Read or Write operation), a second byte is transmitted which contains the low order 8 bit address of any one of the 256 words in the array. Upon receipt of the word address the SMS48 responds with an Acknowledge. After receiving the next byte of data it again responds with an Acknowledge. The Master then terminates the transfer by generating a Stop condition, at which time the SMS48 begins the internal Write cycle. While the internal Write cycle is in progress the SMS48 inputs are disabled and the device will not respond to any requests from the Master.

Acknowledge Polling

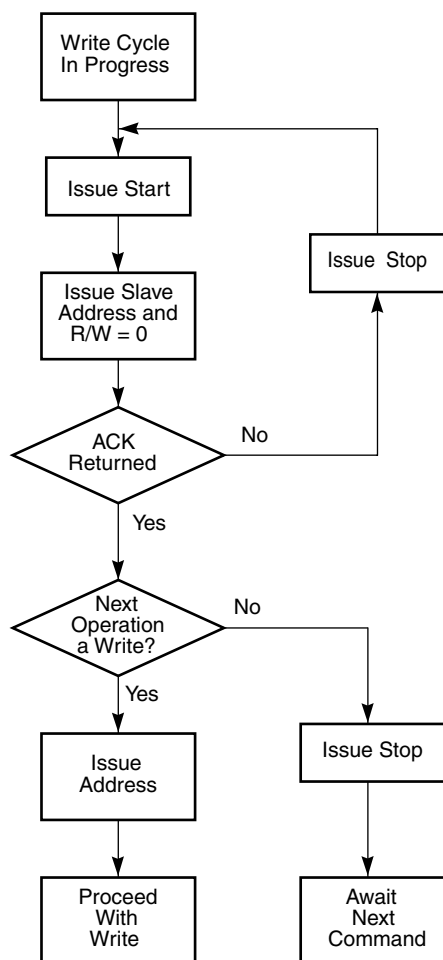
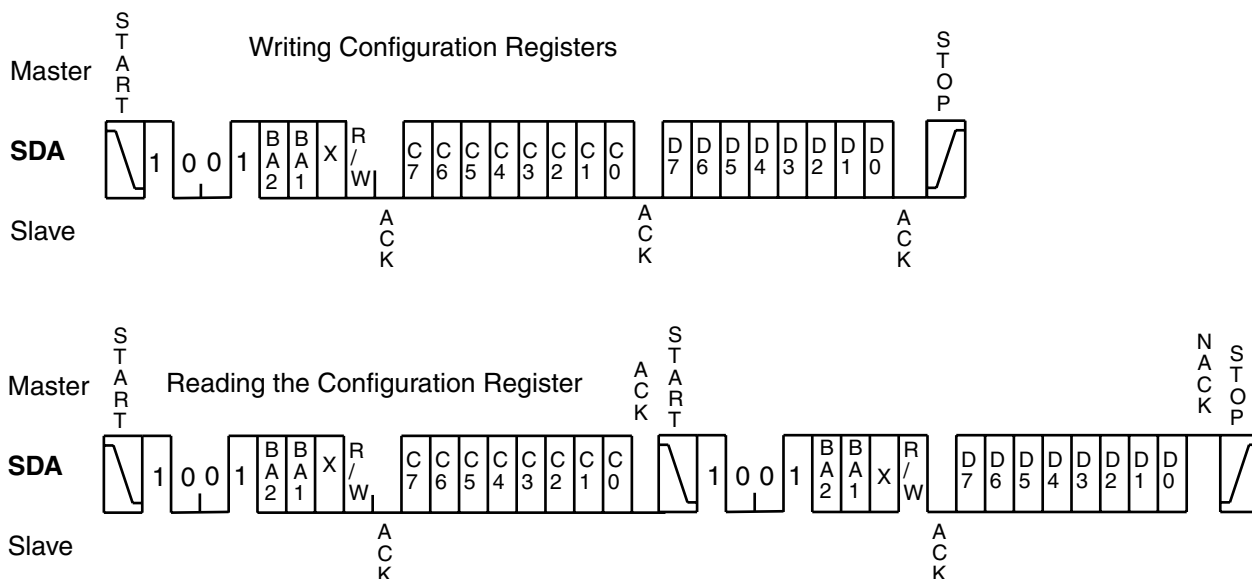
When the SMS48 is performing an internal Write operation it will ignore any new Start conditions. Since the device will only return an acknowledge after it accepts the Start the part can be continuously queried until an acknowledge is issued, indicating that the internal Write cycle is complete. See the flow chart for the proper sequence of operations for polling.

**I²C INTERFACE (CONTINUED)****READ OPERATIONS**

Read operations are initiated with the R/W bit of the identification field set to 1. There are two different Read options: 1. Current Address Byte Read, and 2. Random Address Byte Read.

Random Address Read

Random address Read operations allow the Master to access any register location in a random fashion. This operation involves a two-step process. First, the Master issues a write command which includes the start condition and the Slave address field (with the R/W bit set to Write), followed by the address of the word it is to Read. This procedure sets the internal address counter of the SMS48 to the desired address. After the word address acknowledge is received by the Master it immediately reissues a Start condition, followed by another Slave address field with the R/W bit set to READ. The SMS48 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master sets the SDA line to NACK and generates a Stop condition. The SMS48 discontinues data transmission and reverts to its standby power mode.

**Figure 10 - Write Flow Chart****Figure 9 - Read and Write Operations**



APPLICATIONS

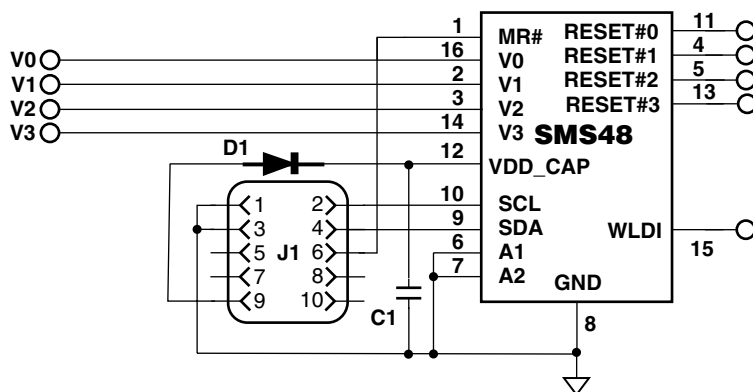


Figure 11 - Application Schematic

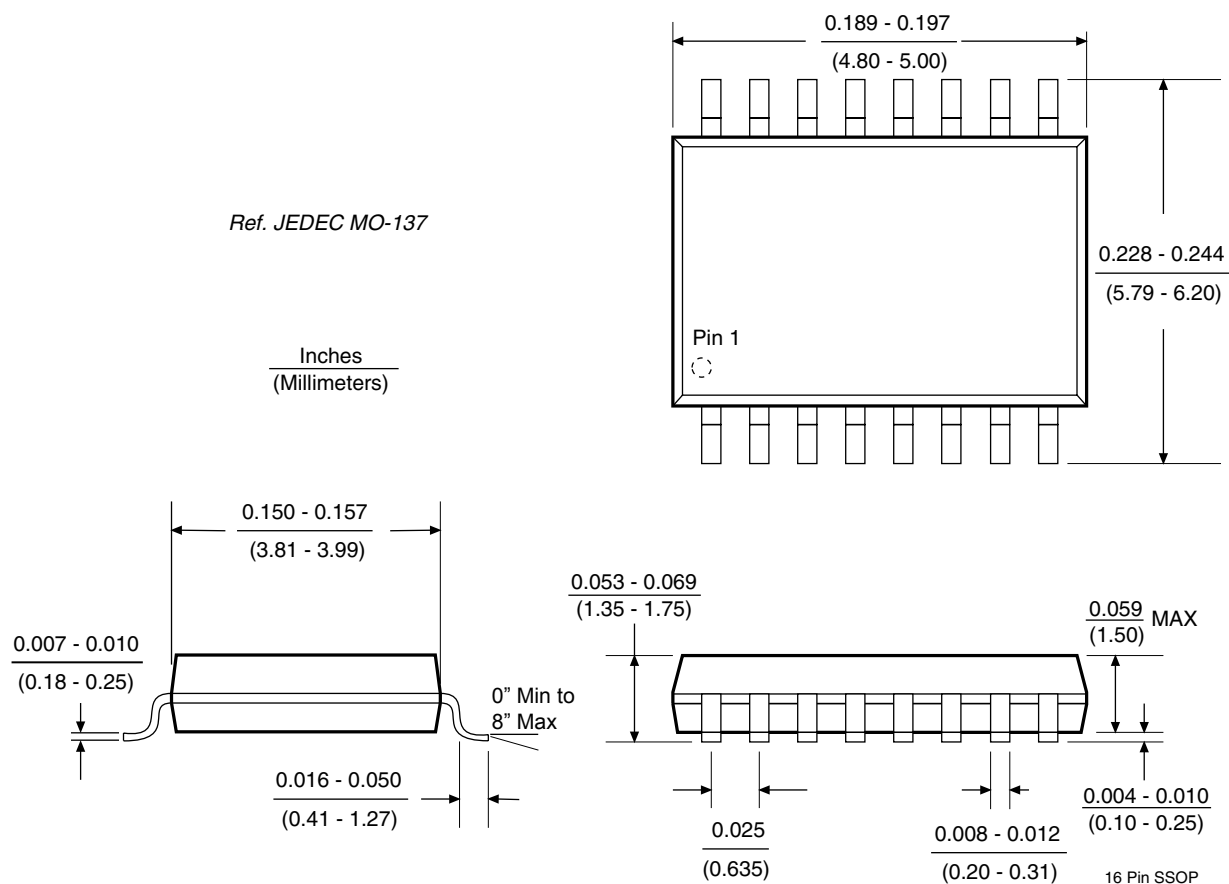
NOTES:

1. C1 is a 0.1µF.
2. Connector J1 is an SMX3200 (see Figure 6).
3. D1 is a 1N4148

**DEFAULT CONFIGURATION REGISTER SETTINGS - SMS48GC-370**

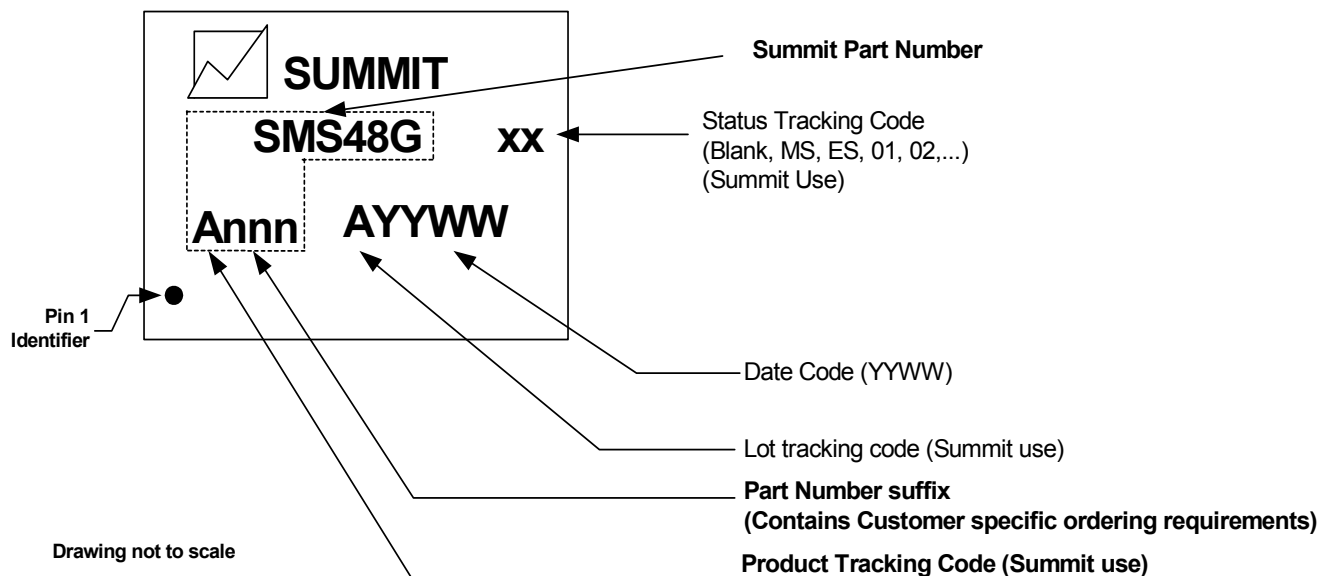
Register	Contents	Function
R00	56	V0 threshold set to 3.090V
R01	28	V1 threshold set to 2.400V
R02	A0	V2 threshold set to 1.400V
R03	14	V3 threshold set to 0.700V
R04	F3	Reset Trigger source set for all channels, V0, V1 set to high range and V2, V3 set to low range
R05	X0	Upper bits are volatile status indication of input supply condition. V0, V1, V2 and V3 set to monitor UV Under Voltage.
R06	C5	Reset timeout set to 100ms, Watchdog Timer set to 1.6s. Bits D4 and D3 indicate revision control.
R07	40	Configuration registers are unlocked.

The default device ordering number is SMS48GC-370, is programmed as described above and tested over the commercial temperature range.

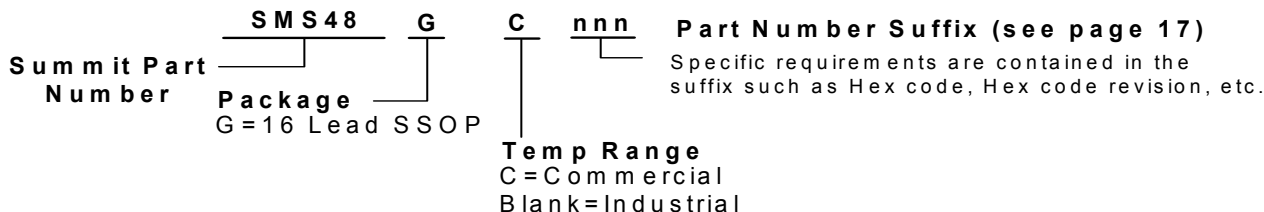
PACKAGE**16 PIN SSOP PACKAGE**



PART MARKING



ORDERING INFORMATION



NOTICE

NOTE 1 - This is a **Preliminary Information** data sheet that describes a Summit product currently in pre-production with limited characterization.

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