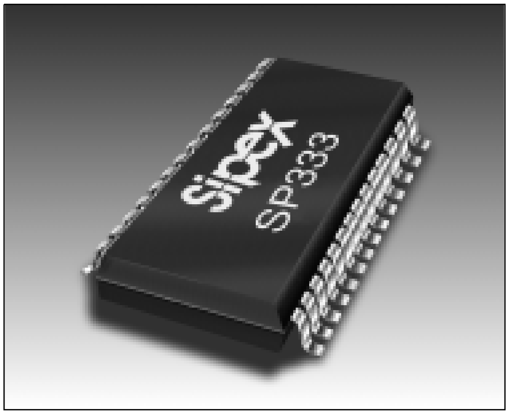
Sipex

SP333

+5V Only RS-232/AppleTalk™ Programmable Transceiver

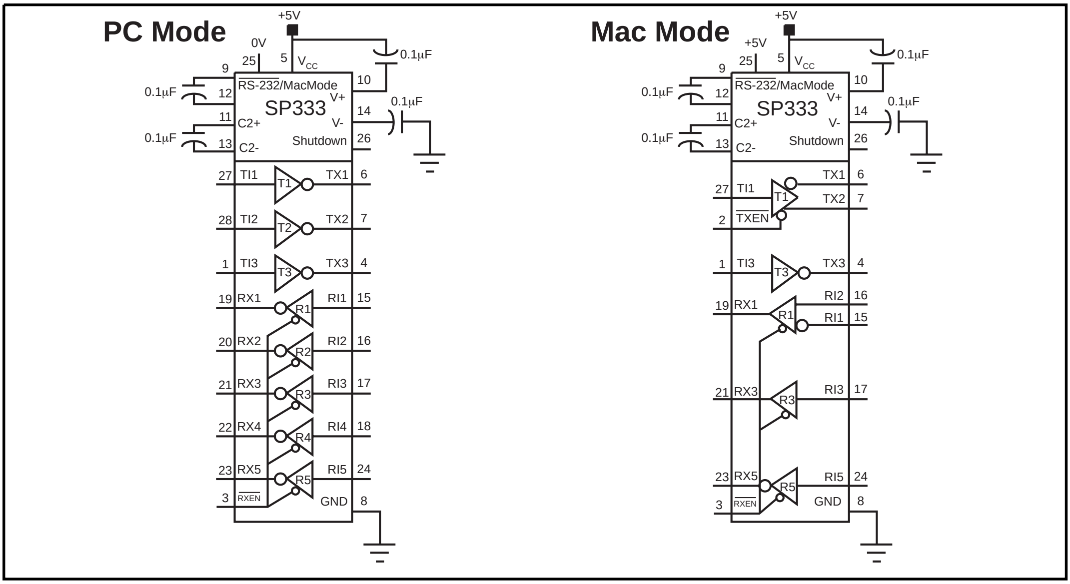
- +5V Only, Single Supply Operation
- Low Power Shutdown
- 28-Pin SOIC Packaging
- 3 Drivers, 5 Receivers – RS-232
- Complete AppleTalk™ Interface
- High Data Rates
  - 5Mbps Differential Transceivers
  - 460kbps Single-Ended Transceivers

Now Available in Lead Free Packaging



DESCRIPTION…

The SP333 is a monolithic device that supports both Macintosh™ and PC serial interfaces. RS-232 mode offers three (3) RS-232 drivers and five (5) RS-232 receivers. Mac mode includes a differential driver and a single-ended inverting driver. Receivers in Mac mode include one differential receiver, one non-inverting single-ended receiver and one inverting single-ended receiver. An on-chip charge pump allows +5V-only operation, and a low power Shutdown mode makes the SP333 ideal for battery powered applications. The interface mode can be changed at any time by a mode select pin.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}...+12V
Input Voltages
  Logic...-0.3V to (V_{CC}+0.5V)
  Drivers..-0.3V to (V_{CC}+0.5V)
  Receivers...±15V
Driver Outputs...±14V
Storage Temperature..-65˚C to +150˚C
Power Dissipation...1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
MAC Mode (pin 25 = +5V)					
Differential Driver					
High Level Output Voltage	+3.6			Volts	I_{OH} = 8mA
Low Level Output Voltage			-3.6	Volts	I_{OH} = –8mA
Differential Output, Load		±5V		Volts	R_L = 450Ω (TX outputs to GND)
Differential Output, No Load			±10	Volts	R_L = ∞
Driver Short Circuit Current		±40	500	mA	–7V≤V_O≤+7V; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Output Leakage Current			±100	µA	–7V≤V_O≤+7V; $\overline{TxEN}$ = V_{CC}
Input High Voltage	2.0			Volts	Applies to differential driver inputs
Input Low Voltage			0.8	Volts	Applies to differential driver inputs
Input Current			±20	µA	V_{IN} = 0V to V_{CC}
Transition Time		30		ns	R_L = 450Ω, C_L = 50pF; Rise/Fall 10% – 90%
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate	5			Mbps	R_L = 450Ω, C_L = 50pF
Single-Ended Inverting Driver					
High Level Output Voltage	+3.6		+6.0	Volts	R_L = 450Ω to GND; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Low Level Output Voltage	–6.0		–3.6	Volts	R_L = 450Ω to GND; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Driver Open Circuit Voltage			±10	Volts	R_L = ∞
Driver Short Circuit Current		±40		mA	–7V≤V_O≤+7V; Infinite duration
Input High Voltage	2.0			Volts	Applies to single-ended driver inputs
Input Low Voltage			0.8	Volts	Applies to single-ended driver inputs
Input Current			±20	µA	V_{IN} = 0V to V_{CC}
Transition Time		30		ns	R_L = 450Ω, C_L = 50pF; Rise/Fall 10% – 90%
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate	5			Mbps	R_L = 450Ω, C_L = 50pF
Differential Receiver					
Differential Input Threshold	-0.2		+0.2	Volts	-7V≤V_{CM}≤+7V
Input Hysteresis		70		mV	V_{CM}=0V
Input Resistance	12			kΩ	-7V≤V_{CM}≤+7V
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Short Circuit Current			85	mA	0V≤V_{OUT}≤V_{CC}

SPECIFICATIONS (CONTINUED)

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Differential Receiver					
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate	5			Mbps	R_L = 450Ω, C_L = 50pF
Single-Ended Inverting Receiver					
Input Voltage Range	–15		+15	Volts	
Input Threshold Low	0.8	1.2		Volts	
Input Threshold High		1.7	3.0	Volts	
Hysteresis	200	500	1000	mV	
Input Impedance	3	5	7	kΩ	
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Propagation Delay					
t_{PHL}		100		ns	
t_{PLH}		100		ns	
Data Rate	5			Mbps	
Single-Ended Non-Inverting Receiver					
Input Voltage Range	–7		+7	Volts	
Input Threshold Low	-0.2			Volts	
Input Threshold High			+0.2	Volts	
Hysteresis		70		mV	
Input Impedance	12	15		kΩ	
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Propagation Delay					
t_{PHL}		100		ns	
t_{PLH}		100		ns	
Data Rate	5			Mbps	
PC Mode (pin 25 = GND)					
RS-232 Driver					
TTL Input Levels					
V_{IL}			0.8	Volts	Applies to transmitter inputs
V_{IH}	2.0			Volts	Applies to transmitter inputs
High Level Voltage Output	+5.0		+15.0	Volts	R_L = 3kΩ to Gnd
Low Level Voltage Output	-15.0		-5.0	Volts	R_L = 3kΩ to Gnd
Open Circuit Output			±15	Volts	R_L = ∞
Short Circuit Current			±100	mA	V_{OUT} = Gnd
Power Off Impedance	300			Ohms	V_{CC}=0V; V_{OUT}= ±2V
Slew Rate		60		V/µs	R_L=3kΩ, C_L=50pF; From +3V to -3V or -3V to +3V
Transition Time			1.56	µs	Rise/fall time, between +3V & –3V ; R_L=3kΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		1.5		µs	R_L=3kΩ, C_L=1000pF; From 1.5V of T_{IN} to 50% of V_{OUT}
t_{PLH}		1.3		µs	R_L=3kΩ, C_L=1000pF; From 1.5V of T_{IN} to 50% of V_{OUT}
Data Rate	460	600		kbps	R_L=3kΩ, C_L=1000pF
RS-232 Receiver					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{SINK} = 4mA
V_{OH}	2.4				I_{SOURCE} = -4mA
Receiver Input High Threshold		1.7	3.0	Volts	

SPECIFICATIONS (CONTINUED)

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 Receiver					
Low Threshold	0.8	1.2		Volts	
Input Voltage Range	-15		+15	Volts	
Input Impedance	3	5	7	kOhms	V_{IN}=±15V
Hysteresis	0.2	0.5	1.0	Volts	V_{CC}=+5V
Transmission Rate	10			Mbps	
Propagation Delay					
t_{PHL}		100	600	ns	From 50% of V_{IN} to 1.5V of R_{OUT}
t_{PLH}		100	600	ns	From 50% of V_{IN} to 1.5V of R_{OUT}
Data Rate	460	600		kbps	
POWER REQUIREMENTS					
No Load Supply Current		15	25	mA	No load; V_{CC}=5.0V; T_A=25˚C
Shutdown Supply Current			75	µA	T_A=25˚C, V_{CC}=5.0V
AC PARAMETERS					
Differential Mode					
t_{PZL}; Enable to Output low		200	1000	ns	C_L=100pF, Figures 2 & 4, S_2 closed
t_{PZH}; Enable to Output high		200	1000	ns	C_L=100pF, Figures 2 & 4, S_1 closed
t_{PLZ}; Disable from Output low		200	1000	ns	C_L=15pF, Figures 2 & 4, S_2 closed
t_{PHZ}; Disable from Output high		200	1000	ns	C_L=15pF, Figures 2 & 4, S_1 closed
Receiver Delay Time from Enable Mode to Tri-state Mode					
Single-Ended Mode					
t_{PZL}; Enable to Output low		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PZH}; Enable to Output high		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
t_{PLZ}; Disable from Output low		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PHZ}; Disable from Output high		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
Differential Mode					
t_{PZL}; Enable to Output low		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PZH}; Enable to Output high		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
t_{PLZ}; Disable from Output low		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PHZ}; Disable from Output high		200	1000	ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed

Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

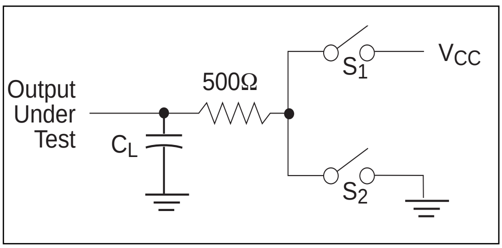


Figure 1. Driver Timing Test Load Circuit

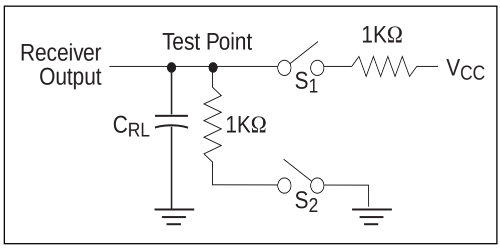


Figure 2. Receiver Timing Test Load Circuit

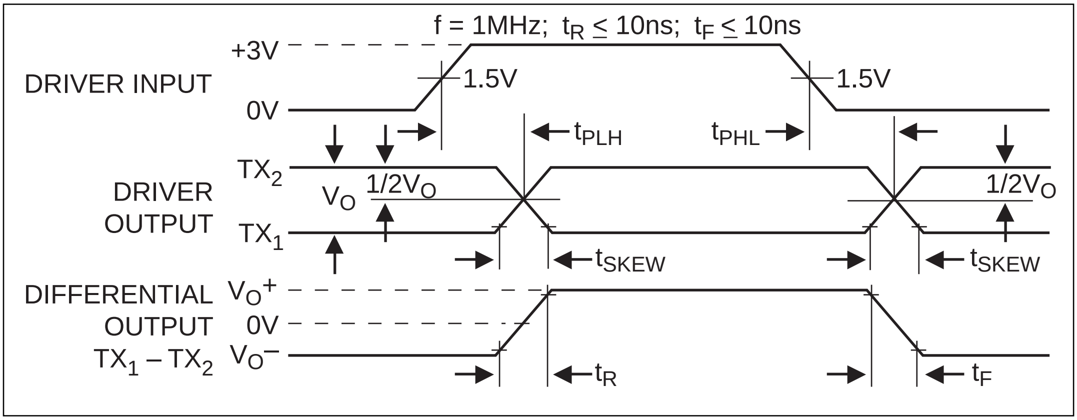


Figure 3. Driver Propagation Delays

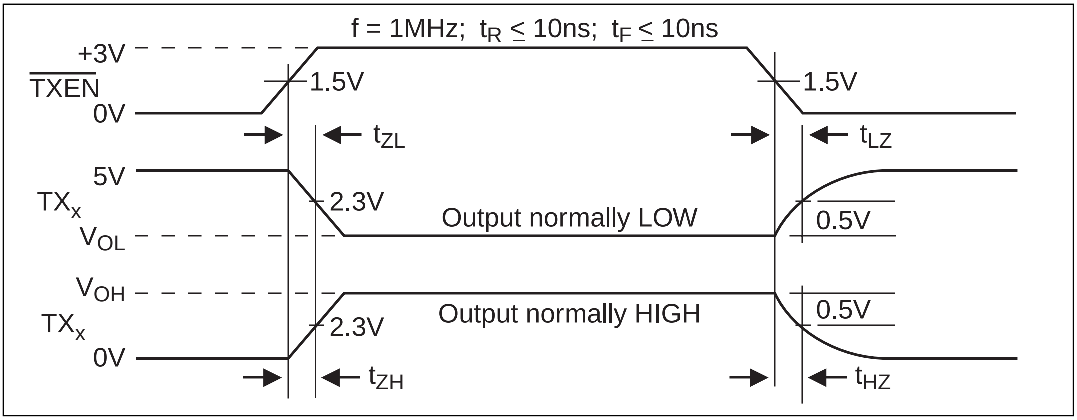


Figure 4. Driver Enable and Disable Times

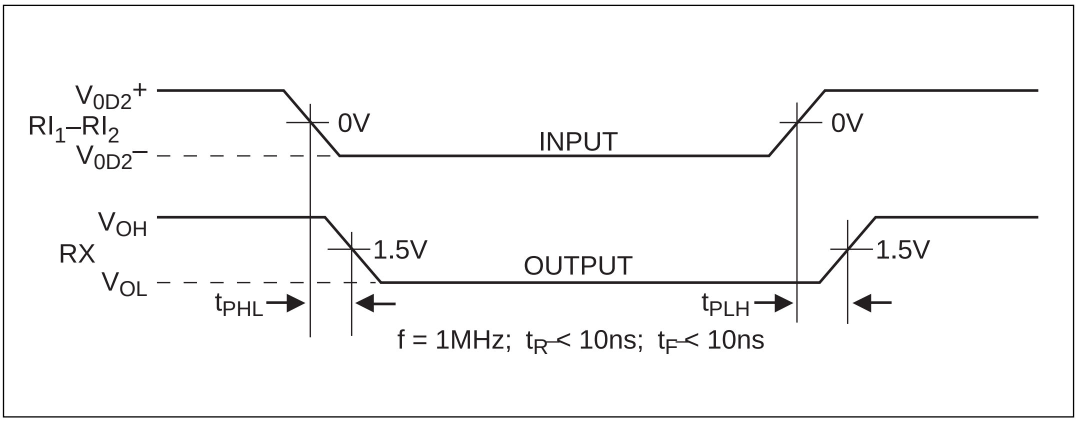


Figure 5. Receiver Propagation Delays

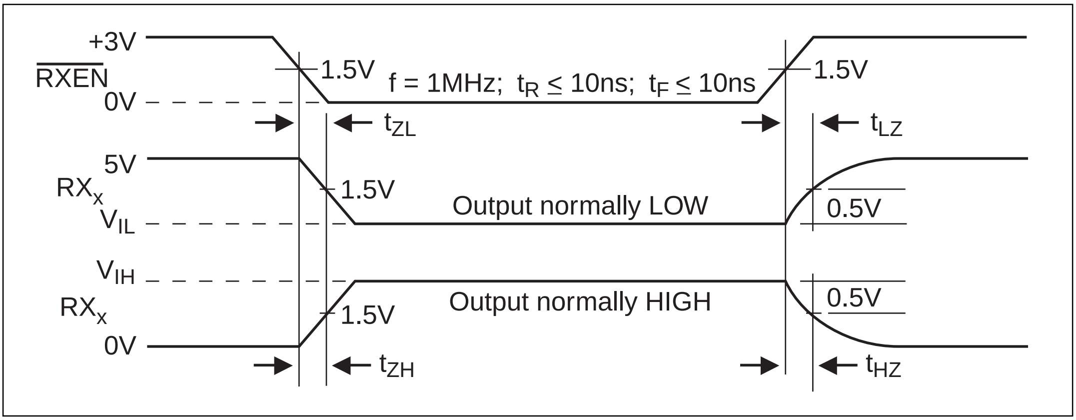


Figure 6. Receiver Enable and Disable Times

THEORY OF OPERATION...

The SP333 is a single chip device that can be configured via software for either RS-232 or AppleTalk™ interface modes at any time. The SP333 is made up of three basic circuit elements: single-ended drivers and receivers, differential drivers and receivers, and charge pump.

APPLETALK™ DRIVERS/RECEIVERS...

To program the SP333 for MacMode, Pin 25 should be connected to a logic HIGH. In MacMode, the SP333 offers a complete AppleTalk serial interface.

The driver section of the AppleTalk interface is made up of a differential driver and a single-ended inverting driver. The differential driver has voltage swings that are typically ±5V on each output pin under loaded conditions, and typically ±8V under no-load conditions. The differential driver can maintain ±3.6V (minimum) swings (per pin) under worst case load conditions of 450Ω between the differential output.

The differential driver is equipped with a tri-state control pin. When TXEN is a logic LOW, the differential driver is active. When the TXEN pin is a logic HIGH, the differential driver outputs are tri-stated. The TXEN pin only functions in MacMode. The differential AppleTalk driver can support data rates up to 5Mbps.

The single-ended AppleTalk driver also has typical voltage output swings of ±5V under loaded conditions, and ±8V under no-load conditions. The single-ended AppleTalk driver can maintain ±3.6V (minimum) swings under worst case conditions of 450Ω to ground. The single-ended AppleTalk driver can support data rates up to 5Mbps.

The receiver section of the SP333 is made up of a differential receiver, a single-ended non-inverting receiver , and a single-ended inverting receiver. The differential receiver has an input sensitivity of ±200mV over a common mode range of ±7V. The receivers have a typical input resistance of 15kΩ (12kΩ minimum). The differential receiver can receive data up to 5Mbps.

The single-ended non-inverting receiver has a ±200mV input threshold, however, the input voltage can vary between ±7V. The typical input resistance of the single-ended non-inverting receiver is 15kΩ (12kΩ minimum). The single-ended non-inverting receiver can also receive data up to 5Mbps.

The SP333 also has a single-ended inverting receiver input. This receiver is basically an RS-232 receiver (R5 receiver) and is typically used as a GPI (General Purpose Input) in the AppleTalk interface. The GPI input has TTL-compatible input thresholds that can receive signals up to ±15V. The input resistance of the single-ended inverting receiver is typically 5kΩ (3kΩ to 7kΩ). The GPI receiver can operate up to 5Mbps.

SINGLE ENDED DRIVERS/RECEIVERS...

RS-232 (V.28) Drivers...

The single-ended drivers and receivers comply the with the RS-232E and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ±9V with no load and is guaranteed to be greater than ±5V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3kΩ and 2500pF, the four RS-232 drivers can still maintain ±5V output levels. The drivers can operate over 400kbps; the propagation delay from input to output is typically 1.5µs. During shutdown, the driver outputs will be put into a high impedance tri-state mode.

RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy tranmission lines. The inputs also have a 5kΩ resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic HIGH state. The input resistance will maintain 3kΩ-7kΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to ±15V levels; this should not affect operation at ±30Volts. The RS-232 receivers can operate over 400kbps.

CHARGE PUMP...

The charge pump is a Sipex-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. The capacitor values of the SP333 can be as low as 0.1µF. *Figure 11a* shows the waveform found on the positive side of capacitor C2, and *Figure 11b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

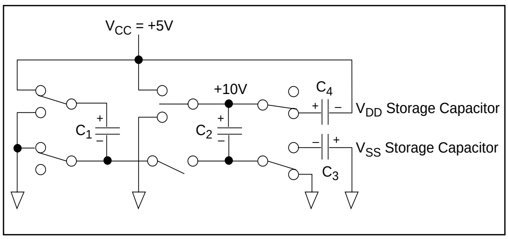


Figure 7. Charge Pump Phase 1

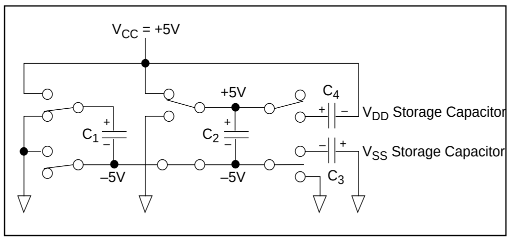


Figure 8. Charge Pump Phase 2

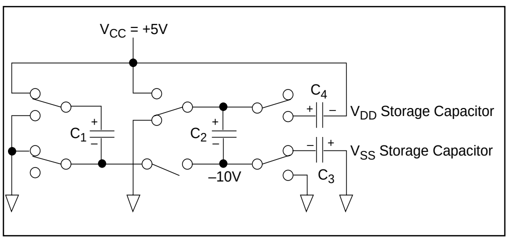


Figure 9. Charge Pump Phase 3

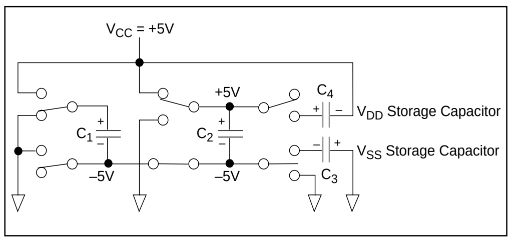


Figure 10. Charge Pump Phase 4

Phase 1

-Vss charge storage- During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

Phase 2

-Vss transfer- Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

Phase 4

-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4, the Vdd storage capacitor. Simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors should be 0.1µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V- pins. The value of the external supply voltages must be no greater than ±10V. The current drain from the ±10V supplies is used for the RS-232 drivers. For the RS-232 driver, the current requirement is 3.5mA per driver. The external power supplies should provide a power supply sequence of either: +10V, –10V, and then +5V; or –10V, +10V, and then +5V. It is critical that the ±10V supplies are on before V_{CC}.

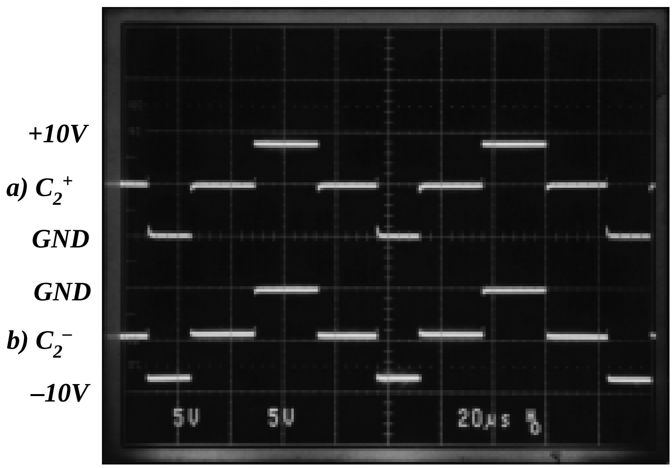


Figure 11. Charge Pump Waveforms

Shutdown Mode

The **SP333** can be put into a low power shutdown mode by connecting the Shutdown pin (SD, Pin 26) to a logic HIGH. During Shutdown, the driver outputs are put into a high impedance tri-state, and the charge pump is put into stand-by mode. The supply current drops to less than 10μA during shutdown and can be activated in either RS-232 or AppleTalk mode. For normal operation, the SD pin should be connected to a logic LOW.

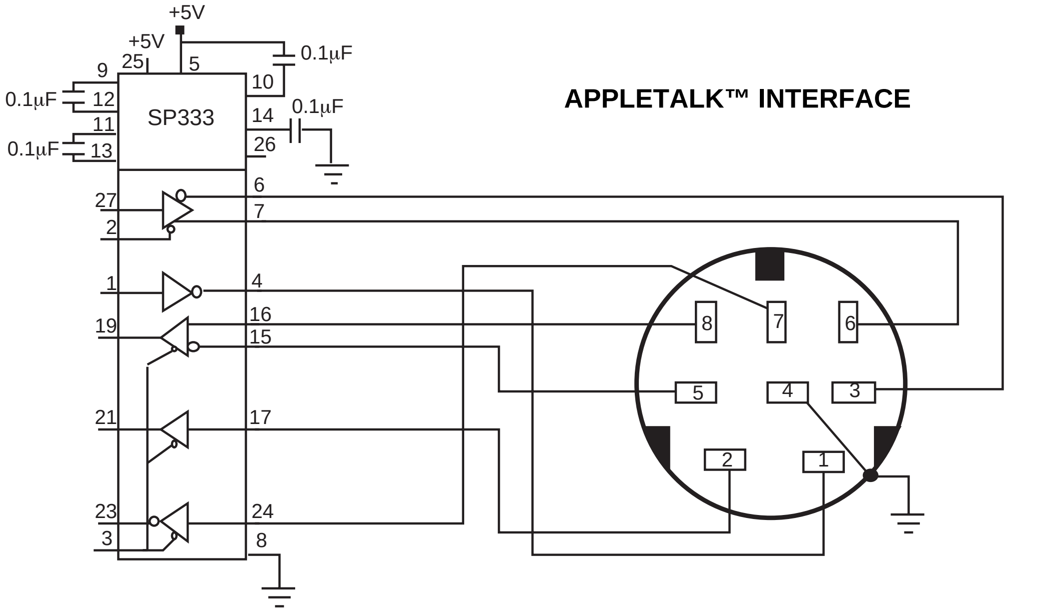
Receiver Enable

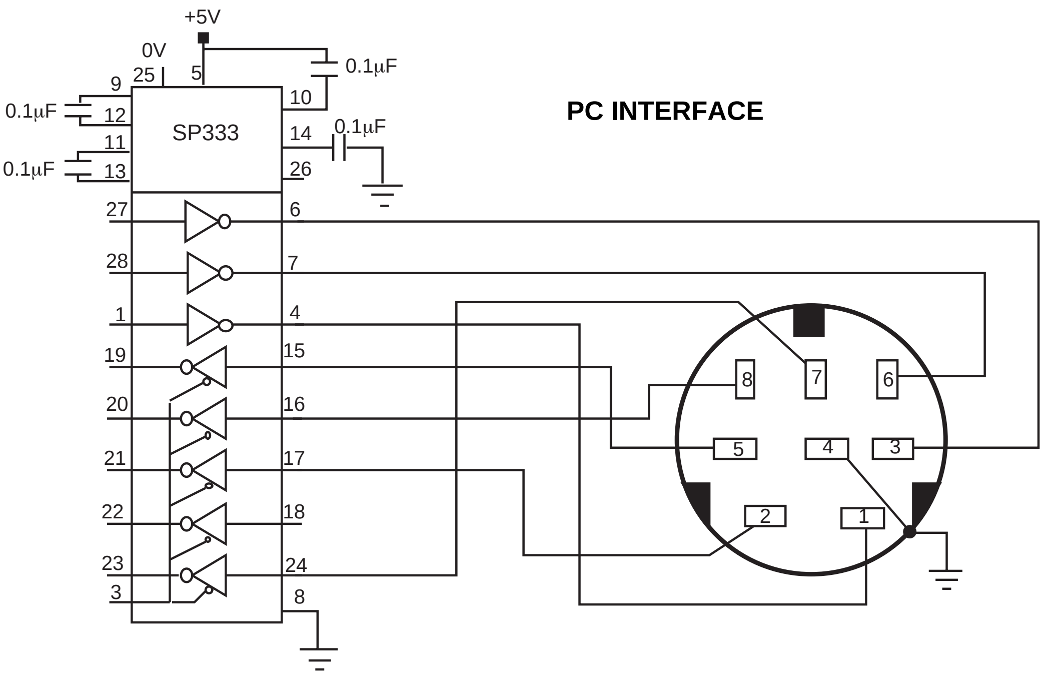
The **SP333** has a control line to enable or disable the receiver outputs. Pin 3 ($\overline{\text{RXEN}}$) is active LOW; a logic LOW on Pin 3 will enable the receiver outputs. A logic HIGH on Pin 3 will disable the receiver outputs. The receiver enable function can be initiated in either RS-232 or AppleTalk mode.

Wake-Up

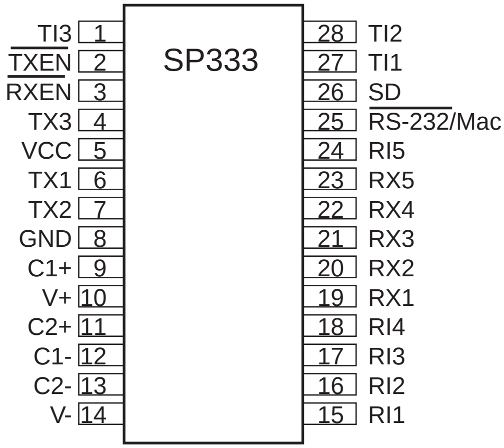
The **SP333** also features a "wake-up" function. The wake up function allows the RS-232 receivers to remain active during Shutdown mode unless they are disabled by the Receiver Enable control pin (Pin 3). The wake-up feature allows users to take advantage of the low power Shutdown mode and keep the receivers active to accept an incoming "ring indicator" signal.

SP333 Typical Application for AppleTalk™ and RS-232



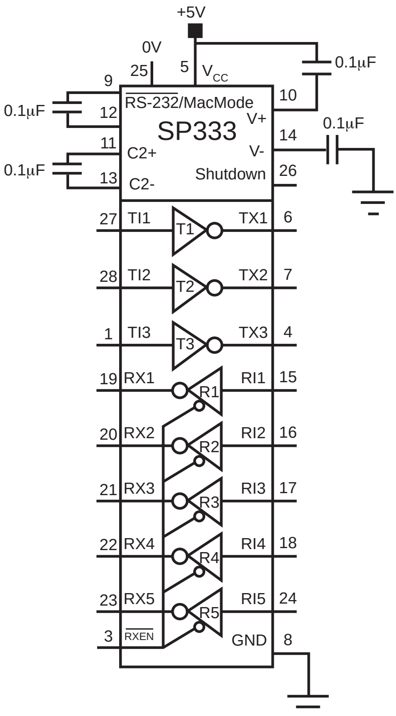


SP333 PIN CONFIGURATION

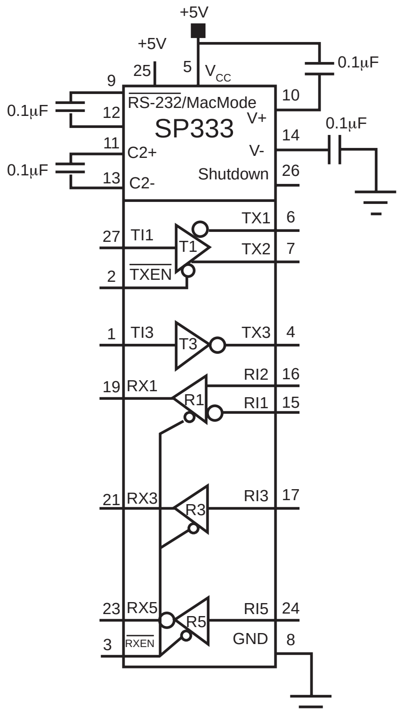


SP333 TYPICAL OPERATING CIRCUIT

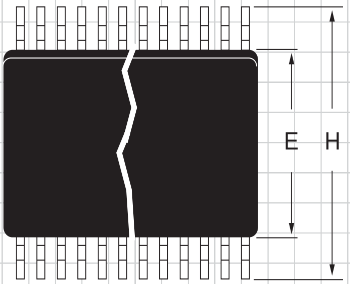
PC Mode (RS-232)

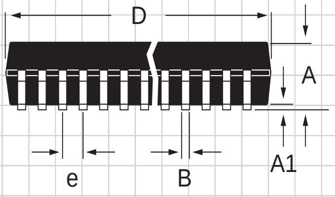


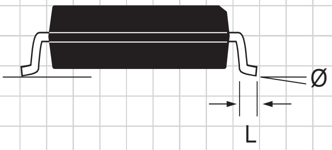
Mac Mode (AppleTalk)



PACKAGE: PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP333CT	0˚C to +70˚C	28-Pin SOIC
SP333ET	-40˚C to +85˚C	28-Pin SOIC

Available in lead free packaging. To order, add "-L" suffix to the part number.
Example: SP33CT= standard. SP333CT-L = lead free.

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and
Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600