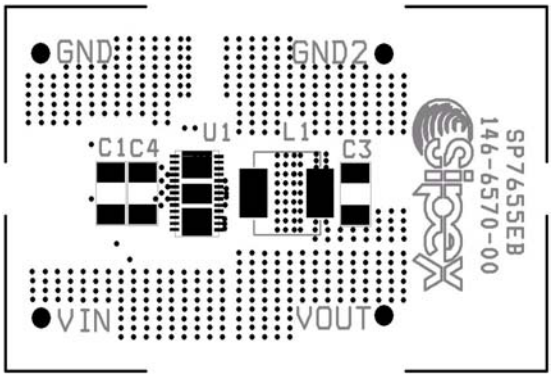
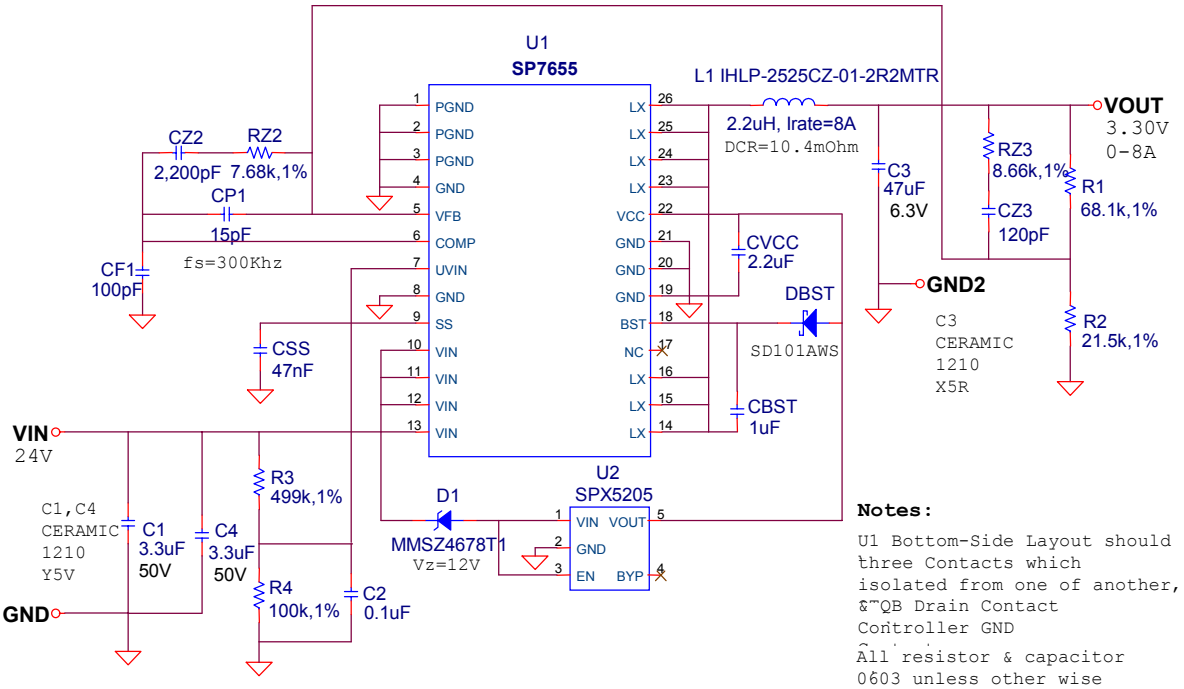
SP7655
Evaluation Board Manual

- Easy Evaluation for the SP7655ER 24V Input, 0 to 8A Output Synchronous Buck Converter
- Built in Low Rds(on) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 85%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown



SP7655EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP7655EB Circuit

Connect the SP7655 Evaluation Board with an external +24V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

VOUT ripple can best be seen touching probe tip to the pad for C3 and scope GND collar touching GND side of C3 using short wrapped wire around collar – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7655 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7655 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$Vout = 0.80V (R1 / R2 + 1) \Rightarrow R2 = R1 / [(Vout / 0.80V) – 1]$

Where $R1 = 68.1K\Omega$ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP7655 Evaluation Board design was optimized for 24V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7655ER provides short circuit protection by sensing Vout at GND.

POWER SUPPLY DATA

The SP7655ER is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7655 Evaluation Board Efficiency plot, with efficiencies to 85% (Including generation of 5V Vcc) and output currents to 8A. SP7655ER Load Regulation is shown in Figure 2 of only 1% change in output voltage from 0.5A load to 8A load. Figures 3 and 4 illustrate a 5A to 8A and 0A to 6A Load Step. Start-up Response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP7655ER is configured for hiccup mode in response to an output dead short circuit condition and will Softstart until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 135mV at no load to 8A load.

While data on individual power supply boards may vary, the capability of the SP7655ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

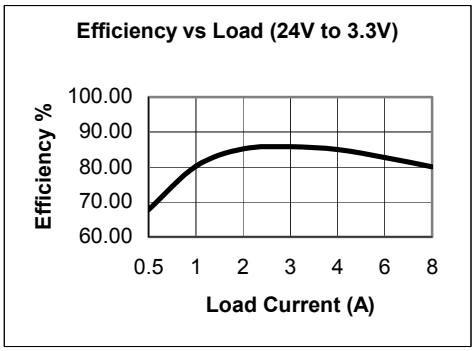


Figure 1. Efficiency vs Load

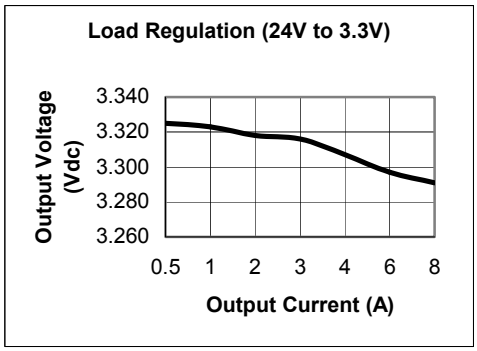


Figure 2. Load Regulation

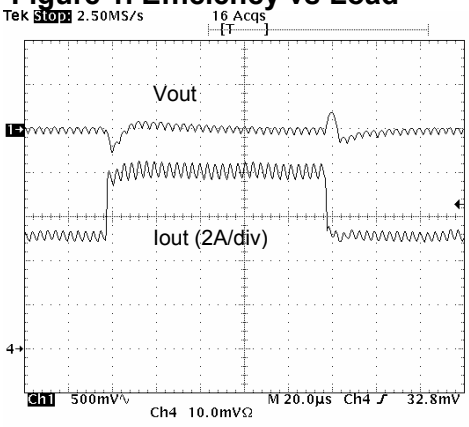


Figure 3. Load Step Response: 5->8A

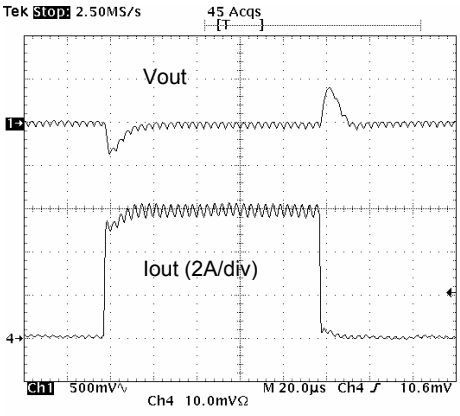


Figure 4. Load Step Response: 0->6A

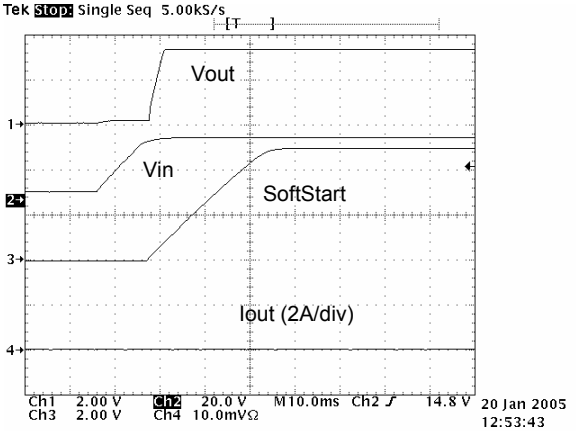


Figure 5. Start-Up Response: No Load

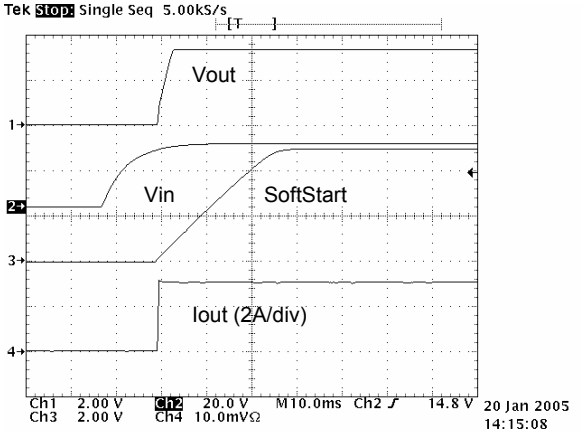


Figure 6. Start-Up Response: 3.0A Load

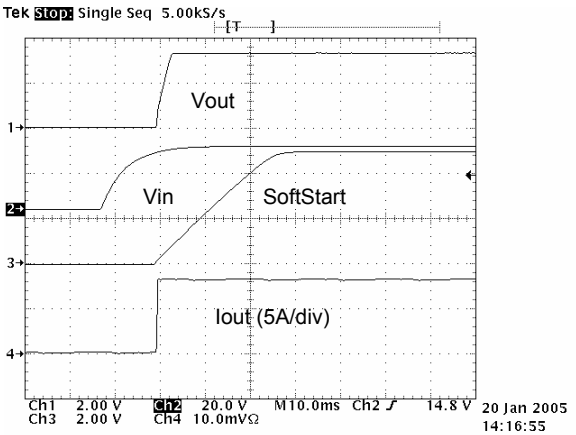


Figure 7. Start-Up Response: 8A Load

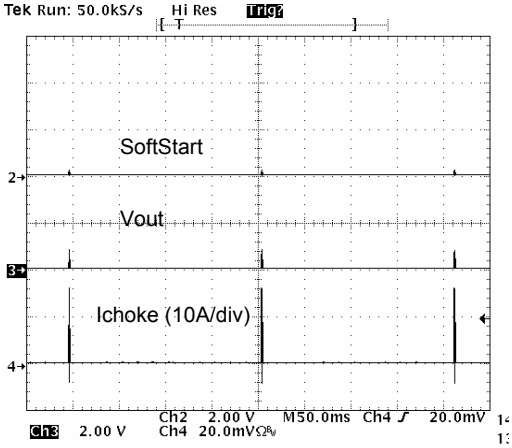


Figure 8. Output Load Short Circuit

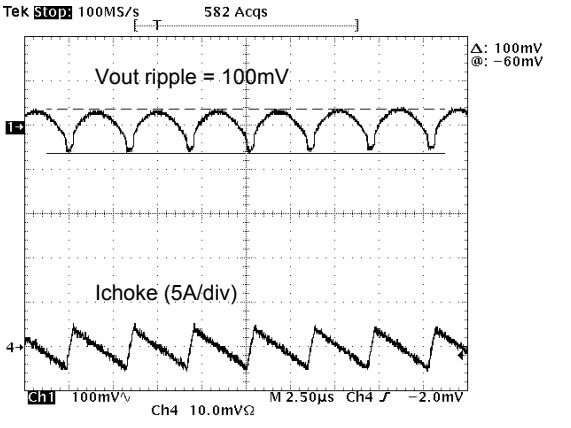


Figure 9. Output Ripple: No Load

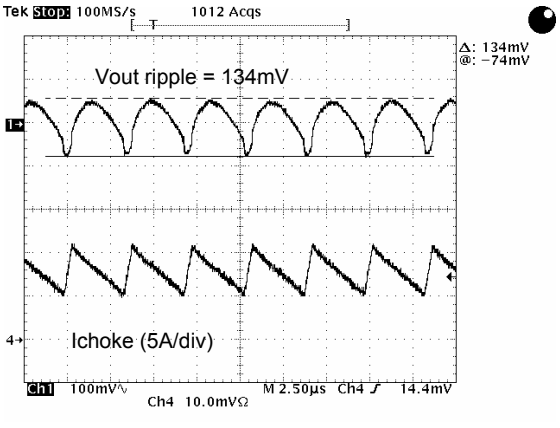
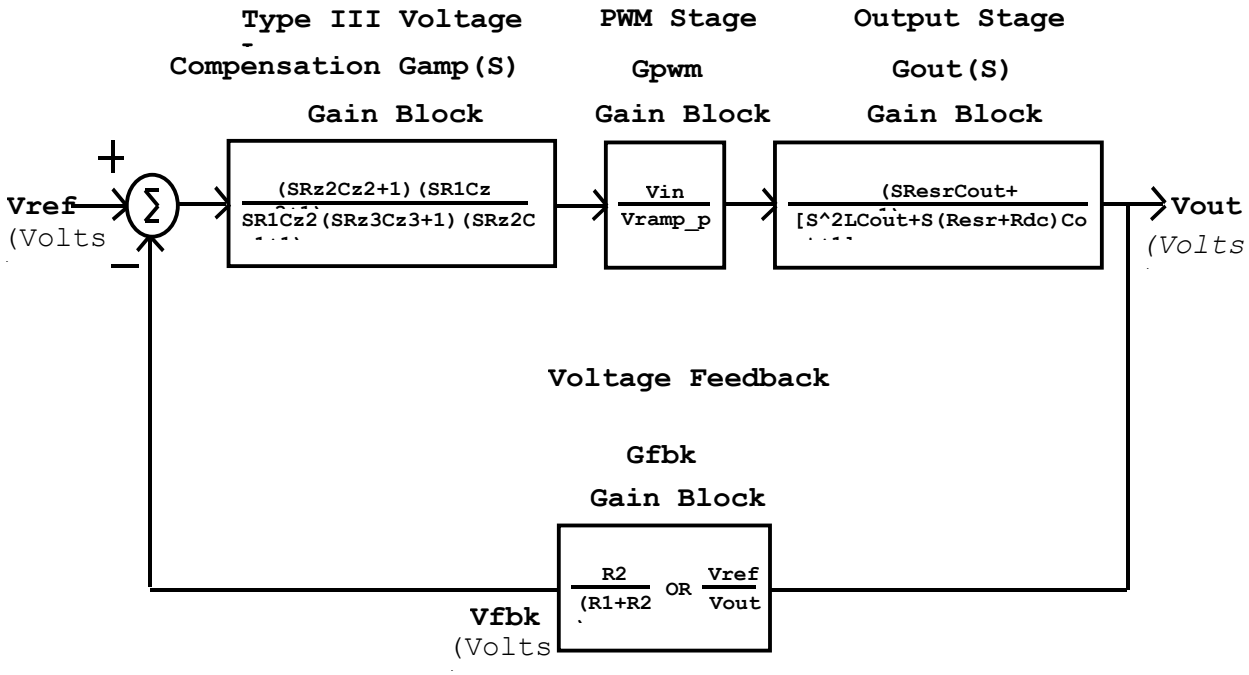


Figure 10. Output Ripple: 8A Load

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7655EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7655EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definition

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7655 Internal RAMP Amplitude Peak to Peak Voltage

Condition

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 11. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows:

a. Choose **fco** = fs / 5

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2 / R1** gain for the desired gain bandwidth
Rz2 = R1 (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP7655ER internal Error Amplify

APPLICATION CIRCUIT FOR 12V INPUT

Figure 12 shows another example of the SP7655ER configured for a common Bus Voltage conversion from +12V input to 3.3V output at 8A.

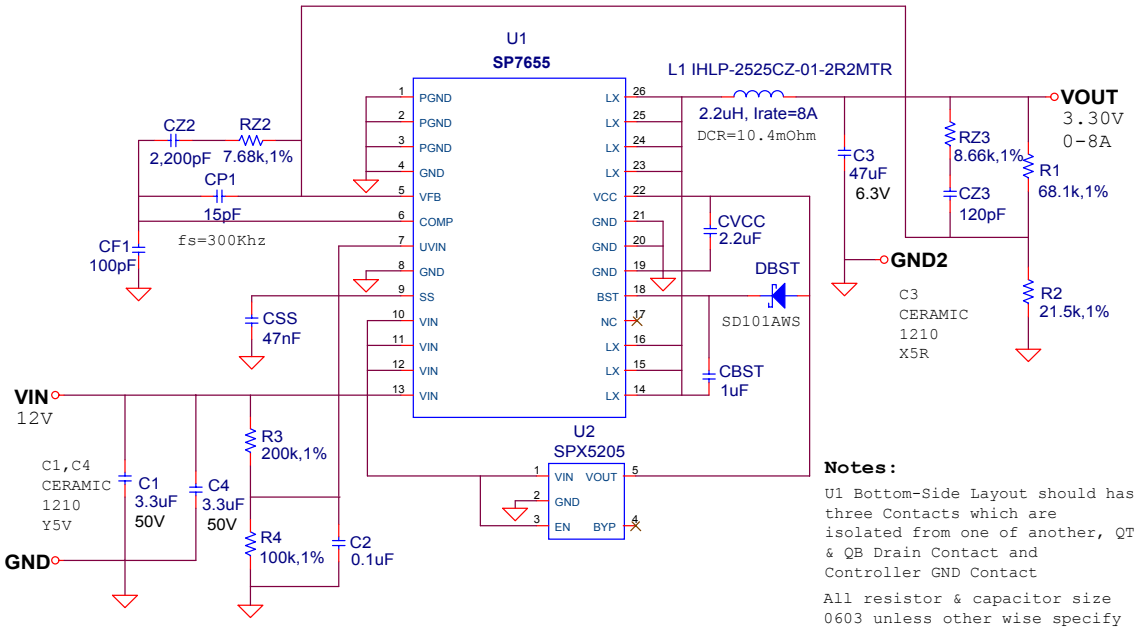


Figure 12. SP7655ER configured for Vin = 12V, Vout = 3.3V at 0-8A Output Load Current

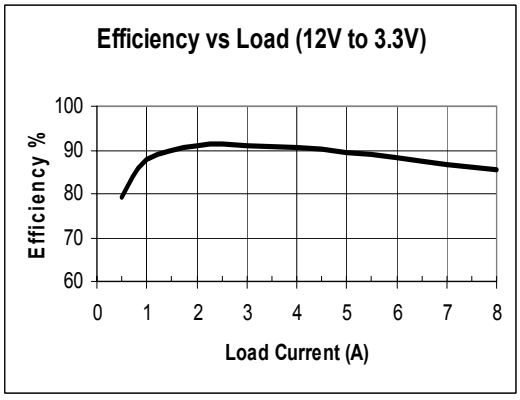


Figure 13. Efficiency vs Load

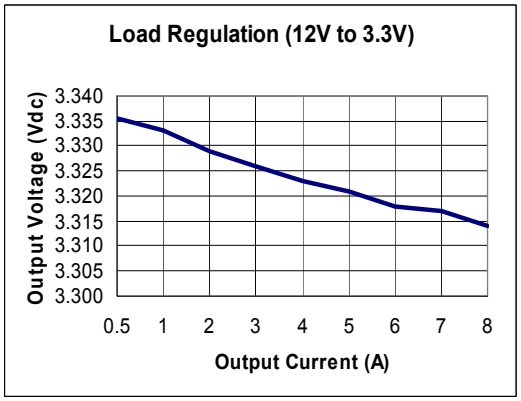


Figure 14. Load Regulation

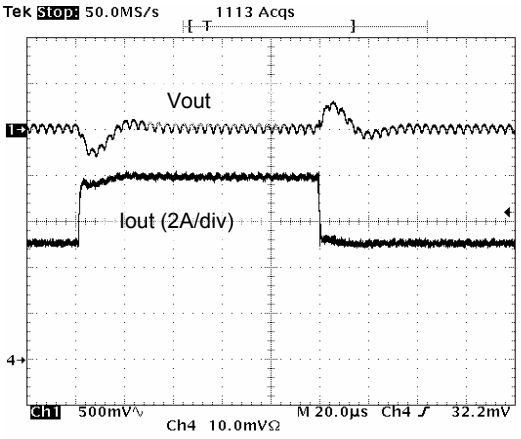


Figure 15. Load Step Response: 5-8A

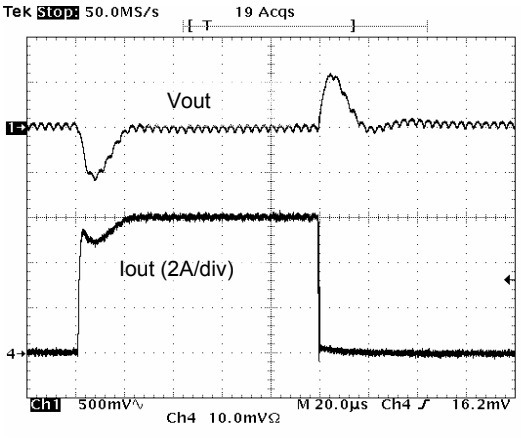


Figure 16. Load Step Response: 0-6A

PC LAYOUT DRAWINGS

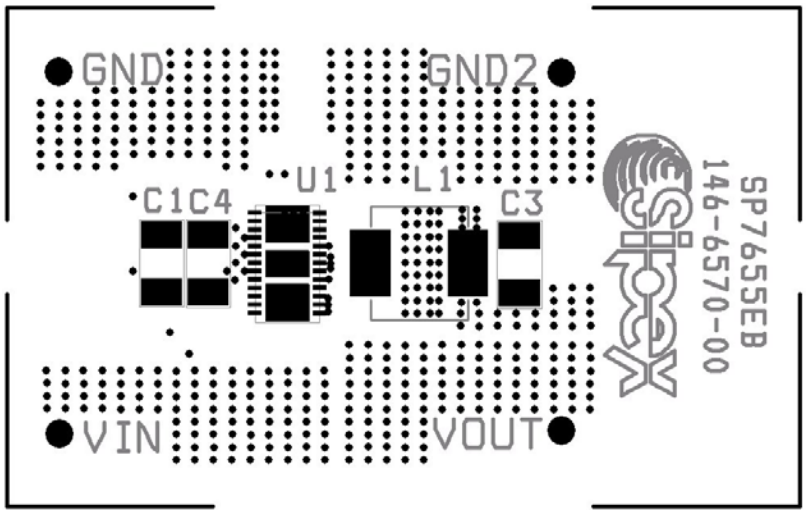


Figure 17. SP7655EB Component Placement

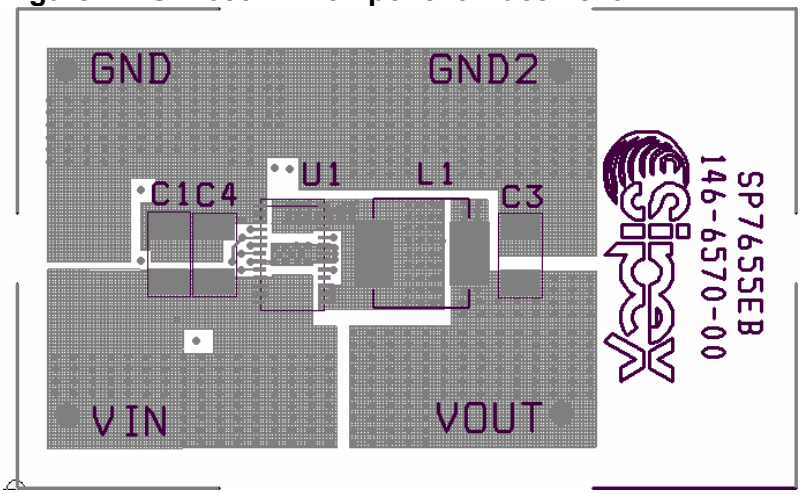


Figure 18. SP7655EB PC Layout Top Side

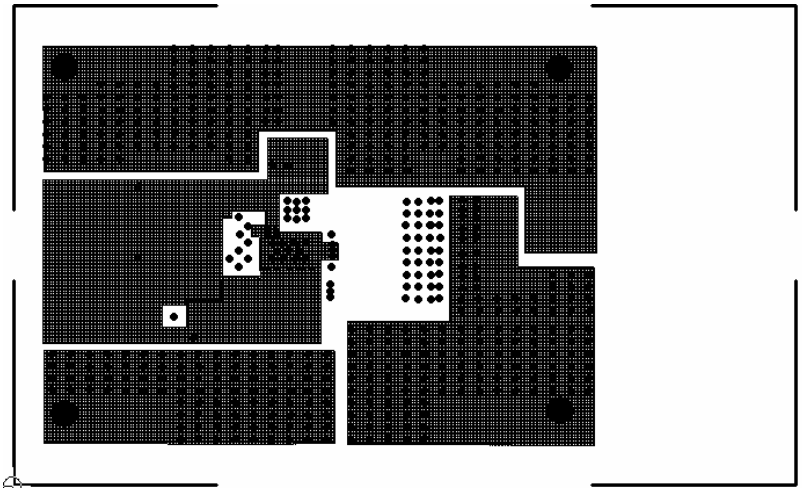


Figure 19. SP7655EB PC Layout 2nd Layer Side

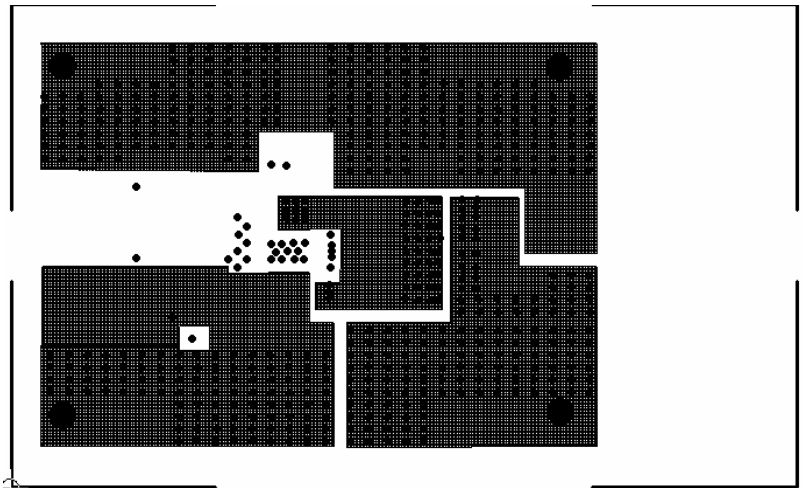


Figure 20. SP7655EB PC Layout 3rd Layer Side

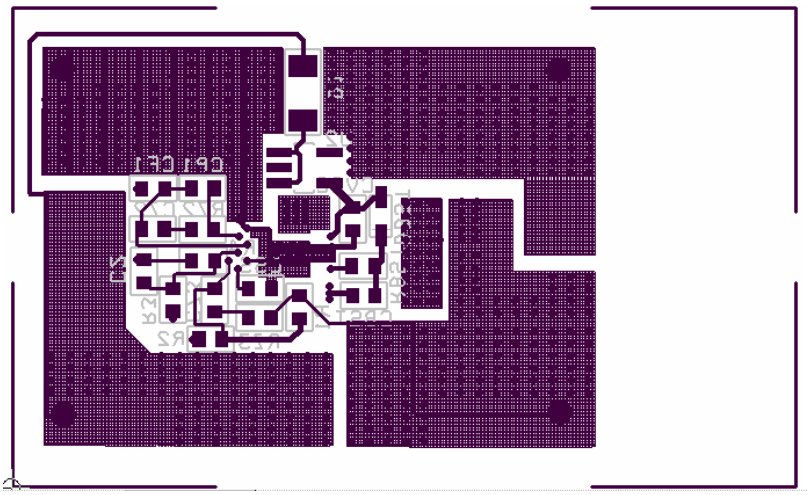


Figure 21. SP7655EB PC Layout Bottom Side

Table 1: SP7655EB List of Materials

SP7655 Vin=28V Evaluation Board Rev. 00 List of Materials							6/18/04
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
1	PCB	1	Sipex	F146-6570-00	1.75"X2.75"	SP7655EB	978-667-8700
2	U1	1	Sipex	SP7655EU	DFN-26	2-FETs Buck Ctrl	978-667-8700
3	U2	1	Sipex	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Reg	978-667-7800
4	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA Schottky Diode	402-563-6866
5	D1	1	ON Semi	MMSZ4678T1	SOD-123	12V, 500mW Zener Diode	800-344-4539
6	L1	1	Vishay	IHLP-2525CZ-01-2R2MTR	6.86x6.47mm	2.2uH Coil 8A 10.4mohm	914-347-2474
7	C3	1	TDK	C3225X5R0J476M	1210	47uF Ceramic X5R 6.3V	978-779-3111
8	C1,C4	2	TDK	C3225X7R1H335M	1210	3.3uF Ceramic X7R 50V	978-779-3111
9	CVCC	1	TDK	C1608X5R1A225K	0603	2.2uF Ceramic X5R 10V	978-779-3111
10	CBST	1	Murata	GRM188R61A105KA61D	0603	1.0uF Ceramic X5R 10V	978-779-3111
11	C2	1	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 50V	978-779-3111
12	CSS	1	Samsung	CL10B473KB8NNNC	0603	47,000pF Ceramic X7R 50V	978-779-3111
13	CP1	1	AVX	06035A150JAT2A	0603	15pF Ceramic COG 50V	978-779-3111
14	CZ2	1	TDK	C1608COG1H222J	0603	2,200pF Ceramic COG 50V	978-779-3111
15	CF1	1	ROHM	MCH185A101JK	0603	100pF Ceramic COG 50V	978-779-3111
16	CZ3	1	AVX	06035A121JAT2A	0603	120pF Ceramic COG 50V	978-779-3111
17	RZ2	1	ROHM	MCR03EZPFX7681	0603	7.68K Ohm Thick Film Res 1%	800-344-4539
18	R2	1	SEI Electronics	RMC-1/16W-21.5K-1%	0603	21.5K Ohm Thick Film Res 1%	800-344-4539
19	RZ3	1	Vishay	CRCW0603-8661FRT1	0603	8.66K Ohm Thick Film Res 1%	800-344-4539
20	R1	1	Vishay	CRCW0603-6812FRT1	0603	68.1K Ohm Thick Film Res 1%	800-344-4539
21	R3	1	Vishay	CRCW0603-4993FRT1	0603	499K Ohm Thick Film Res 1%	800-344-4539
22	RBST	1	ROHM	MCR03EZPEFX20R0	0603	20.0 Ohm Thick Film Res 1%	800-344-4539
23	R4	1	Vishay	CRCW0603-1003FRT1	0603	100K Ohm Thick Film Res 1%	800-344-4539
24	VIN, VOUT, GND, GND2	4		K24C/M	.042 Dia	Input/Output Terminal Posts	800-344-4539

Vector Electronic

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7655EB	-40°C to +85°C	SP7655 Evaluation Board
SP7655ER	-40°C to +85°C	26-pin DFN