

# DATA SHEET

## **SSTVF16857**

DDR PC1600-PC3200 14-bit  
SSTL\_2 registered driver with  
differential clock inputs

Product data

2003 Sep 19

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

## SSTVF16857

### FEATURES

- Stub-series terminated logic for 2.5 V  $V_{DDQ}$  (SSTL\_2)
- Optimized for PC 2700 DDR (Double Data Rate) SDRAM applications
- Suitable for PC1600/PC2100 DDR SDRAM applications
- Suitable for PC3200 applications when used at  $V_{DD} = 2.6$  V
- Inputs compatible with JESD8-9 SSTL\_2 specifications.
- Flow-through architecture optimizes PCB layout
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Full DDR300/333/400 solution @ 2.5V when used with PCKV857
- Available in TSSOP-48, TVSOP-48 and 56 ball VFBGA packages
- Superior VREF noise rejection

### DESCRIPTION

The SSTVF16857 is a 14-bit SSTL\_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V.  $V_{DDQ}$  must not exceed  $V_{CC}$ . Inputs are SSTL\_2 type with  $V_{REF}$  normally at  $0.5 \cdot V_{DDQ}$ . The outputs support class I which can be used for standard stub-series applications or capacitive loads. Master reset (RESET) asynchronously resets all registers to zero.

The SSTVF16857 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM or SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 166 MHz will have a burst rate of 333 MT/s (mega-transfers per second). The modules require between 23 and 27 registered control and address lines, so two 14-bit wide devices will be used on each module. The SSTVF16857 is intended to be used for SSTL\_2 input and output signals.

The device data inputs consist of differential receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

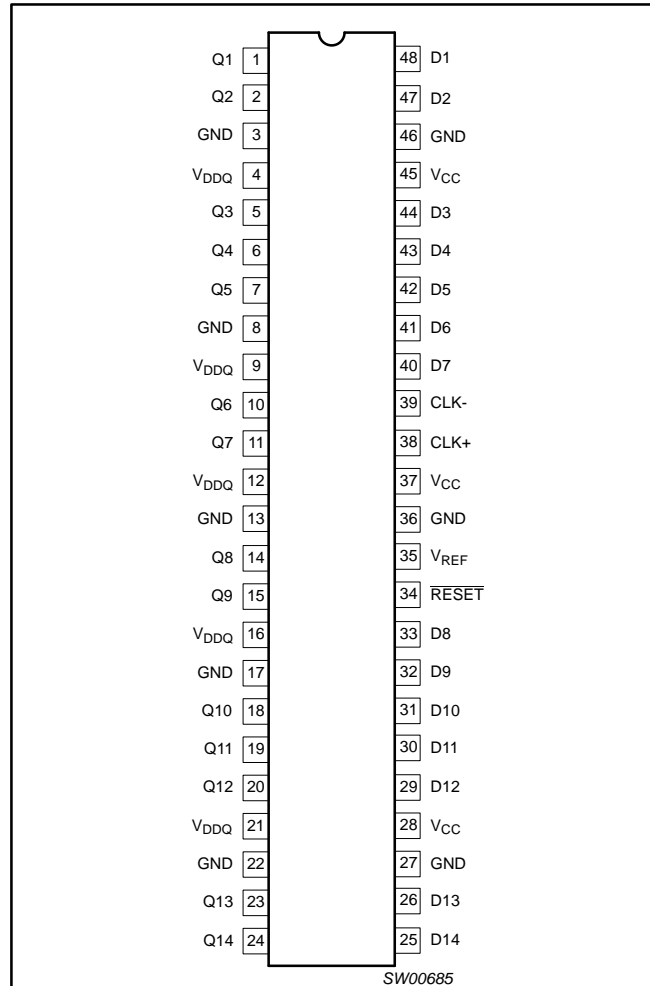
The clock input is fully differential to be compatible with DRAM devices that are installed on the DIMM. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CLK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device must support an asynchronous input pin (reset), which when held to the LOW state will assume that all registers are reset to the LOW state and all outputs drive a LOW signal as well.

### QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay; CLK to Qn	$C_L = 30$ pF; $V_{DDQ} = 2.5$ V	1.9	ns
$C_i$	Input capacitance	$V_{CC} = 2.5$ V	2.9	pF

### PIN CONFIGURATION



# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

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## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic TSSOP Type I	0 to +70 °C	SSTVF16857DGG	SOT362-1
48-Pin Plastic TSSOP (TVSOP)	0 to +70 °C	SSTVF16857DGV	SOT480-1
56-Ball Plastic VFBGA	0 to +70 °C	SSTVF16857EV	SOT702-1

## PIN DESCRIPTION

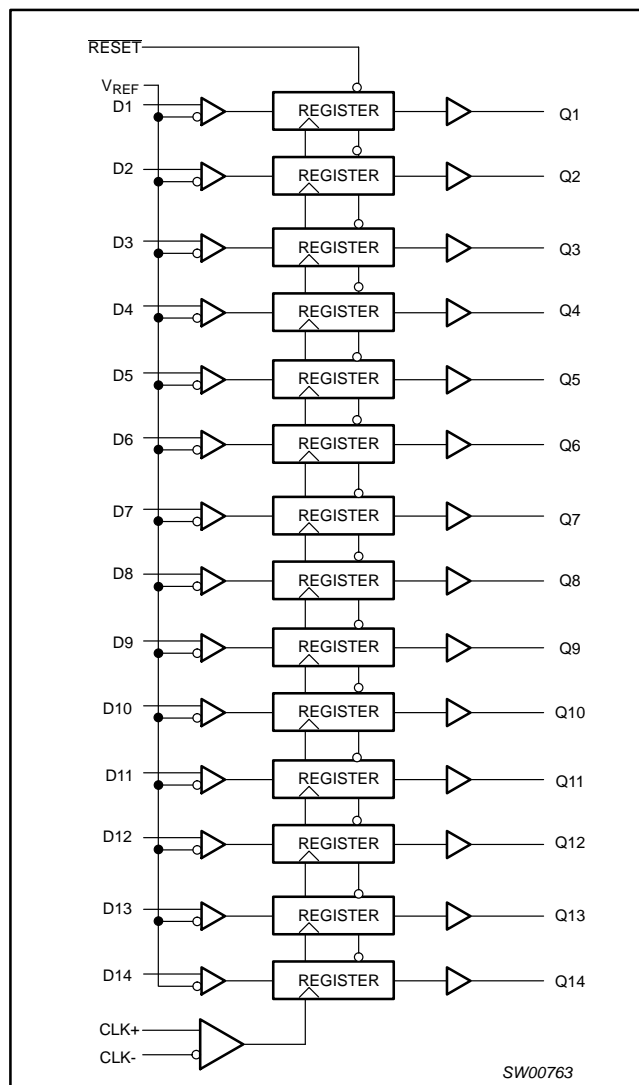
PIN NUMBER	SYMBOL	NAME AND FUNCTION
34	RESET	LVC MOS asynchronous master reset (Active LOW)
48, 47, 44, 43, 42, 41, 40, 33, 32, 31, 30, 29, 26, 25	D1 - D14	SSTL_2 data inputs
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q1 - Q14	SSTL_2 data outputs
35	V <sub>REF</sub>	SSTL_2 input reference level
3, 8, 13, 17, 22, 27, 36, 46	GND	Ground (0 V)
28, 37, 45	V <sub>CC</sub>	Positive supply voltage
4, 9, 12, 16, 21	V <sub>DDQ</sub>	Output supply voltage
38 39	CLK+ CLK-	Differential clock inputs

## FUNCTION TABLE

INPUTS				OUTPUT
RESET	CLK	CLK	D	Q
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	L or H	X	Q <sub>0</sub>

H = High voltage level  
 L = Low voltage level  
 ↓ = High-to-Low transition  
 ↑ = Low-to-High transition  
 X = Don't care

## LOGIC DIAGRAM



# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

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## BALL CONFIGURATION

	1	2	3	4	5	6
A	Q1	NC	NC	NC	NC	D1
B	GND	Q2	V <sub>CC</sub>	V <sub>CC</sub>	D2	GND
C	Q4	Q3	Q5	D5	D3	D4
D	V <sub>CC</sub>	GND	Q6	CLK-	D6	D7
E	V <sub>CC</sub>	Q7			CLK+	V <sub>CC</sub>
F	GND	Q8			V <sub>REF</sub>	GND
G	V <sub>CC</sub>	GND	Q9	RESET	D9	D8
H	Q11	Q12	Q10	D10	D12	D11
J	GND	Q13	V <sub>CC</sub>	V <sub>CC</sub>	D13	GND
K	Q14	NC	NC	NC	NC	D14

SW00952

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	—	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5	V <sub>DDQ</sub> + 0.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	—	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>		-0.5	V <sub>DDQ</sub> + 0.5	V
I <sub>OUT</sub>	DC output current	V <sub>O</sub> = 0 to V <sub>DDQ</sub>	—	±50	mA
	Continuous current <sup>4</sup>	V <sub>CC</sub> , V <sub>DDQ</sub> , or GND	—	±100	
T <sub>stg</sub>	Storage temperature range <sup>2</sup>		-65	+150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The continuous current at V<sub>CC</sub>, V<sub>DDQ</sub>, or GND should not exceed ±100 mA.

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

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## RECOMMENDED OPERATING CONDITIONS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	2.5	2.7	V
V <sub>DDQ</sub>	Output supply voltage		2.3	2.5	2.7	V
V <sub>REF</sub>	Reference voltage (V <sub>REF</sub> = 0.5 × V <sub>DDQ</sub> )	PC1600-PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.30	1.35	V
V <sub>TT</sub>	Termination voltage		V <sub>REF</sub> - 40 mV	V <sub>REF</sub>	V <sub>REF</sub> + 40 mV	V
V <sub>I</sub>	Input voltage		0	—	V <sub>CC</sub>	V
V <sub>IH</sub>	AC HIGH-level input voltage	All inputs	V <sub>REF</sub> + 310 mV	—	—	V
V <sub>IL</sub>	AC LOW-level input voltage	All inputs	—	—	V <sub>REF</sub> - 310 mV	V
V <sub>IH</sub>	DC HIGH-level input voltage	All inputs	V <sub>REF</sub> + 150 mV	—	V <sub>DDQ</sub> + 0.5 V	V
V <sub>IL</sub>	DC LOW-level input voltage	All inputs	V <sub>SS</sub> - 0.5 V	—	V <sub>REF</sub> - 150 mV	V
I <sub>OH</sub>	HIGH-level output current		—	—	-20	mA
I <sub>OL</sub>	LOW-level output current		—	—	20	mA
T <sub>amb</sub>	Operating free-air temperature range		0	—	70	°C

### NOTE:

- Unused control inputs must be held HIGH or LOW to prevent them from floating.

## DC ELECTRICAL CHARACTERISTICS—PC1600-PC2700

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = 0 to +70 °C				
			MIN	TYP <sup>2</sup>	MAX		
V <sub>IK</sub>	I/O supply voltage	V <sub>CC</sub> = 2.3 V; I <sub>I</sub> = -18 mA	—	—	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>OH</sub> = -100 μA V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -16 mA	V <sub>CC</sub> - 0.2	—	—		
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>OL</sub> = 100 μA	—	—	0.2	V	
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 16 mA	—	—	0.35		
V <sub>CMR</sub>	CLK, $\overline{\text{CLK}}$	Common mode range for reliable performance	0.97	—	1.53	V	
V <sub>PPmim</sub>	CLK, $\overline{\text{CLK}}$	Minimum peak-to-peak input to ensure logic state	—	—	360	mV	
I <sub>I</sub>	Data inputs, $\overline{\text{RESET}}$	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.15 V or 1.35 V	—	0.01	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V		—	0.01	±5	
	CLK, $\overline{\text{CLK}}$	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.15 V or 1.35 V	—	0.05	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V		—	0.05	±5	
V <sub>REF</sub>		V <sub>CC</sub> = 2.7 V	V <sub>REF</sub> = 1.15 V or 1.35 V	—	0.05	±5	μA
I <sub>CC</sub>	Quiescent supply current CLK and $\overline{\text{CLK}}$ in opposite state <sup>1</sup>	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	RESET = GND	—	0.5	10	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V	RESET = V <sub>CC</sub>	—	10	25	mA
C <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV, V <sub>CC</sub> = 2.5 V	V <sub>REF</sub> = 1.15 V or 1.35 V	2.5	2.9	3.4	pF
	CLK, $\overline{\text{CLK}}$	V <sub>ICR</sub> = 1.25 V, V <sub>I(PP)</sub> = 360 mV, V <sub>CC</sub> = 2.5 V	V <sub>REF</sub> = 1.15 V or 1.35 V	2.5	2.9	3.4	
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 2.5 V	V <sub>REF</sub> = 1.15 V or 1.35 V	2.5	2.9	3.4	

### NOTES:

- When CLK and  $\overline{\text{CLK}}$  are HIGH, typical I<sub>CC</sub> = 25 mA.
- All typical values are at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C (unless otherwise specified).

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

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## DC ELECTRICAL CHARACTERISTICS—PC3200

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = 0 to +70 °C				
			MIN	TYP <sup>2</sup>	MAX		
V <sub>IK</sub>	I/O supply voltage	V <sub>CC</sub> = 2.5 V; I <sub>I</sub> = -18 mA	—	—	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.5 V to 2.7 V; I <sub>OH</sub> = -100 μA V <sub>CC</sub> = 2.5 V; I <sub>OH</sub> = -16 mA	V <sub>CC</sub> - 0.2	—	—		
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.5 V to 2.7 V; I <sub>OL</sub> = 100 μA V <sub>CC</sub> = 2.5 V; I <sub>OL</sub> = 16 mA	—	—	0.2 0.35	V	
V <sub>CMR</sub>	CLK, $\overline{\text{CLK}}$	Common mode range for reliable performance	0.97	—	1.53	V	
V <sub>PPmin</sub>	CLK, $\overline{\text{CLK}}$	Minimum peak-to-peak input to ensure logic state	—	—	360	mV	
I <sub>I</sub>	Data inputs, $\overline{\text{RESET}}$	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.25 V or 1.35 V	—	0.01	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V		—	0.01	±5	
	CLK, $\overline{\text{CLK}}$	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.25 V or 1.35 V	—	0.05	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V		—	0.05	±5	
V <sub>REF</sub>	V <sub>CC</sub> = 2.7 V	V <sub>REF</sub> = 1.25 V or 1.35 V	—	0.05	±5	μA	
I <sub>CC</sub>	Quiescent supply current CLK and $\overline{\text{CLK}}$ in opposite state <sup>1</sup>	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	RESET = GND	—	0.5	10	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V	RESET = V <sub>CC</sub>	—	10	25	mA
C <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV, V <sub>CC</sub> = 2.6 V	V <sub>REF</sub> = 1.25 V or 1.35 V	2.5	2.9	3.4	pF
	CLK, $\overline{\text{CLK}}$	V <sub>I</sub> (CR) = 1.25 V, V <sub>I</sub> (PP) = 360 mV, V <sub>CC</sub> = 2.6 V	V <sub>REF</sub> = 1.25 V or 1.35 V	2.5	2.9	3.4	
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 2.6 V	V <sub>REF</sub> = 1.25 V or 1.35 V	2.5	2.9	3.4	

### NOTES:

- When CLK and  $\overline{\text{CLK}}$  are HIGH, typical I<sub>CC</sub> = 25 mA.
- All typical values are at V<sub>CC</sub> = 2.6 V and T<sub>amb</sub> = 25 °C (unless otherwise specified).

## TIMING REQUIREMENTS—PC1600-PC2700

Over recommended operating conditions; T<sub>amb</sub> = 0 to +70 °C (unless otherwise noted) (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			V <sub>CC</sub> = 2.5 V ±0.2 V		
			MIN	MAX	
f <sub>clock</sub>	Clock frequency		—	200	MHz
t <sub>w</sub>	Pulse duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW		1.0	—	ns
t <sub>su</sub>	Setup time	Data before CLK↑, $\overline{\text{CLK}}$ ↓	0.2	—	ns
		RESET HIGH before CLK↑, $\overline{\text{CLK}}$ ↓	0.8	—	
t <sub>h</sub>	Hold time		0.75	—	ns

## TIMING REQUIREMENTS—PC3200

Over recommended operating conditions; T<sub>amb</sub> = 0 to +70 °C (unless otherwise noted) (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			V <sub>CC</sub> = 2.5 V ±0.2 V		
			MIN	MAX	
f <sub>clock</sub>	Clock frequency		—	210	MHz
t <sub>w</sub>	Pulse duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW		1.0	—	ns
t <sub>su</sub>	Setup time	Data before CLK↑, $\overline{\text{CLK}}$ ↓	0.2	—	ns
		RESET HIGH before CLK↑, $\overline{\text{CLK}}$ ↓	0.8	—	
t <sub>h</sub>	Hold time		0.75	—	ns

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

SSTVF16857

## SWITCHING CHARACTERISTICS—PC1600-PC2700

Over recommended operating conditions;  $T_{amb} = 0$  to  $+70$  °C;  $V_{DDQ} = 2.3 - 2.7$  V and  $V_{DDQ}$  does not exceed  $V_{CC}$ .  
Class I,  $V_{REF} = V_{TT} = V_{DDQ} \times 0.5$  and  $C_L = 10$  pF (unless otherwise noted) (see Figure 1)

SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		
			MIN	MAX	
$f_{max}$	Maximum clock frequency		200	—	MHz
$t_{PLH}/t_{PHL}$	CLK and $\overline{\text{CLK}}$	Q	1.0	2.6	ns
$t_{PHL}$	RESET	Q	2.0	4.0	ns

## SWITCHING CHARACTERISTICS—PC3200

Over recommended operating conditions;  $T_{amb} = 0$  to  $+70$  °C;  $V_{DDQ} = 2.3 - 2.7$  V and  $V_{DDQ}$  does not exceed  $V_{CC}$ .  
Class I,  $V_{REF} = V_{TT} = V_{DDQ} \times 0.5$  and  $C_L = 10$  pF (unless otherwise noted) (see Figure 1)

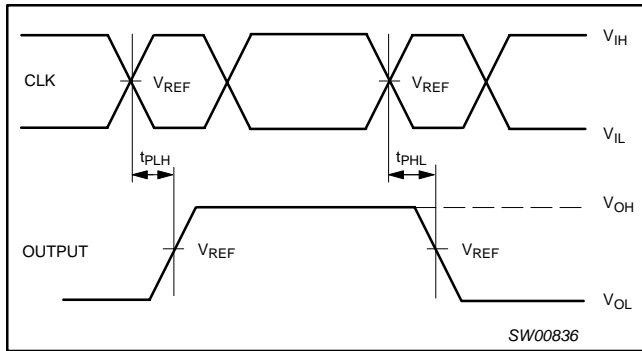
SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		
			MIN	MAX	
$f_{max}$	Maximum clock frequency		210	—	MHz
$t_{PLH}/t_{PHL}$	CLK and $\overline{\text{CLK}}$	Q	1.0	2.6	ns
$t_{PHL}$	RESET	Q	2.0	4.0	ns

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

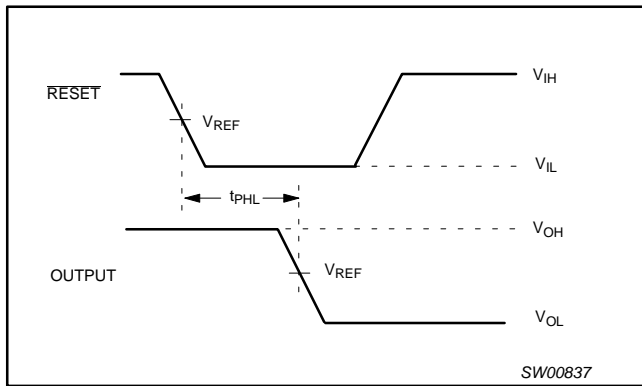
SSTVF16857

## PARAMETER MEASUREMENT INFORMATION

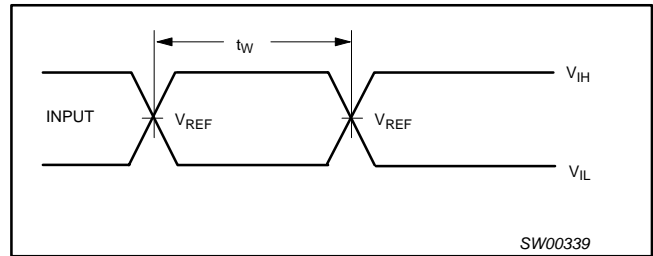
### AC WAVEFORMS



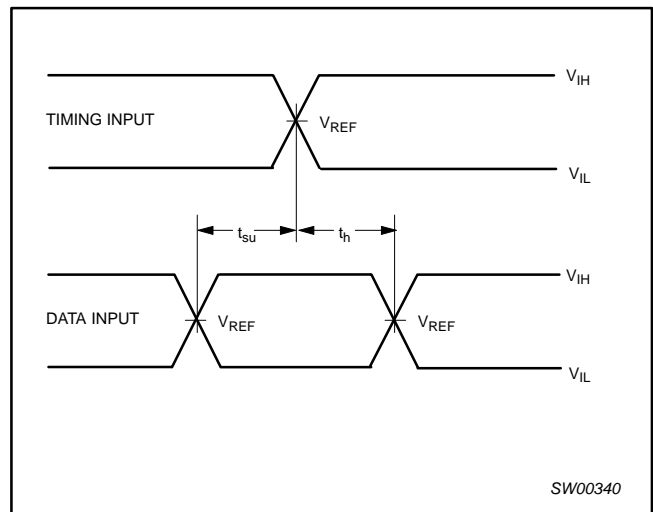
Waveform 1. Propagation delay times



Waveform 2. Propagation delay  $\overline{\text{RESET}}$  to output.



Waveform 3. Pulse duration



Waveform 4. Setup and hold times

### TEST CIRCUIT

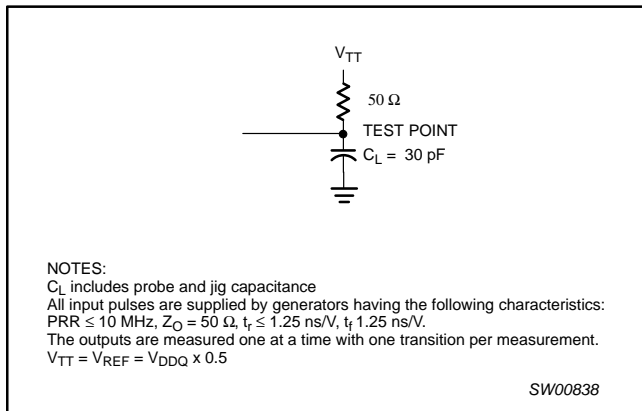


Figure 1. Load circuitry

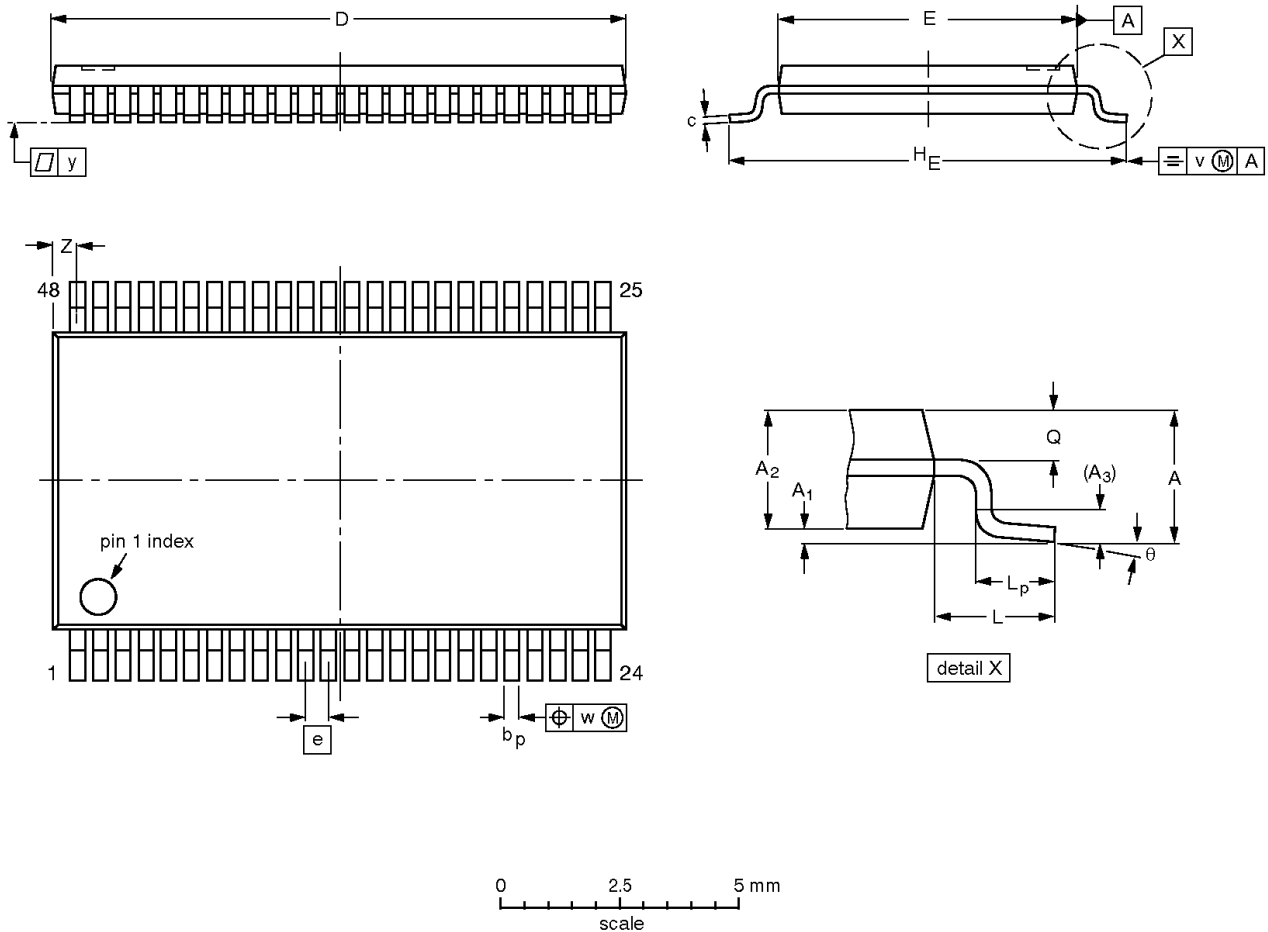


DDR PC1600-PC3200 14-bit SSTL\_2  
registered driver with differential clock inputs

SSTVF16857

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

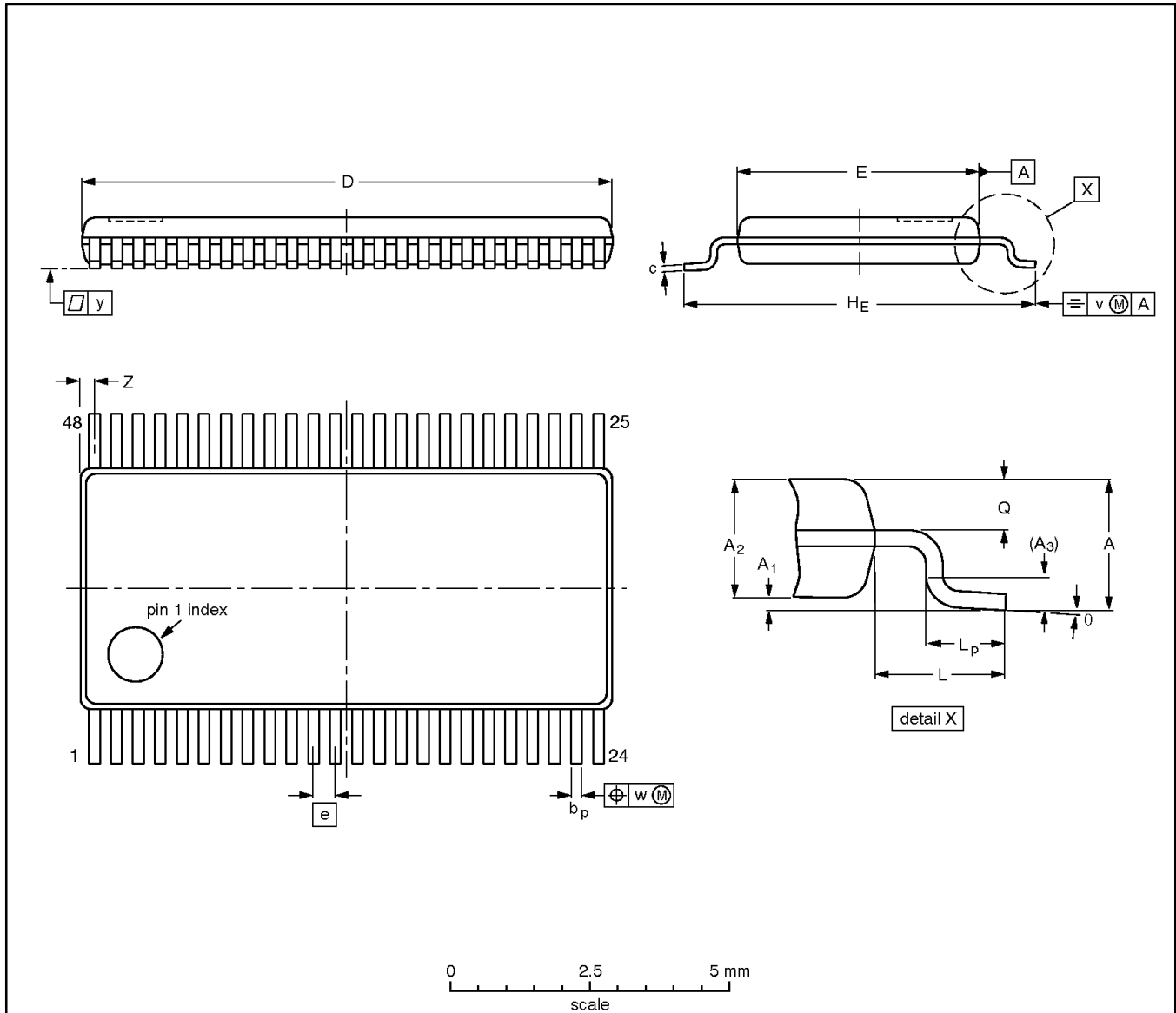
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

DDR PC1600-PC3200 14-bit SSTL<sub>2</sub>  
registered driver with differential clock inputs

SSTVF16857

TSSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.80 9.60	4.50 4.30	0.40	6.60 6.20	1.00	0.70 0.50	0.40 0.30	0.20	0.07	0.08	0.40 0.10	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

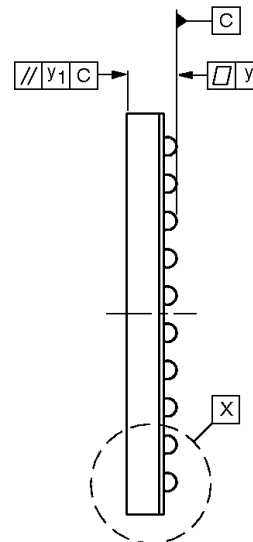
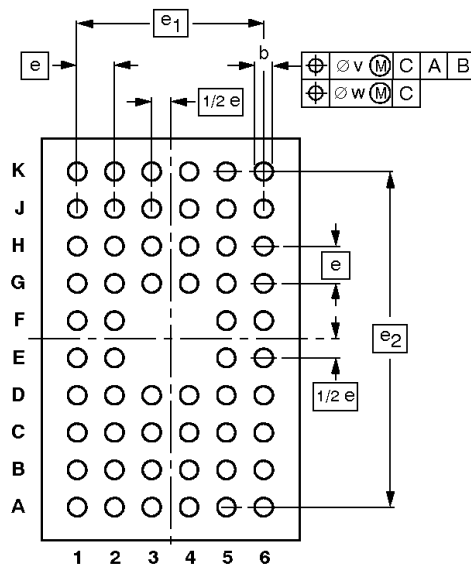
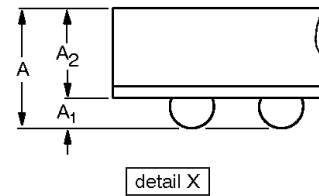
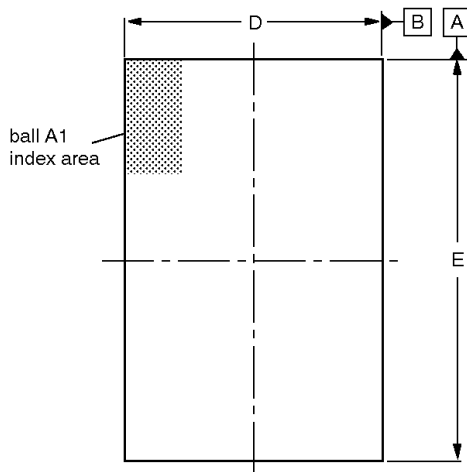
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT480-1		MO-153				97-03-20 99-12-27

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

SSTVF16857

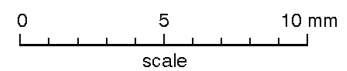
**VFPGA56: plastic very thin fine-pitch ball grid array package; 56 balls;**  
**body 4.5 x 7 x 0.65 mm**

**SOT702-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	0.97	0.28 0.16	0.69 0.61	0.37 0.27	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT702-1		MO-225				01-06-06 01-06-25

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DDR PC1600-PC3200 14-bit SSTL\_2  
registered driver with differential clock inputs

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SSTVF16857

**REVISION HISTORY**

Rev	Date	Description
_1	20030919	<b>Product data (9397 750 12077); ECN 853-2405 30362 dated 18 September 2003.</b>

# DDR PC1600-PC3200 14-bit SSTL\_2 registered driver with differential clock inputs

SSTVF16857

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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9397 750 12077

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