ST2226A

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PWM-Controlled Constant Current Driver for LED Displays

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ST2226A

PWM-Controlled Constant Current Driver for LED Displays

General Description

The ST2226A is a LED driver incorporating shift registers, data latches, 16-channel constant current circuitry with current value set by an external resistor, 1024 gray level PWM (Pulse Width Modulation) functional unit and time division capability. Each channel can provide a maximum current of 60 mA. Time division operation allows driving up to 1 or 2 LEDs with a single output channel (mode-1 and mode-2 respectively).

Block Diagram

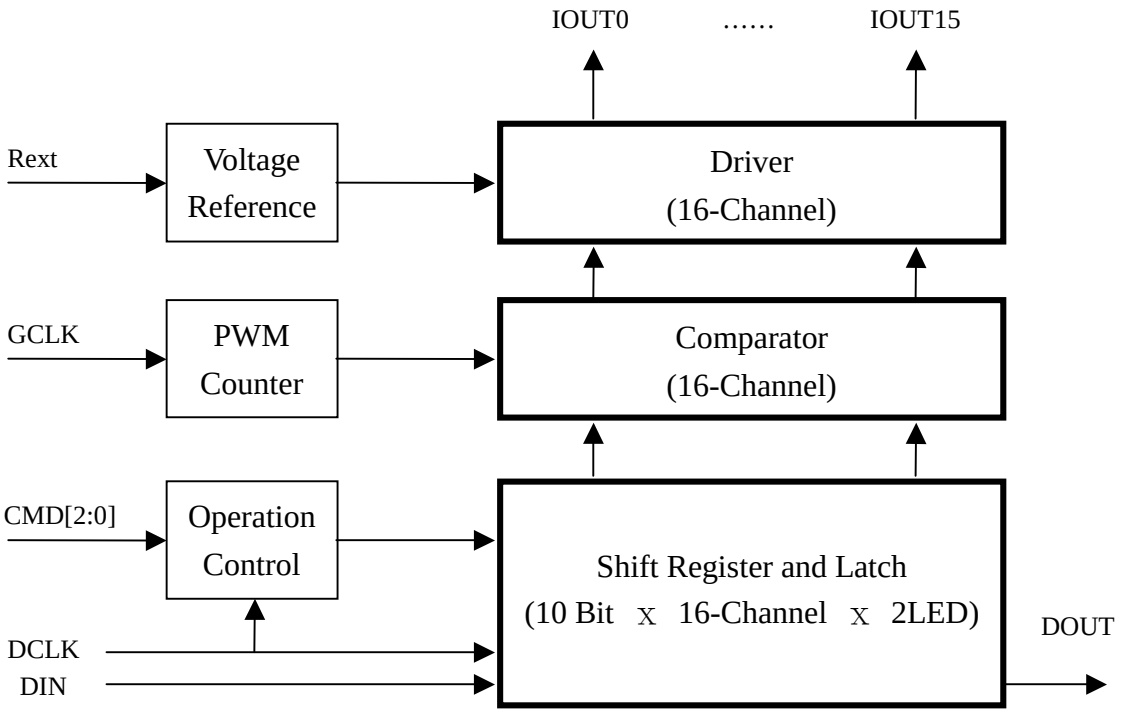


Figure 1. Functional block diagram

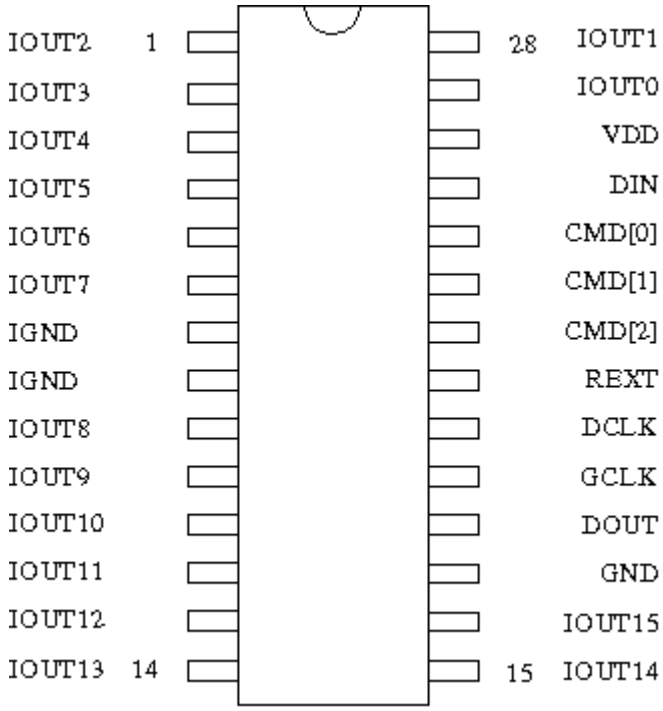
Features

- Constant current outputs with current value settings by an external resistor
- Maximum output current: 60 mA
- Time division output allows the driving of 1 or 2 LEDs with a single output
- Maximum / minimum output voltage: 10V / 1.25V
- 10 bits luminance data with PWM current outputs
- Serial shift-in architecture for luminance data in time division Mode 1 and Mode 2

Absolute Maximum Ratings

Supply Voltage (AV_{DD}, DV_{DD})	-0.3 to 6	V
Input Voltage Range (V_{IN})	-0.3 to DV_{DD}+0.3	V
Driver Output Voltage Range (V_{OUT})	-0.3 to 10	V
Driver Output Current (I_{OUT})	0 to 60	mA
Power Dissipation (T_a = 50 ℃or less)	2.50, SDIP28 1.32, SOP28 2.92, QFN32	W
Thermal Resistance (Θ_{ja})	40.0, SDIP28 75.9, SOP28 34.2, QFN32	℃ / W
Operating temperature range (T_{op})	-40 to 85	℃
Storage temperature range (T_{stg})	-55 to 150	℃

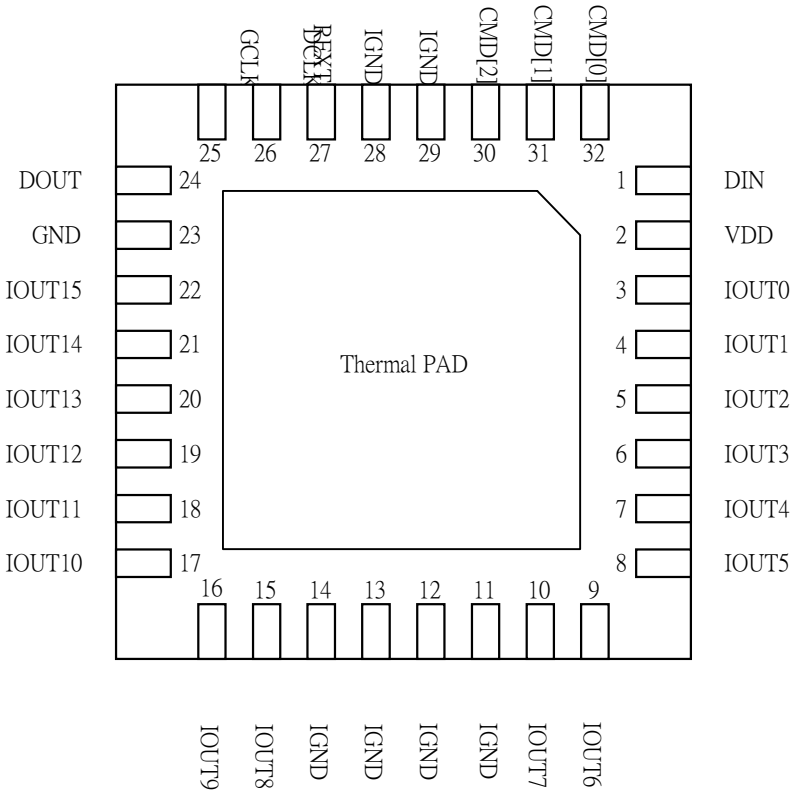
Pin Connection (SDIP28 / SOP28 Top View)



Pin Assignment (SDIP28 / SOP28)

Pin No.	NAME	Pin No.	NAME
1	IOUT2	15	IOUT14
2	IOUT3	16	IOUT15
3	IOUT4	17	GND
4	IOUT5	18	DOUT
5	IOUT6	19	GCLK
6	IOUT7	20	DCLK
7	IGND	21	REXT
8	IGND	22	CMD[2]
9	IOUT8	23	CMD[1]
10	IOUT9	24	CMD[0]
11	IOUT10	25	DIN
12	IOUT11	26	VDD
13	IOUT12	27	IOUT0
14	IOUT13	28	IOUT1

Pin Connection (QFN32 Bottom View)



Pin Assignment (QFN32)

Pin No.	NAME	Pin No.	NAME	Pin No.	NAME
1	DIN	12	IGND	23	GND
2	VDD	13	IGND	24	DOUT
3	IOUT0	14	IGND	25	GCLK
4	IOUT1	15	IOUT8	26	DCLK
5	IOUT2	16	IOUT9	27	REXT
6	IOUT3	17	IOUT10	28	IGND
7	IOUT4	18	IOUT11	29	IGND
8	IOUT5	19	IOUT12	30	CMD[2]
9	IOUT6	20	IOUT13	31	CMD[1]
10	IOUT7	21	IOUT14	32	CMD[0]
11	IGND	22	IOUT15	Thermal PAD	IGND

Pin Description

NAME	PIN NO.	I/O	DESCRIPTION
CMD[2:0]	SDIP/SOP: 22, 23, 24 QFN: 30, 31, 32	I	Encoded commands for data transfer, time division operation and PWM display: CMD[2:0] Command [000]: Mode-1 time division operation / No operation for display [001]: Mode-2 time division operation / No operation for display [010]: Data transfer enable (Shift-In) [011]: Data latch strobe (Capture) [100]: First LED emitting [101]: Second LED emitting [110]: LED emitting disable / IOUT disable (Stop) [111]: Test mode CMD commands are latched at the rising edges of DCLK. There is one DCLK latency between Shift-in command latched and data shift-in.
DIN	SDIP/SOP: 25 QFN: 1	I	Serial input for luminance data (time division mode-1/2)
DOUT	SDIP/SOP: 18 QFN: 24	O	Serial output for luminance data (time division mode-1/2).
DCLK	SDIP/SOP: 20 QFN: 26	I	Synchronous clock input for command and serial data transfer. The input data of DIN is synchronous to rising edges of DCLK, and transferred to DOUT on falling edges of DCLK.
GCLK	SDIP/SOP: 19 QFN: 25	I	Clock input for PWM operation.
IOUT0-15	SDIP/SOP: 27, 28, 1, 2 3, 4, 5, 6, 9, 10, 11, 12 13, 14, 15, 16 QFN: 3, 4, 5, 6, 9, 10, 15, 16, 17, 18, 19, 20, 21, 22	O	LED driver outputs.

REXT	SDIP/SOP: 21 QFN: 27	O	Driver current setting. LED current is set to a current value by connecting an external resistor between REXT and GND.
VDD	SDIP/SOP: 26 QFN: 2	-	Power supply
GND	SDIP/SOP: 17 QFN: 23	-	Analog and digital ground
IGND	SDIP/SOP: 7, 8 QFN: 11, 12, 13, 14, 28, 29, Thermal pad	-	Two ground-pin for driver outputs.

Recommended Operating Conditions

DC Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD}, AV_{DD}	4.75	5	5.25	V
Driver output voltage when driver on, V_{OUT}	1.25	-	5	V
Driver output voltage when driver off[1], V_{OUT}	0	-	10	V
Driver output current, I_{OUT}	5	-	60	mA
High-level input voltage, V_{IH}	$0.8DV_{DD}$	-	DV_{DD}	V
Low-level input voltage, V_{IL}	0	-	$0.2\ DV_{DD}$	V
High-level output current, I_{OH}	-	-	-1	mA
Low-level output current, I_{OL}	-	-	1	mA
Operating free-air temperature[2], T_{op}	-20	-	80	℃

AC Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
DCLK clock frequency, f_{DCLK}		-	-	15	MHz
DCLK pulse duration, t_{wh} / t_{wl}	High or low level	20	-	-	ns
DCLK rise/fall time t_r / t_f		-	-	40	ns
GCLK clock frequency, f_{GCLK}		-	-	20	MHz
GCLK pulse duration, t_{wh} / t_{wl}	High or low level	15	-	-	ns
GCLK rise/fall time t_r /t_f		-	-	20	ns
Setup time, t_{su}	CMD to DCLK DIN to DCLK DCLK to CMD	25 25 25	-	-	ns
Hold time, t_h / t_{wh}	CMD to DCLK DIN to DCLK DCLK to CMD	25 25 25	-	-	ns

1. The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (10V).
2. Recommended junction temperature range is from –20 to 150 ℃.

Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
High-level digital output voltage, V_{OH}		DV_{DD}-0.5	-	-	V
Low-level digital output voltage, V_{OL}		-	-	0.5	V
Input current, I_I		-	-	±1	μA
Supply current (Digital)	DCLK = 10MHz, GCLK = 10MHz		0.5		mA
Supply current (Analog)	REXT = 2K		14		mA
Voltage reference, V_{BG}	Rext = 2KΩ	1.24	1.26	1.28	V
Driver output current, I_{OUT}	Rext = 2KΩ, V_{OUT} = 2.0V		32.2		mA
Driver output leakage current, I_{OL}		-	-	1	μA
Driver current skew between channels, I_{OL1}	V_{OUT} = 2V, I = 40mA	-	±3	±6	%
Driver current skew between chips, I_{OL2}	V_{OUT} = 2V, I = 40mA	-	±6	±12	%

Switching Characteristics, C_L = 15pF, IOUT = 20mA

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Rise time, t_r	DOUT	-	5	10	ns
	IOUT	-	25	40	
Fall time, t_f	DOUT	-	5	10	ns
	IOUT	-	25	40	
Propagation delay, t_d	GCLK to IOUT	-	30	40	ns

Typical Control Method

1) Command Sequence

To manipulate ST2226A, we should properly control the CMD, DIN, DCLK, and GCLK as following steps:

1. Issue command "*Shift-in*", and then enter luminance data DIN. Note that ST2226A starts to shift-in data at the DCLK rising edge next to the edge which latched *Shift-in* command.
2. After data are completely entered, send command "*Capture*" to save data in registers.
3. Send command "*Disable*". This step is needed before the "Emitting" command to keep the chip synchronized.
4. Issue command "*Emitting" or "Disable*". Note that:
   A. ST2226A generates its output in one-shot fashion, i.e. the output after (1024) x T_{GCLK} is always zero.
   B. There are 2 GCLK latencies between the latched *LED Emitting/Disable* command and PWM start/stop. This is shown in Figure 2.
5. Repeat step 1~4. In the same frame, the luminance data doesn't have to change, just repeat step 3~4. Note that the second command "*Emitting*" will be omitted if (1024) x T_{GCLK} PWM has not finished, unless the "*Disable*" command is sent in advance.

The process discussed above could be summarized in the following table and timing diagram. At the same time, DCLK and GCLK remain free running.

Table 1. Example of Command Sequence

	Frame N-1			**Frame N**															**Frame N+1**		
CMD			*NOP*[3]	*Capture*	*Disable*	*Emitting / Disable*	*Shift-In*	…	*Shift-In*	*Disable*	*Emitting / Disable*	*Shift-In*	…	*Shift-In*	*Disable*	*Emitting / Disable*	*NOP*	…	*NOP*	*Capture*	…	…
DIN	…	…	…	*Don't care.*	*Don't care.*	*Don't care.*	*Don't care.*	*Shift-in Data.*	…	*Shift-in Data*	*Don't care.*	*Don't care.*	*Shift-in Data*	…	*Shift-in Data*	*Don't care.*	*Don't care.*	*Don't care.*	*Don't care.*	…	…	

[3] We used the NOPs (No operation) to wait for the next frame data (at 60Hz) ready.

2) LED Emitting Time and Current

ST2226A adjusts the LED luminance using PWM (pulse width modulation) technique. The luminance data (D_V) has a resolution of 10 bits (1024steps) and can be set independently for each LED. The relationship between Iout, luminance data, and emitting time is shown in Figure 2.

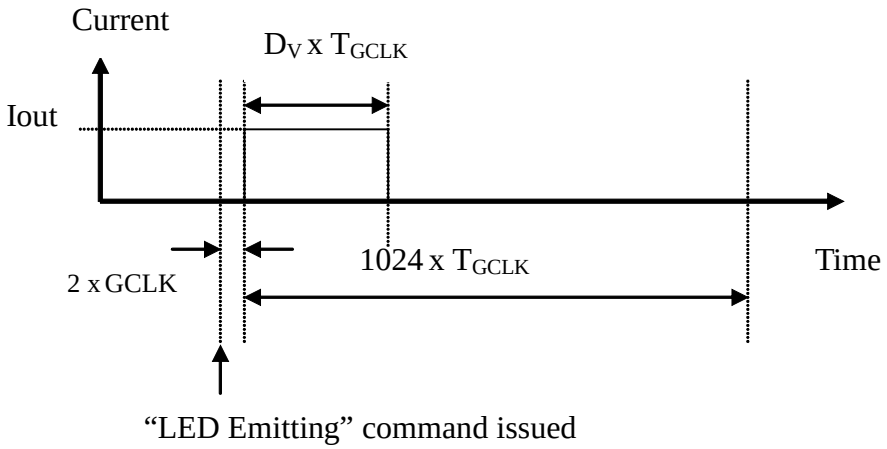


Figure 2. PWM Current Output

3) Phase Relationship of DCLK and GCLK

Matching ST2226A's GCLK and DCLK is an important step in the system design. If there is a certain length of delay between the rising edge of DCLK and of GCLK, the command "*LED Emitting*"& "*LED Disable*" will not be correctly recognized, which will then cause the display data loss. It is safe to keep both of GCLK and DCLK rising at the same time, so that the frequencies of DCLK and GCLK have an integer multiple relationship.

For the design which has a fixed, corresponding clock phase relationship between GCLK & DCLK, e.g. the display controller is built by FPGAs, this clock phase problem is unlikely to happen. However, if it dose happen, try to control the clock phase, e.g. invert GCLK, to solve this problem. On the contrary, for the design which can not control the clock phase, e.g. the display controller is built by microprocessors, the following sequential modification on "*Emitting*" & "*Disable*" commands is preferred to be employed in the design:

1. Gate GCLK.
2. Issue "*Emitting*" or "*Disable*" command.
3. Let go of GCLK.

Timing Diagrams

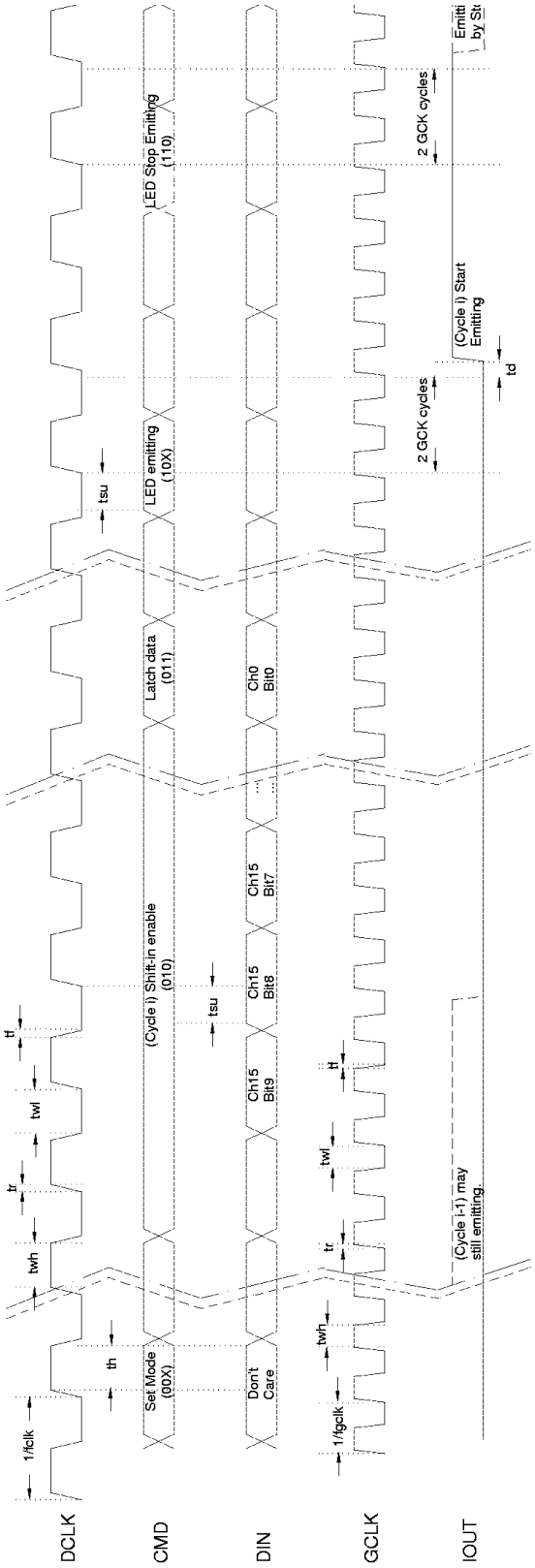
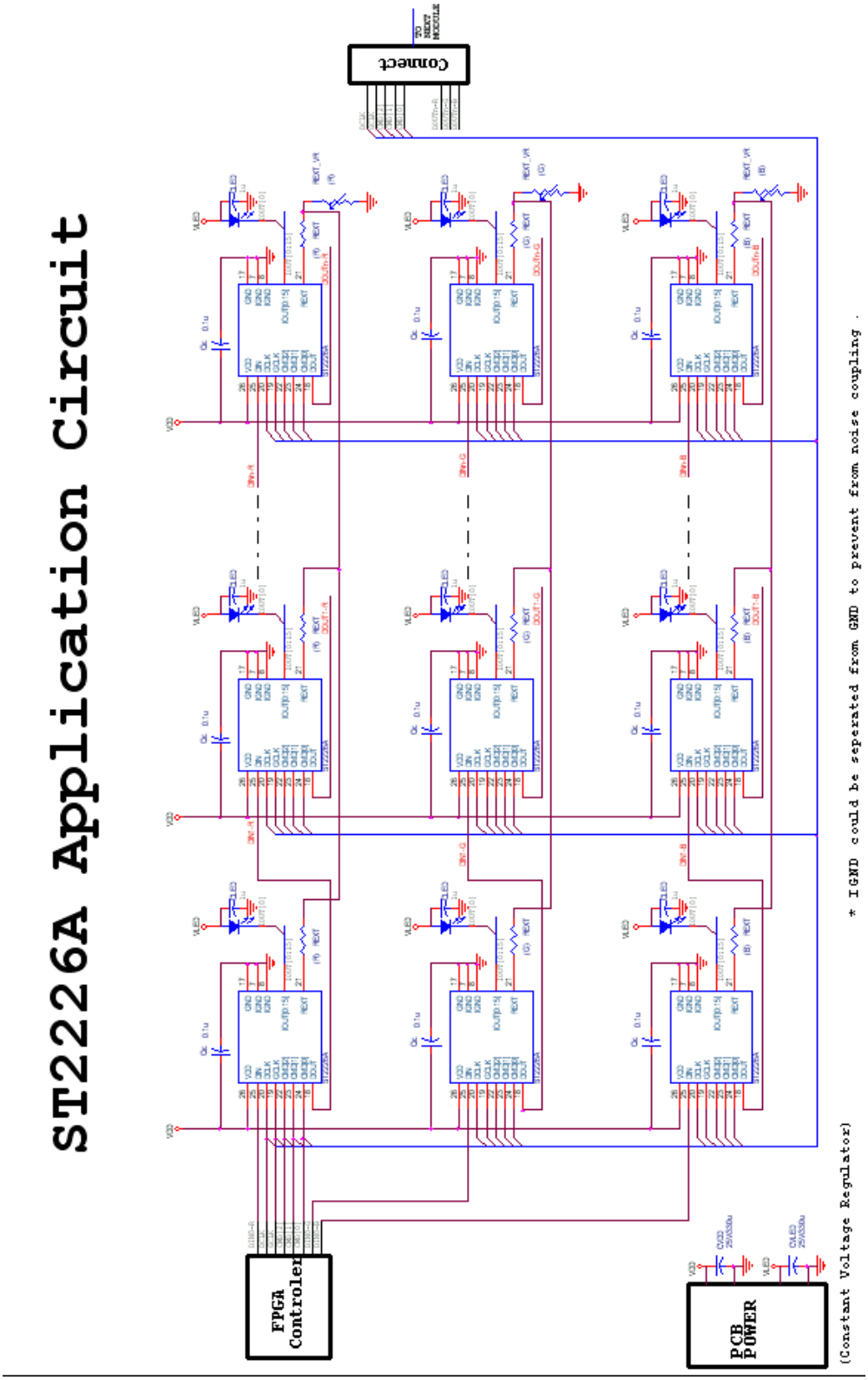


Figure 3. Timing Diagram

Application Diagrams



Detailed Description

1) Time Division Operation

Since ST2226A can drive 1 LED or 2 LEDs, the user can choose either MODE1 luminance data or MODE2 luminance data. After the luminance data is given, a command should be issued so that the driver can operate in MODE1 or in MODE2. Figure 4 shows the route of data shift-in in MODE2. Later we will explain the data structure of MODE1 and MODE2 in more details.

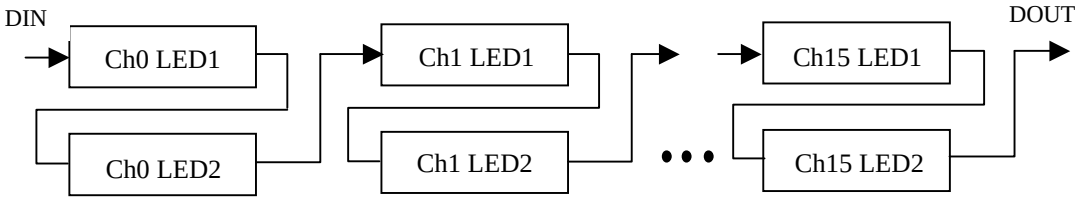


Figure 4. Block Diagram for Primary Bus.

Figure 5. shows how to switch between 2 LEDs. When "*LED1 Emitting*" command is sent, LED1 PWM output will start 2 GCLK later. At the same time, the switch of LED1 should be turned on. On the other hand, LED2 switch should be turned on when LED2 PWM output starts. Again, "*Disable*" command must be sent before "*LED1/LED2 Emitting*". By periodically switching the emitting commands and LED switches, we could drive 2 LEDs per channel.

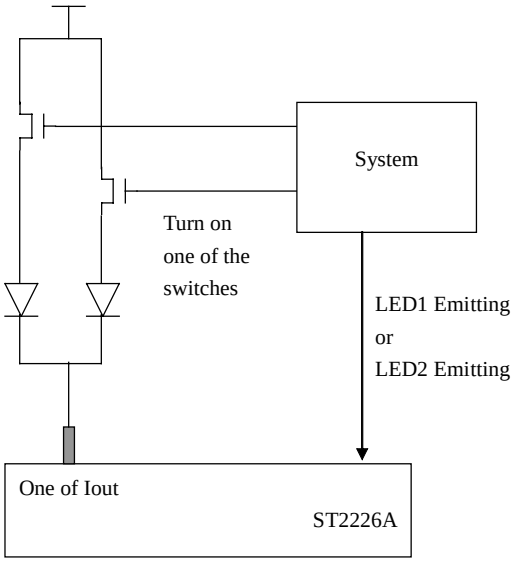


Figure 5. System Configuration for MODE 2 Operation

2) Serial Shift-In Luminance Data

In the MODE1 operation, the data for shift registers and latches is set as {16(channel) x 10 bit (luminance) x 1(led)} whereas in MODE2 operation, the data is set as {16(channel) x 10 bit (luminance) x 2(led)} configuration. The driver IC can remember both 2 sets of luminance data.

The serial shift architecture assumes a FIFO (first-in firs-out) discipline, hence in the MODE1 operation, the most significant bit (MSB, Bit 9, Channel 15) luminance data is the first data shifted in, whereas the least significant bit (LSB, Bit 0, Channel 0) is the last data bit in a data set. The data structure for the MODE1 and MODE2 is shown in the Figure 6. and Figure 7. respectively.

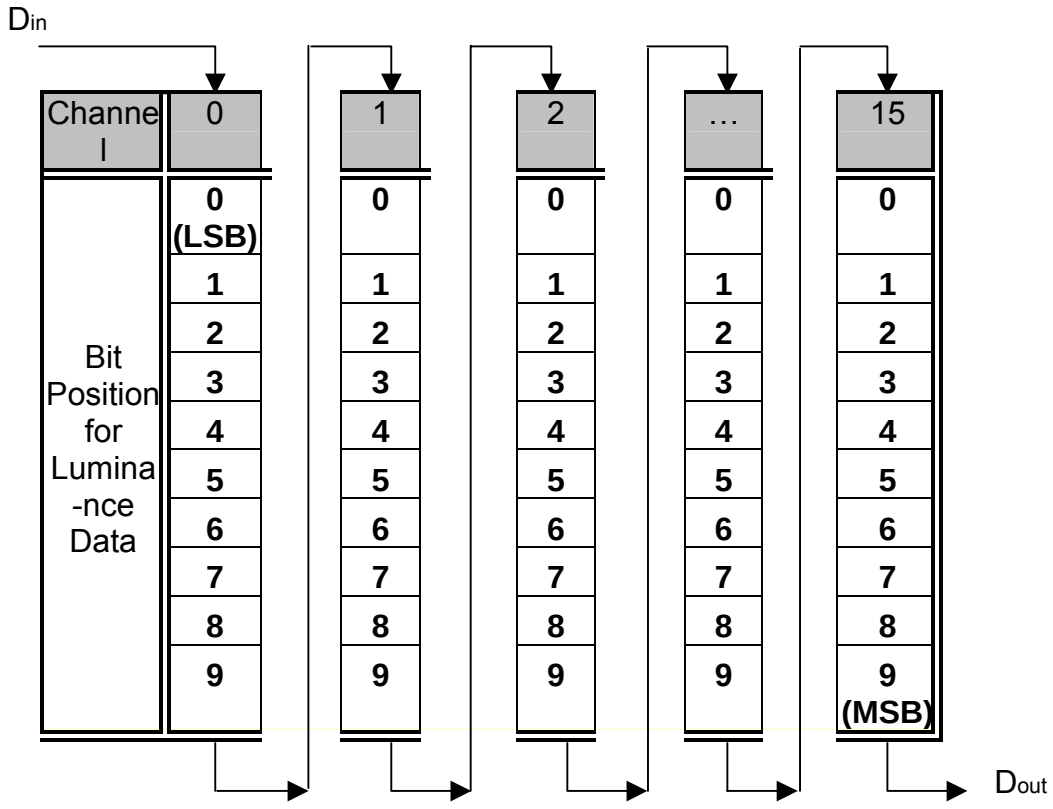


Figure 6. Luminance Data Structure in MODE 1

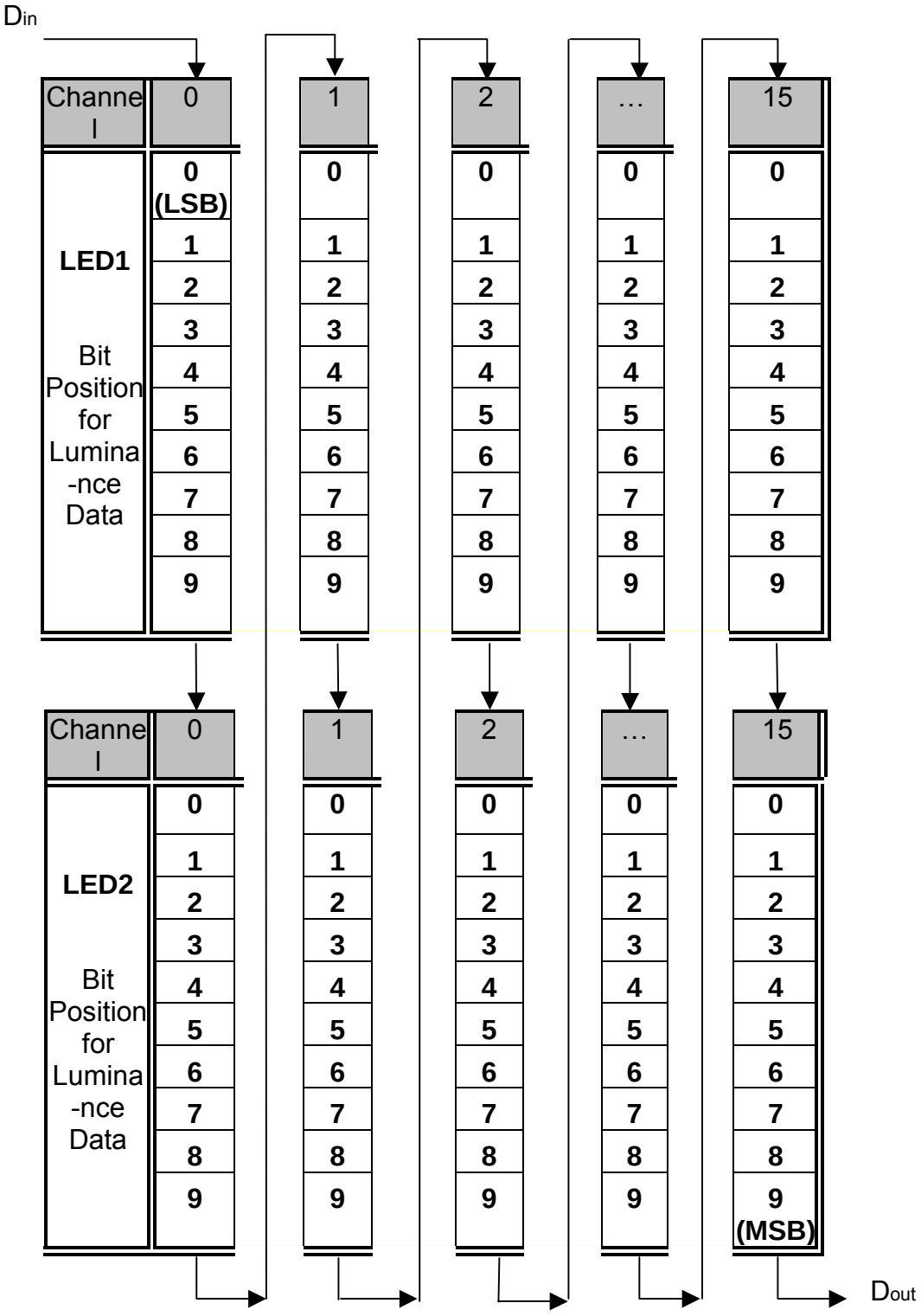


Figure 7. Luminance Data Structure in MODE 2

3) Driver Current Output

The drive current is set by an external resistor, Rext, connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 5mA to the maximum 60 mA. Note that the REXT pin voltage is designed to be independent of supply voltage, temperature, and process variation, and is approximately 1.26V.

The output current could be calculated roughly by the following equation:

Iout = (1.26 / Rext) x 51

The full-scale current IOUT vs. Rext is shown in Figure 8.

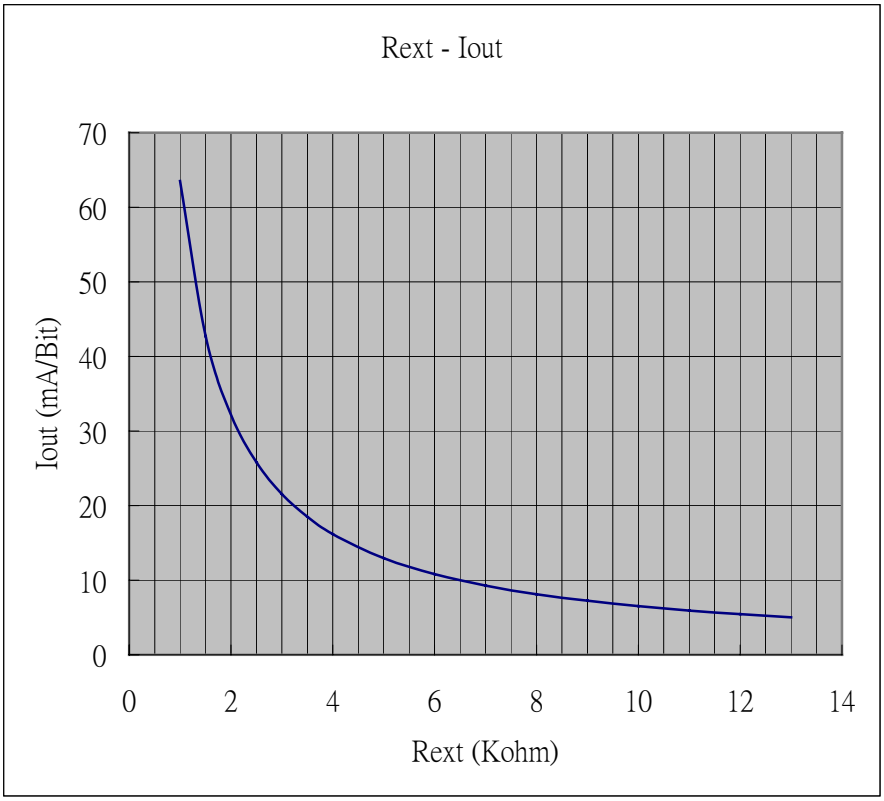


Figure 8. Driver current as a function of R_{EXT}

4) Power Rating

For the relationship between power dissipation and operating temperature, please refer to the following Figure 9.

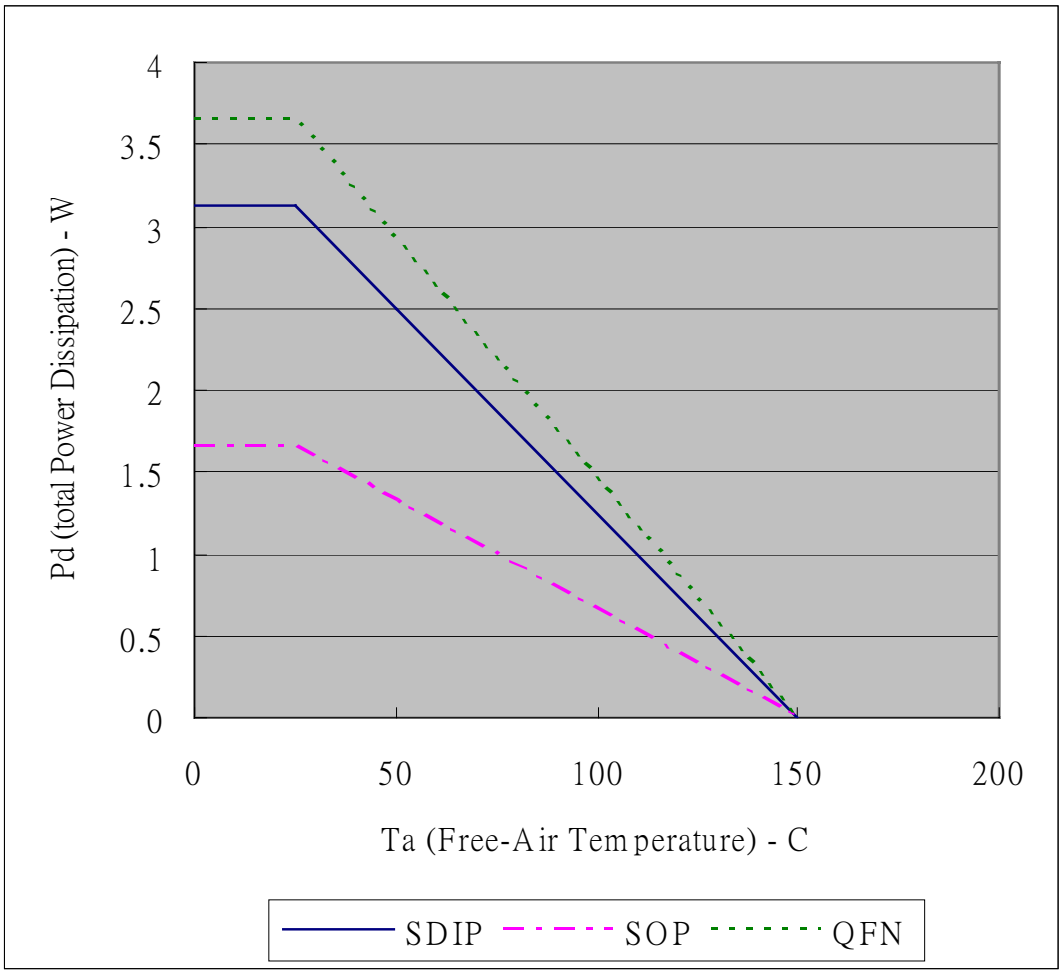


Figure 9. Power Dissipation vs. Operating Temperature

5) Advantages for application

To understand what the advantages over ON-OFF type drivers, we assume that in MODE 1 operation, the frame rate is 60Hz, DCLK & GCLK both run at 10MHz. We can shift in (1/60Hz)/(1/10MHz)=167K bits per frame. One channel takes 10 bits, thus 167K/10=16.7K channels (single color pixels). For two dimension display, we take the square root of 16.7K pixels, which equals 129. The resolution, in this case is 129*129. We can round the data a little bit, and we can construct a 128*128 image by connecting 1024 driver ICs. (1,024 EA drivers*16 channels≒16,384 bit).

Within a frame, there are 1024*16*10=163K DCLK & GCLK cycles, and we know that the PWM takes 1024 GCLK cycles and is one-shot. So we can issue up to 163K/1024=160 PWM cycles within a frame. This can be used as an 160-level total brightness control in addition to the 1024-level pixel-dependent luminance control. These 160- “LED1 Emitting” shall be issued periodically within a frame. Each time when issuing the “LED1 Emitting” command, the shift-in process will be pended for a few cycles; however, we can resume feeding the data right after the “LED1 Emitting” command is issued.

To make the total brightness at full scale, all 160 “LED1 Emitting” commands should be issued. To make the total brightness half of the full scale, we can issue 80-“LED1 Emitting” commands in companion with 80-“LED Disable” commands, so that all the 128*128 LEDs are half of their brightness.

A comparison table for PWM LED driver vs. ON-OFF type is provided for reference.

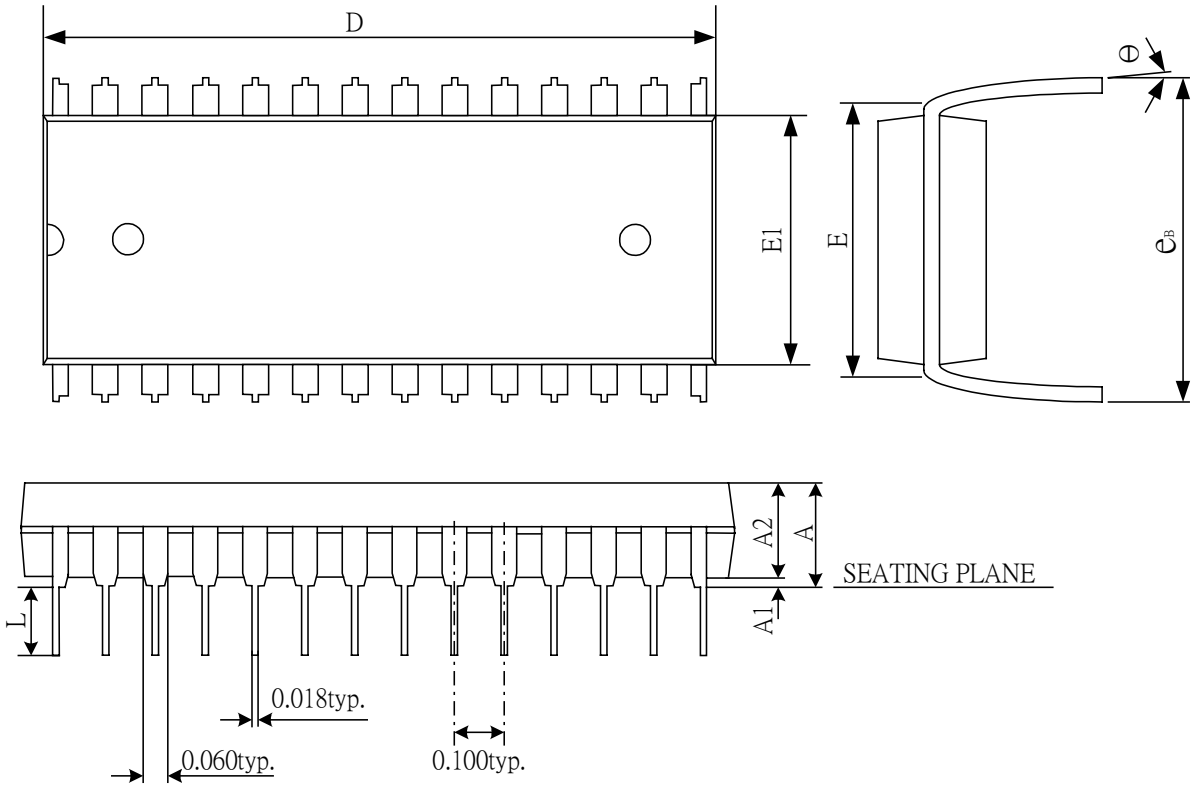
Table 2. Comparison between PWM and ON-OFF Free Running

	PWM	ON-OFF
Frame rate	60	60
No. shift-in pixels	128 x 128	128 x 128
Grayscale for each pixel	1024	1024
Grayscale for overall panel	160	1
Clocks needed per frame	167k	16.8Meg
Clock rate	10 MHz	1.0 GHz[4]

[4] Surely out of spec. Can’t realize in this configuration. System designs for ON-OFF type drivers thus need to reduce frame rate or the no. shift-in pixels or grayscale level for each pixel.

Package Outline Dimension

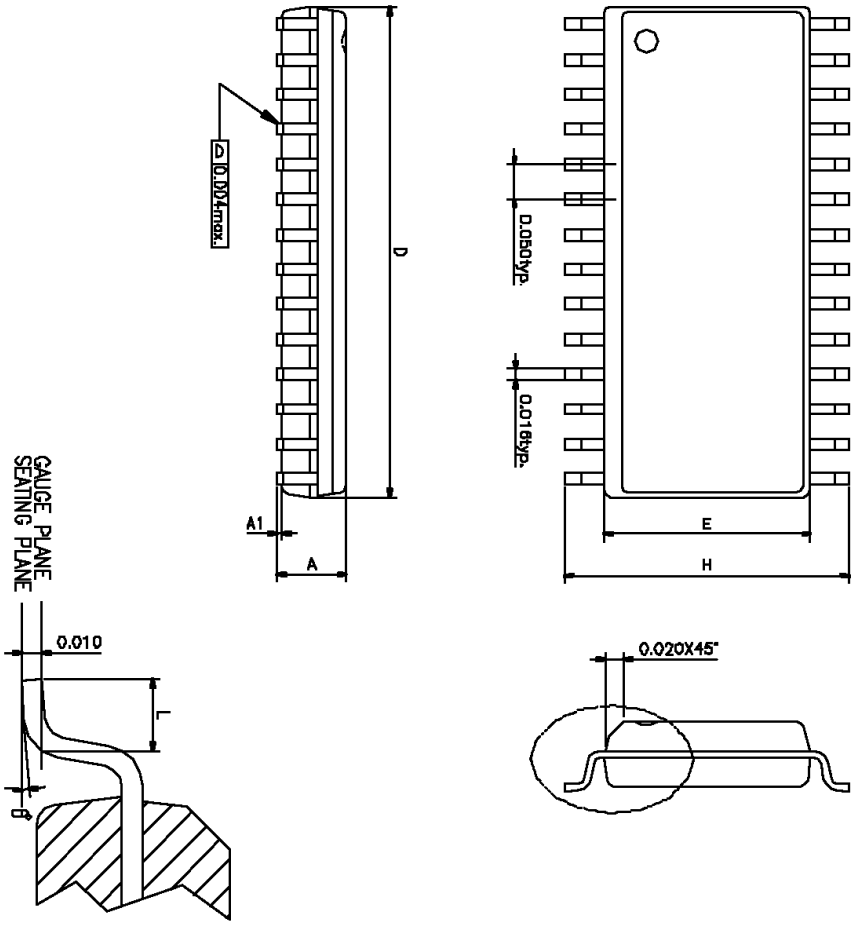
SDIP28



SYMBOLS	DIMENSION IN INCH		
	MIN.	NOM.	MAX.
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E1	0.283	0.288	0.293
E	0.31 BSC		
L	0.115	0.130	0.150
e_B	0.330	0.350	0.370
θ	0	7	15

Note:
1. JEDEC OUTLINE : N/A

SOP28

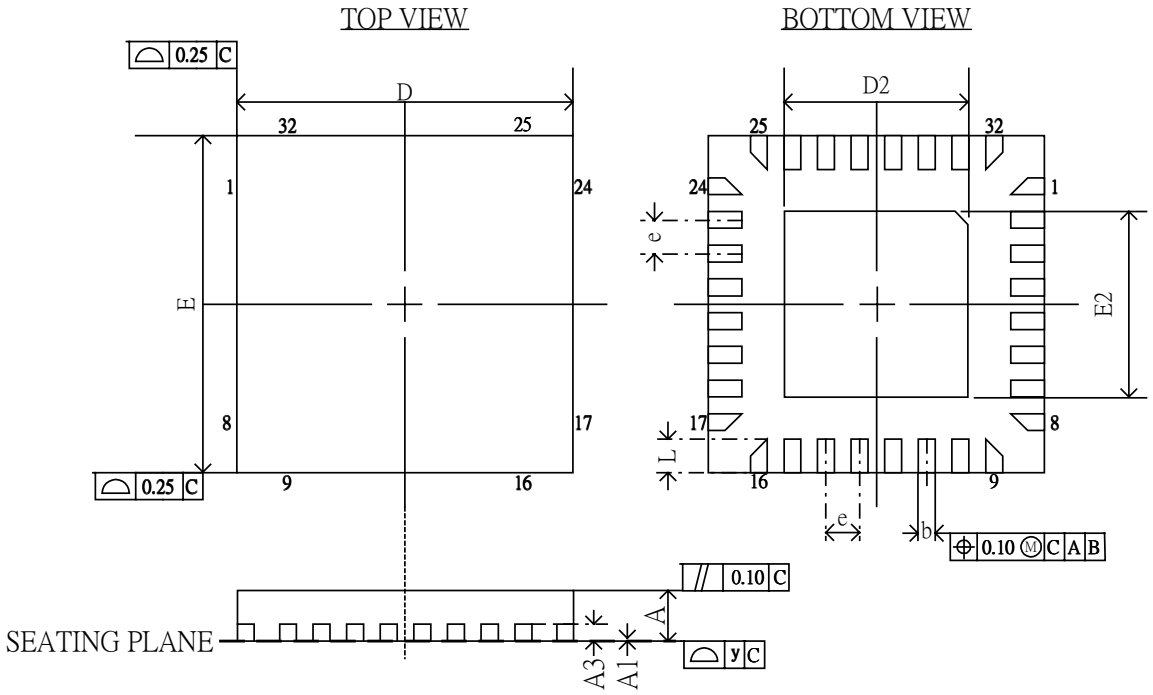


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.697	0.713
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AE
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

QFN32



SYMBOL	DIMENSION (mm)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.25 REF			9.84 REF		
b	0.18	0.23	0.30	7.09	9.06	11.81
D	5.00 BSC			196.85 BSC		
D2	1.25	2.70	3.25	49.21	106.30	127.95
E	5.00 BSC			196.85 BSC		
E2	1.25	2.70	3.25	49.21	106.30	127.95
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.81	15.75	19.69
y	0.10			3.94		

Note: 1.DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145.5M-1994.

2. REFER TO JEDEC STD. MO-220 WHHD-2 ISSUE A

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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