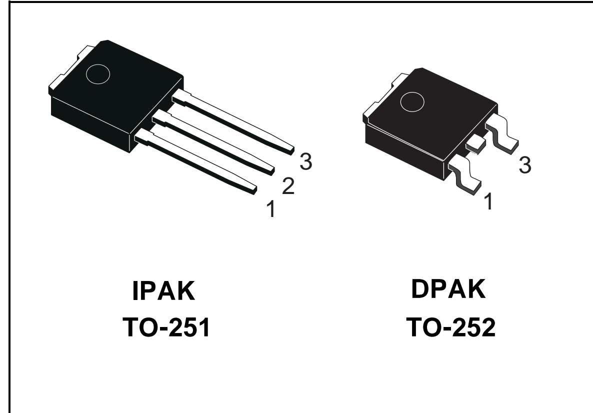
STD1LNC60

N-CHANNEL 600V - 12Ω - 1A - IPAK/DPAK PowerMESH™II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD1LNC60	600 V	< 15 Ω	1 A

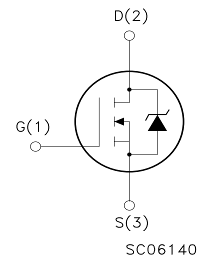
- TYPICAL R_{DS}(on) = 12 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



DESCRIPTION

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITH MODE POWER SUPPLIES (SMPS)
- BATTER CHARGER, ADAPTOR AND STAND-BY POWER SUPPLY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuos) at T_C = 25°C	1	A
I_D	Drain Current (continuos) at T_C = 100°C	0.63	A
I_{DM} (•)	Drain Current (pulsed)	4	A
P_{TOT}	Total Dissipation at T_C = 25°C	30	W
	Derating Factor	0.24	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 1A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	4.16	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
Rthj-sink	Thermal Resistance case-sink Typ	1.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	1	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	40	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.5 A		12	15	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 0.5A		0.87		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		108		pF
C_{oss}	Output Capacitance			18		pF
C_{rss}	Reverse Transfer Capacitance			2.5		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 300V, I_D = 0.5 A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		7.2 8		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 480V, I_D = 1 A, V_{GS} = 10V		7.3 3.4 2.5	10	nC nC nC

SWITCHING OFF

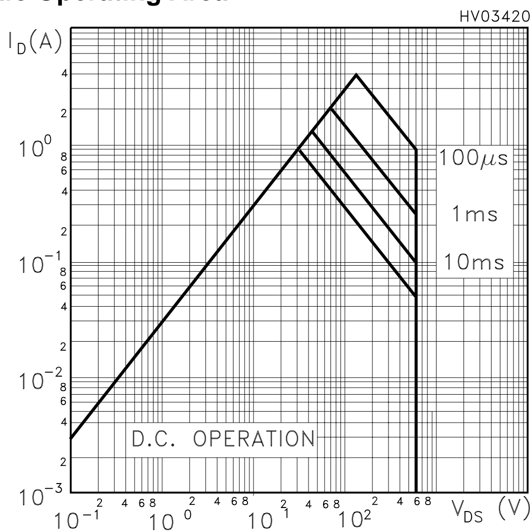
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 480V, I_D = 1 A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		33 11 43		ns ns ns

SOURCE DRAIN DIODE

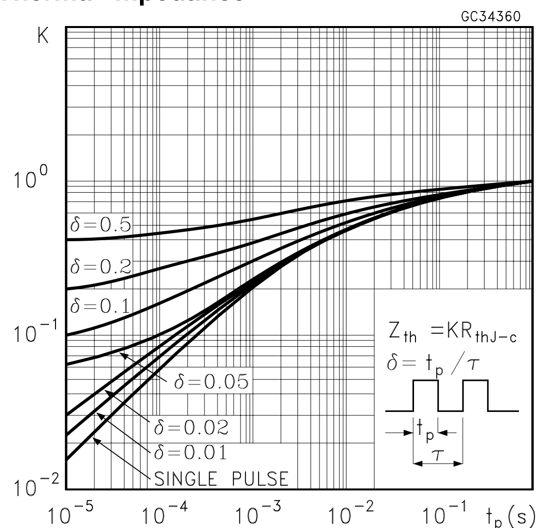
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				1 4	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 1 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1A, di/dt = 100A/µs, V_{DD} = 20V, Tj = 150°C (see test circuit, Figure 5)		450 720 3.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

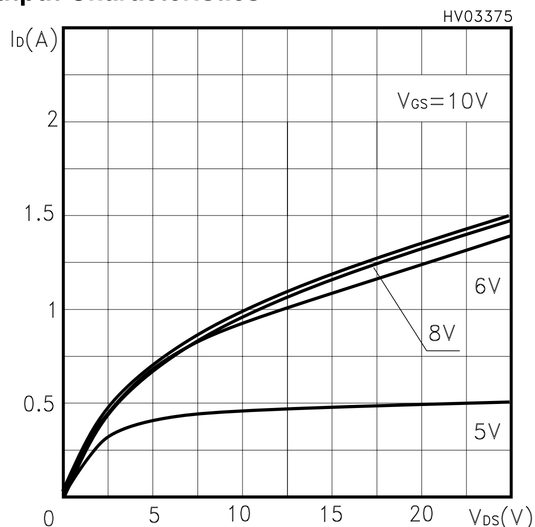
Safe Operating Area



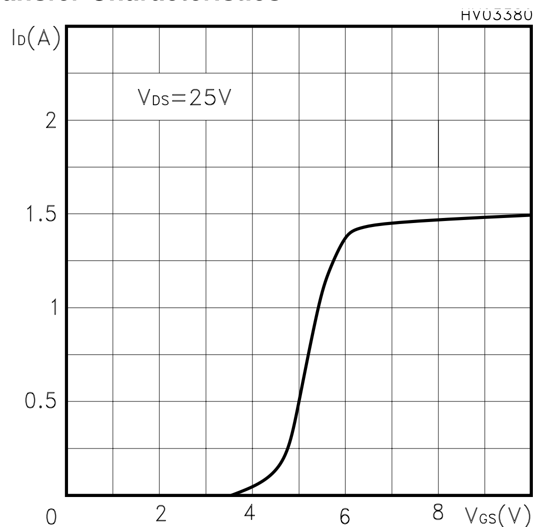
Thermal Impedance



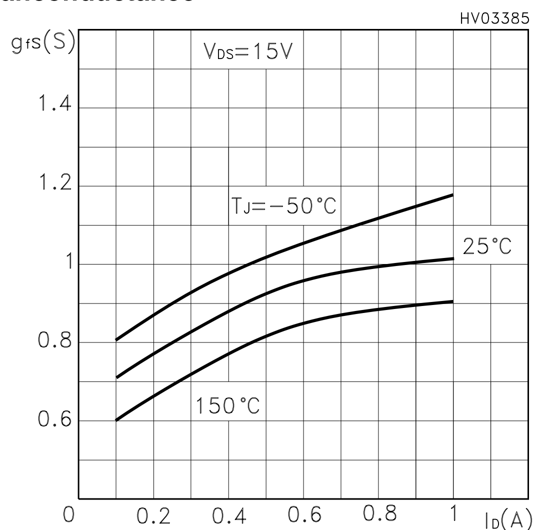
Output Characteristics



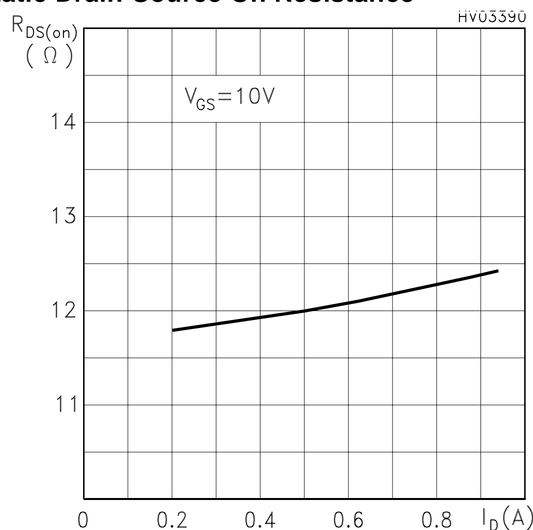
Transfer Characteristics



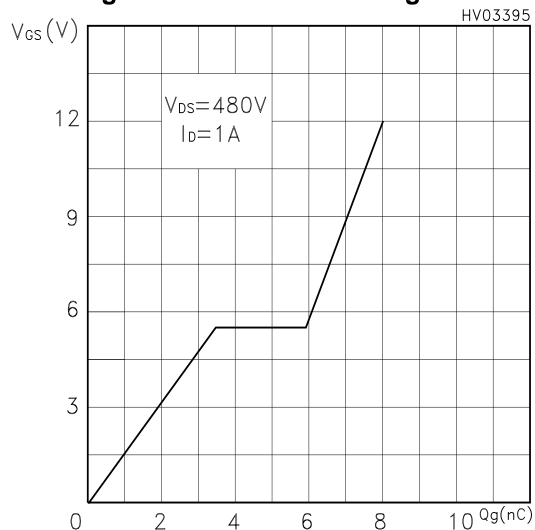
Tranconductance



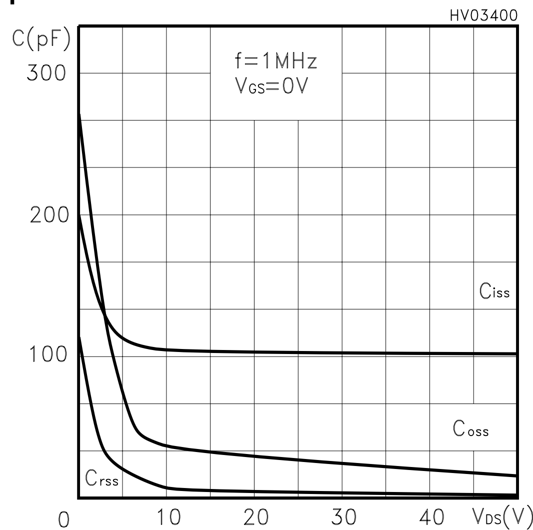
Static Drain-Source On Resistance



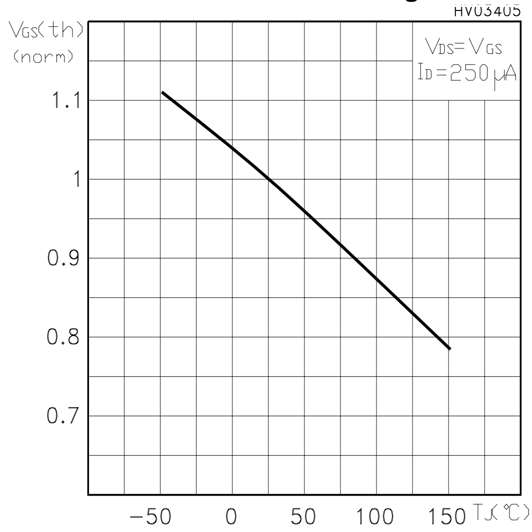
Gate Charge vs Gate-source Voltage



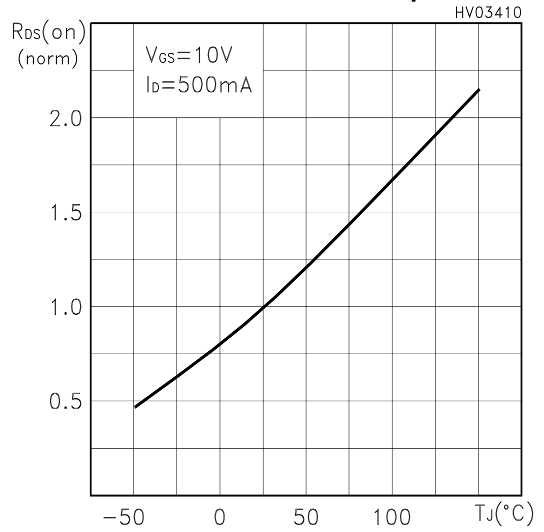
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

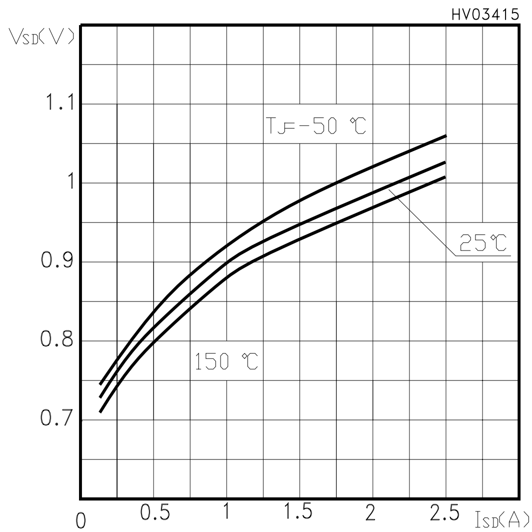


Fig. 1: Unclamped Inductive Load Test Circuit

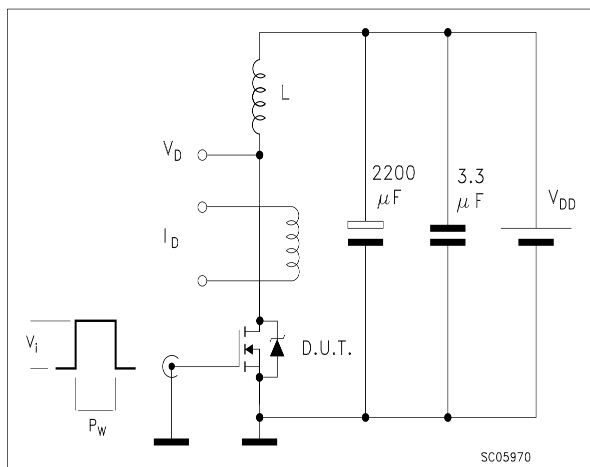


Fig. 2: Unclamped Inductive Waveform

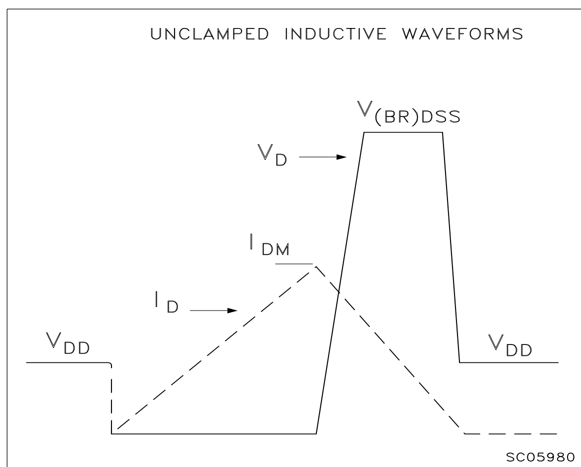


Fig. 3: Switching Times Test Circuit For Resistive Load

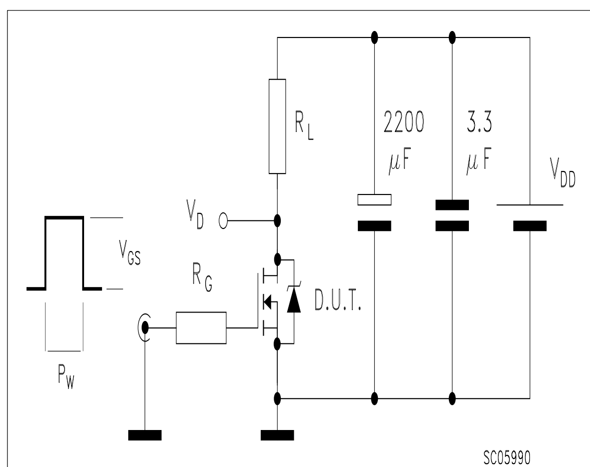


Fig. 4: Gate Charge test Circuit

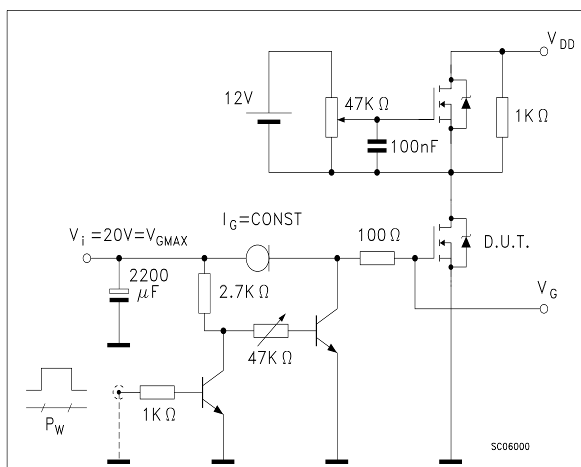
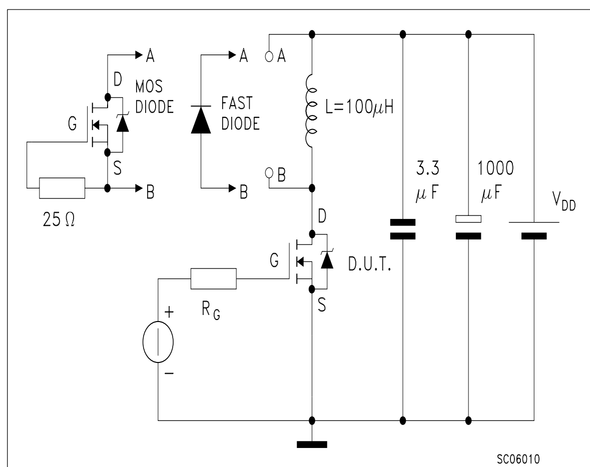
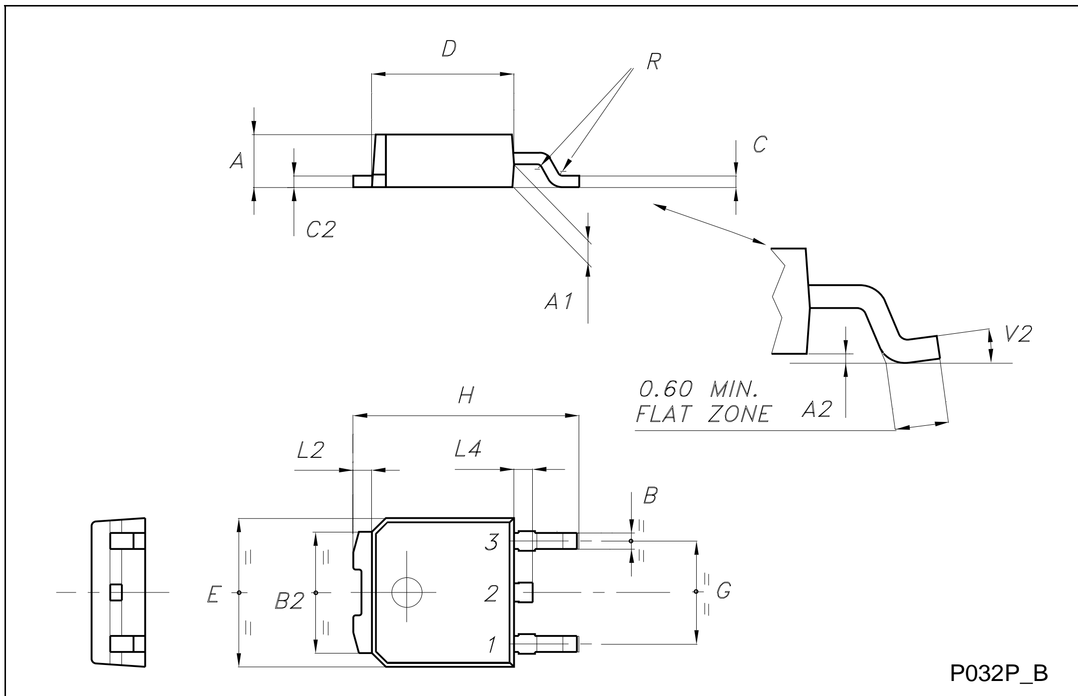


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



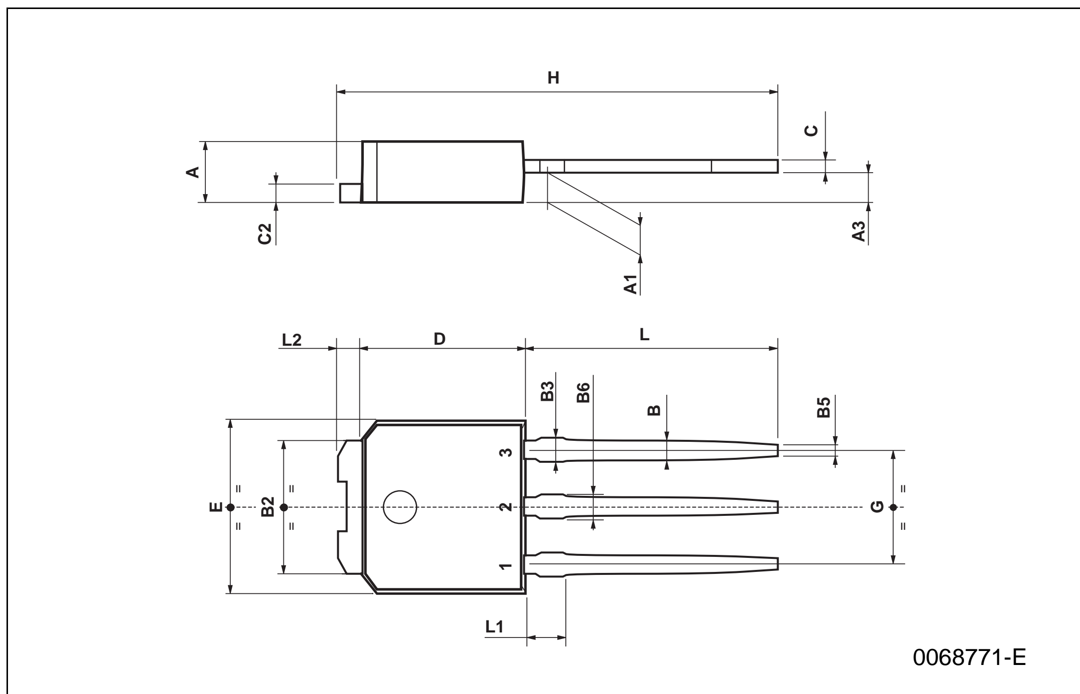
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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