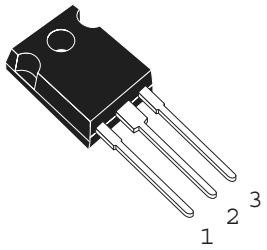
STW240NF55

N-CHANNEL 55V - 0.0027 Ω - 120A TO-247
STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D(1)
STW240NF55	55V	<0.0035Ω	120A

- TYPICAL R_{DS}(on) = 0.0027Ω
- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

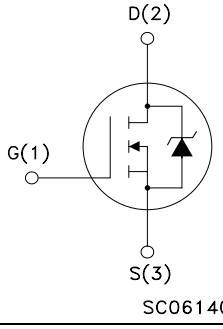


TO-247

DESCRIPTION
This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS
- HIGH CURRENT, HIGH SWITCHING SPEED
- OR-ING FUNCTION

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW240NF55	W240NF55	TO-247	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate- source Voltage	± 20	V
I_D(1)	Drain Current (continuous) at T_C = 25°C	120	A
I_D(1)	Drain Current (continuous) at T_C = 100°C	120	A
I_{DM}(•)	Drain Current (pulsed)	480	A
P_{tot}	Total Dissipation at T_C = 25°C	500	W
	Derating Factor	3.33	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	5	V/ns
E_{AS}(3)	Single Pulse Avalanche Energy	3.5	J
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area.
(1)Current Limited by Package
(2) I_{SD} ≤ 120A, di/dt ≤ 600A/µs, V_{DD} ≤ 48V, T_j ≤ $T_{JMAX.}$
(3) Starting T_j = 25 °C, I_D = 60A, V_{DD} = 30V

THERMAL DATA

$R_{thj\text{-}case}$ $R_{thj\text{-}amb}$ T_l	Thermal Resistance Junction-case Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose (1.6 mm from case, for 10 sec)	Max Max Typ	0.3 50 300	°C/W °C/W °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	55			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C				1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 60 A		2.7	3.5	mΩ

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 15 V I_D = 60 A		100		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		12250 2600 745		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 27.5 V I_D = 60 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		52 235		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=27.5V I_D=120A V_{GS}=10V		350 75 140	480	nC nC nC

SWITCHING OFF

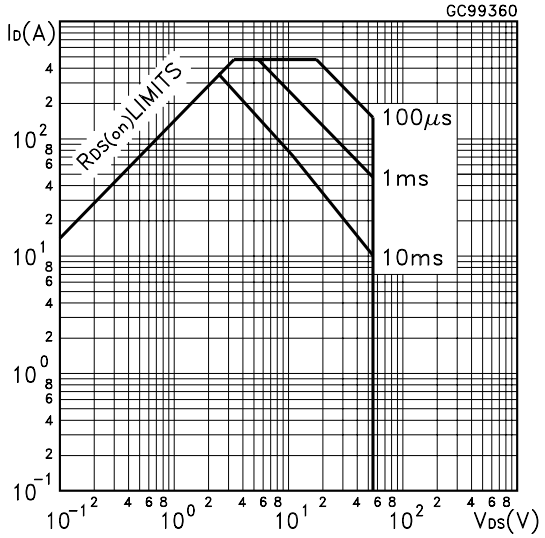
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 27.5 V I_D = 60 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 3)		225 115		ns ns

SOURCE DRAIN DIODE

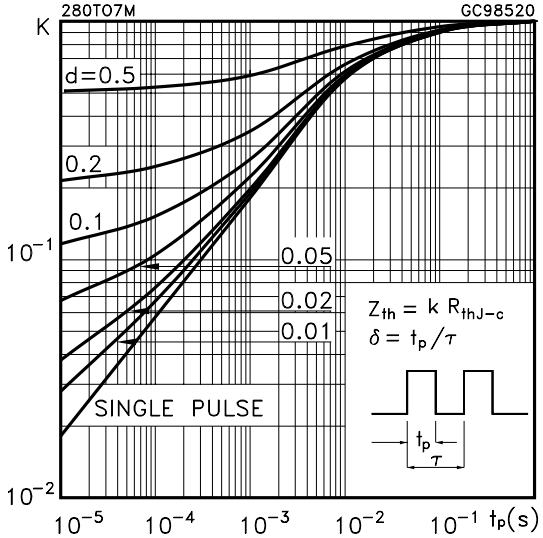
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				120 480	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 120 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 120 A di/dt = 100A/µs V_{DD} = 20 V T_j = 150°C (see test circuit, Figure 5)		115 435 7.6		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

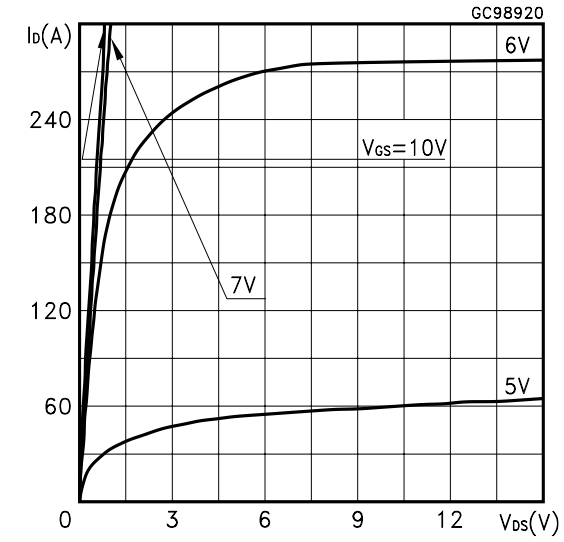
Safe Operating Area



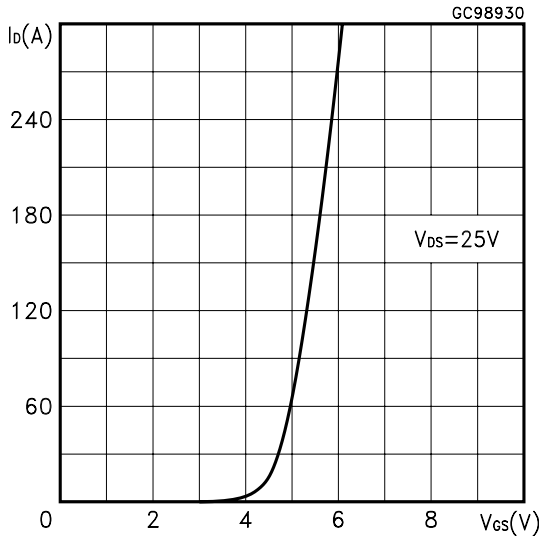
Thermal Impedance



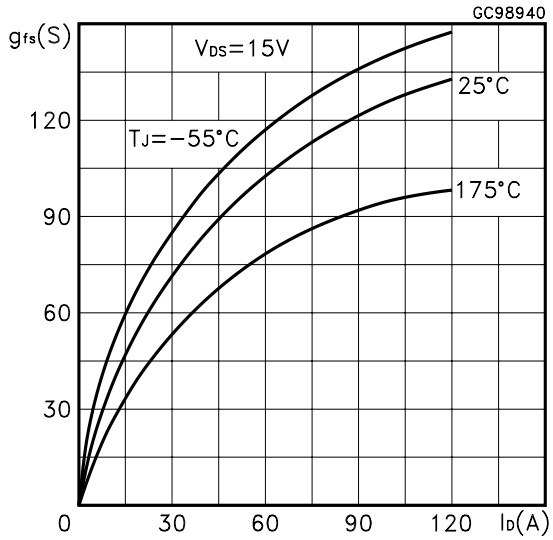
Output Characteristics



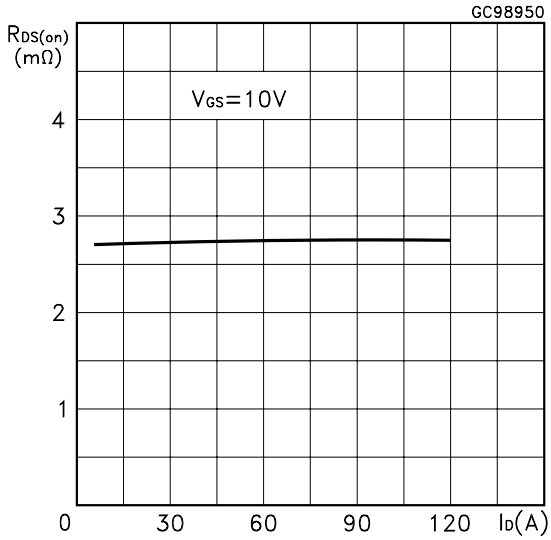
Transfer Characteristics



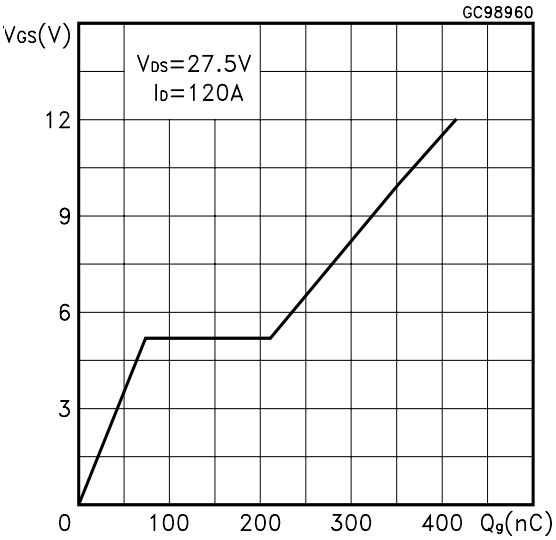
Transconductance



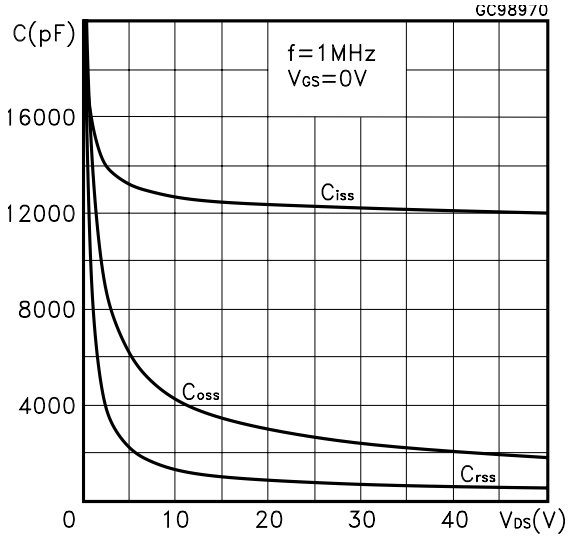
Static Drain-source On Resistance



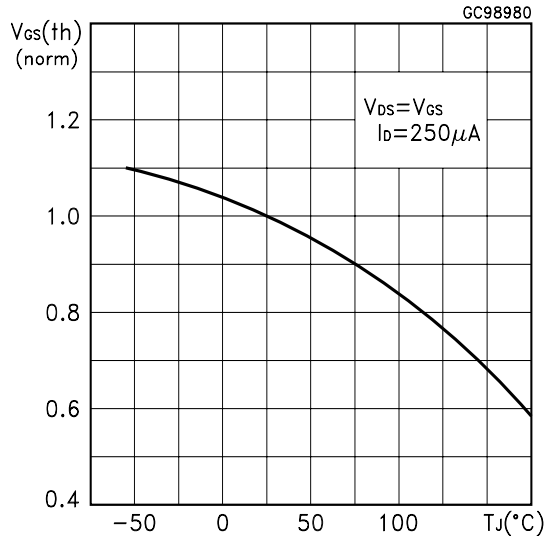
Gate Charge vs Gate-source Voltage



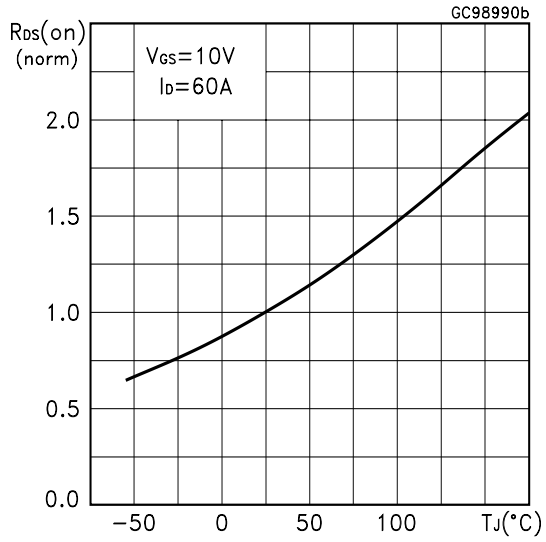
Capacitance Variations



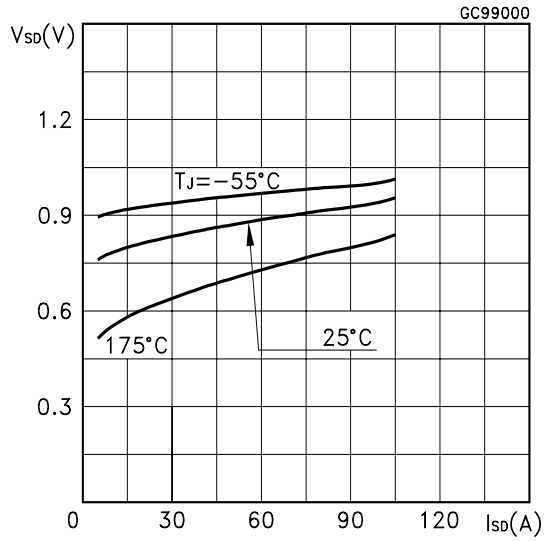
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature

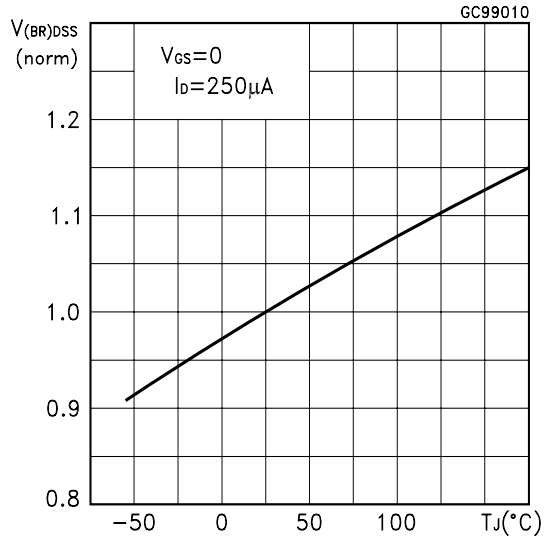


Source-drain Diode Forward Characteristics



.

Normalized Breakdown Voltage vs Temperature



.

Fig. 1: Unclamped Inductive Load Test Circuit

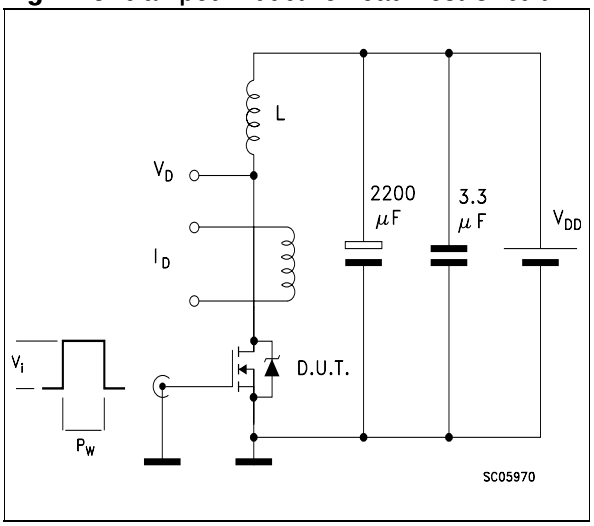


Fig. 2: Unclamped Inductive Waveform

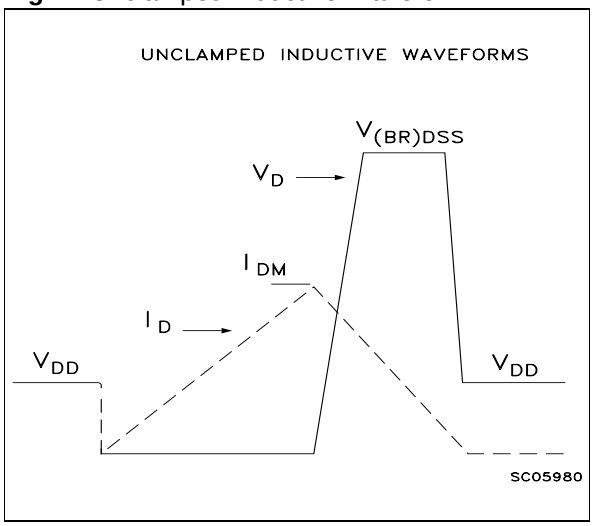


Fig. 3: Switching Times Test Circuits For Resistive Load

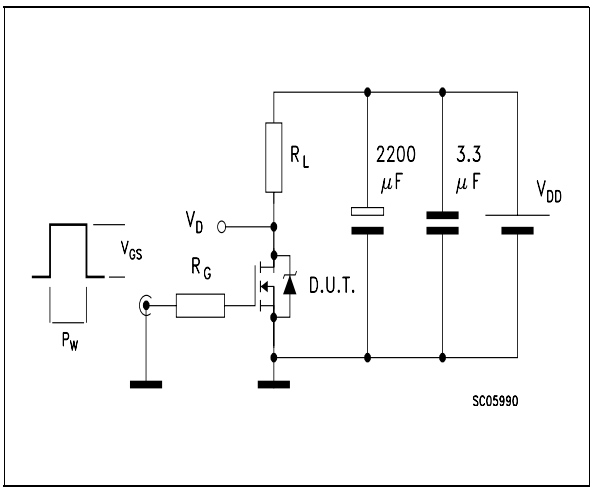


Fig. 4: Gate Charge test Circuit

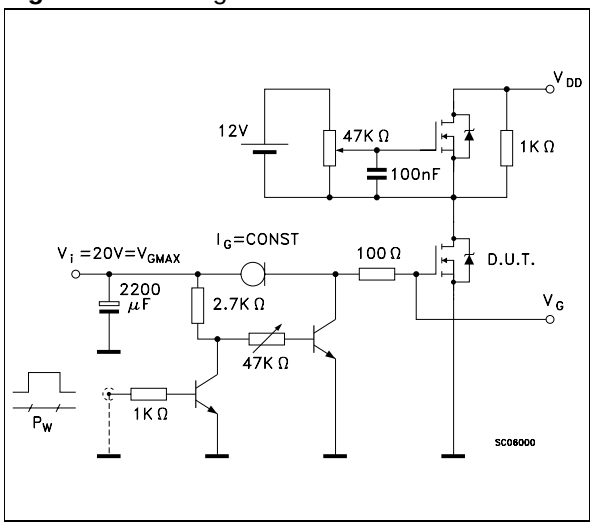
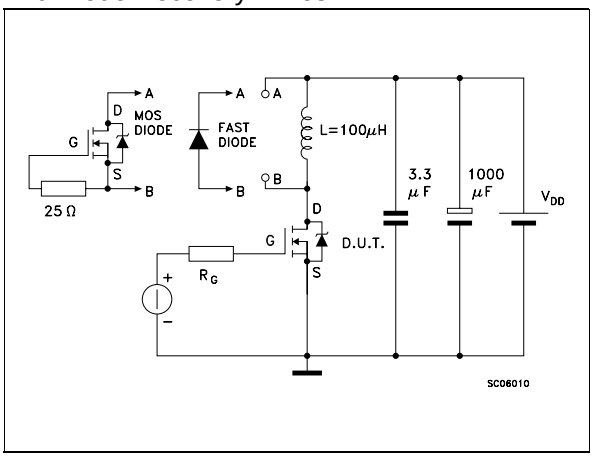


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118