



## N-Channel 25-V (D-S) MOSFET



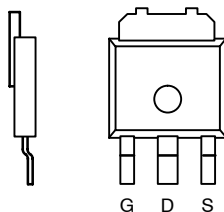
PRODUCT SUMMARY			
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a, e</sup>	$Q_g$ (Typ)
25	0.0052 @ $V_{GS} = 10$ V	89	30 nC
	0.0076 @ $V_{GS} = 4.5$ V	80	

## FEATURES

- TrenchFET® Power MOSFET
- 100%  $R_g$  Tested
- RoHS Compliant

## APPLICATIONS

- DC/DC Conversion, Low-Side
  - Desktop PC
  - Notebook PC

TO-252  
Reverse Lead DPAK

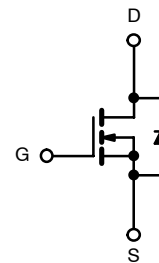
Drain Connected to Tab

Top View

Ordering Information:

SUR50N025-05P—E3 (Lead (Pb)-Free)

SUR50N025-05P-T4—E3 (Lead (Pb)-Free, alternate tape orientation)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	89 <sup>a, e</sup>
		$T_C = 70^\circ\text{C}$	75 <sup>a, e</sup>
		$T_A = 25^\circ\text{C}$	36 <sup>b, c</sup>
		$T_A = 70^\circ\text{C}$	30 <sup>b, c</sup>
Pulsed Drain Current	$I_{DM}$	100	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	7.7 <sup>b, c</sup>
Avalanche Current Pulse	$I_{AS}$	45	mJ
Single Pulse Avalanche Energy	$E_{AS}$	101	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	83 <sup>a</sup>
		$T_C = 70^\circ\text{C}$	58 <sup>a</sup>
		$T_A = 25^\circ\text{C}$	11.5 <sup>b, c</sup>
		$T_A = 70^\circ\text{C}$	8.0 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	10	13	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{thJC}$	1.5	1.8	

## Notes:

- Based on  $T_C = 25^\circ\text{C}$ .
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  sec
- Maximum under steady state conditions is  $90^\circ\text{C}/\text{W}$ .
- Calculated based on maximum junction temperature. Package limitation current is 50 A.

SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	25			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		20		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			-6.0		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.4		2.4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0042	0.0052	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		0.0062	0.0076	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		65		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 0 V, f = 1 MHz		3600		pF
Output Capacitance	C <sub>oss</sub>			790		
Reverse Transfer Capacitance	C <sub>rss</sub>			430		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		63	95	nC
		V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A		30	45	
Gate-Source Charge	Q <sub>gs</sub>			10.5		
Gate-Drain Charge	Q <sub>gd</sub>		10.5			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.0	1.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 12 V, R <sub>L</sub> = 0.24 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		24	36	ns
Rise Time	t <sub>r</sub>			13	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			24	36	
Fall Time	t <sub>f</sub>			7.5	12	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 12 V, R <sub>L</sub> = 0.24 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		11	17	
Rise Time	t <sub>r</sub>			11	17	
Turn-Off Delay Time	t <sub>d(off)</sub>			29	44	
Fall Time	t <sub>f</sub>			8	12	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			55	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 30 A		0.9	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		34	51	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			25	38	nC
Reverse Recovery Fall Time	t <sub>a</sub>			17		ns
Reverse Recovery Rise Time	t <sub>b</sub>			17		

## Notes

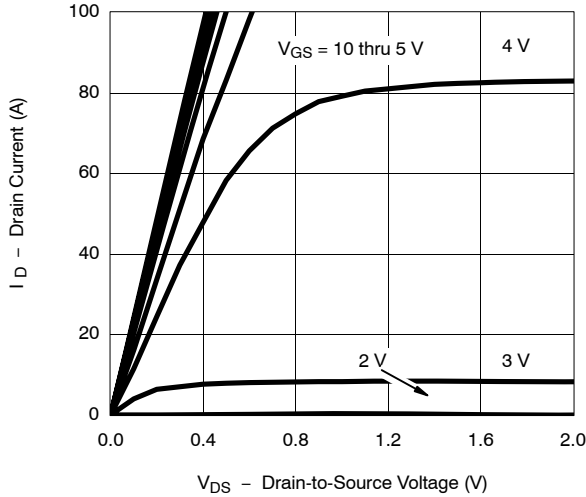
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

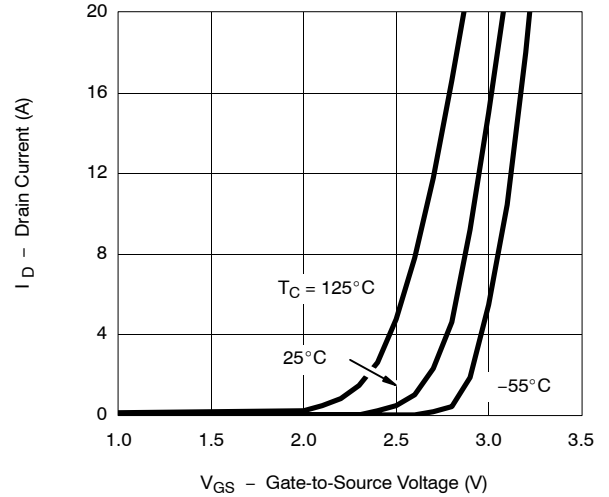


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

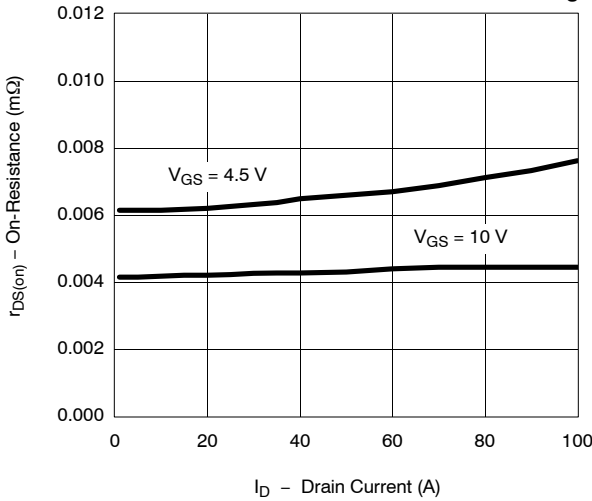
**Output Characteristics**



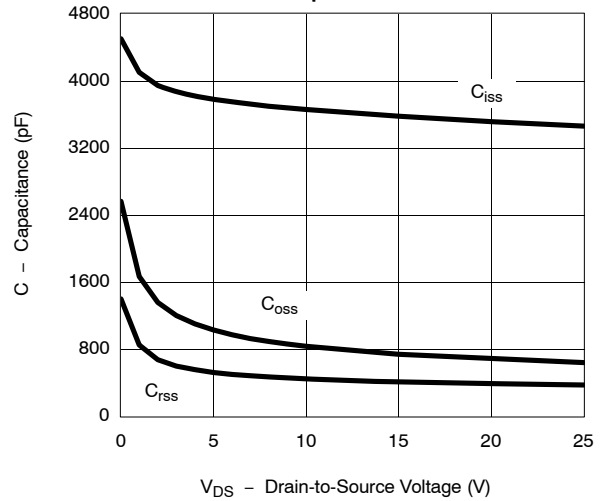
**Transfer Characteristics**



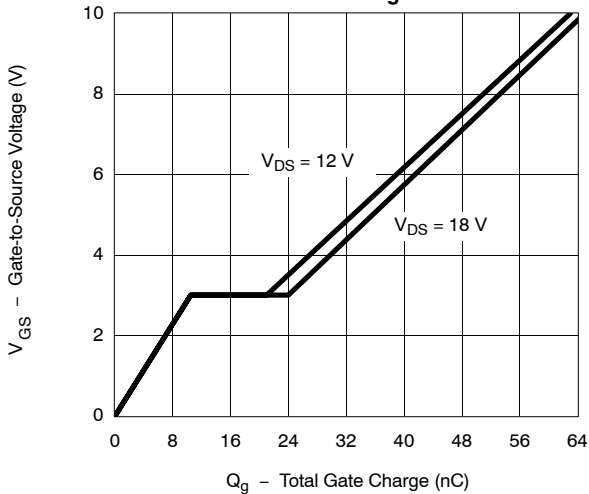
**On-Resistance vs. Drain Current and Gate Voltage**



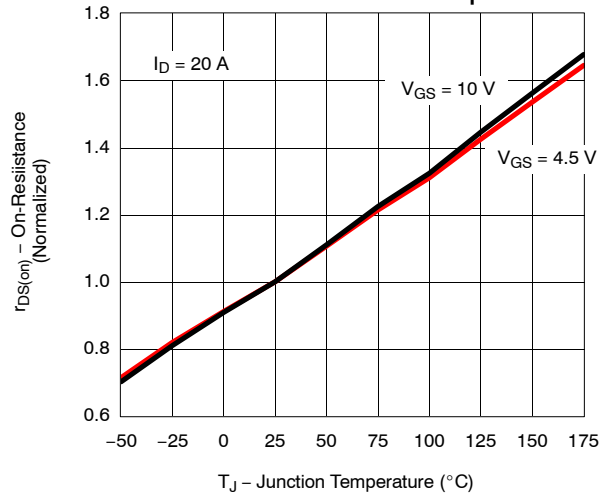
**Capacitance**



**Gate Charge**



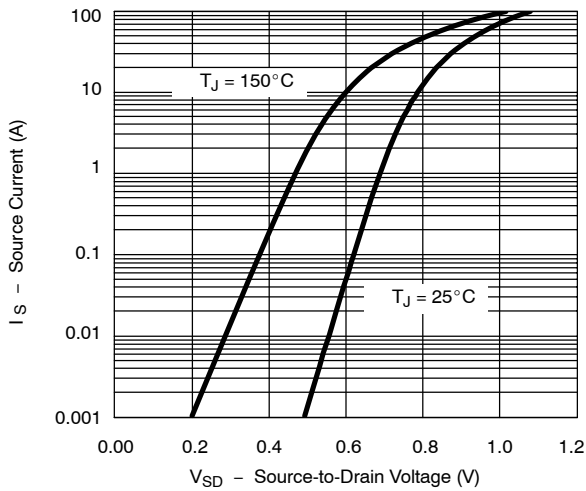
**On-Resistance vs. Junction Temperature**



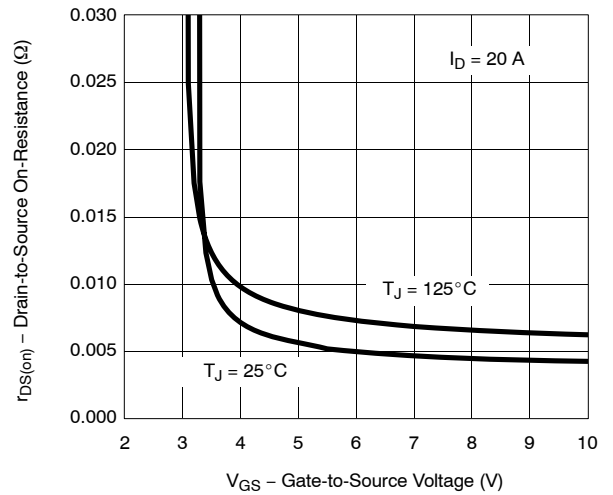


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

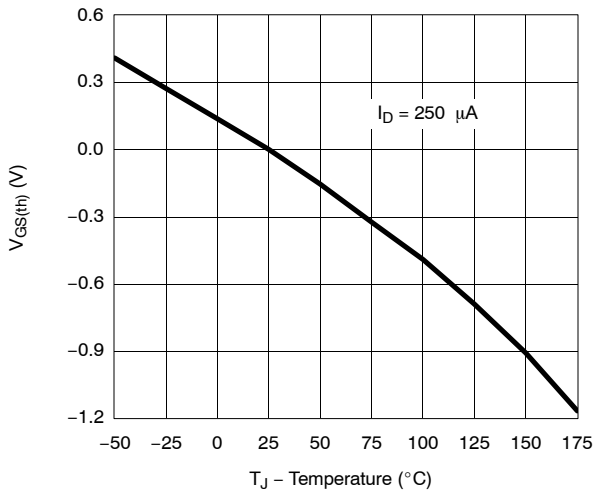
**Source-Drain Diode Forward Voltage**



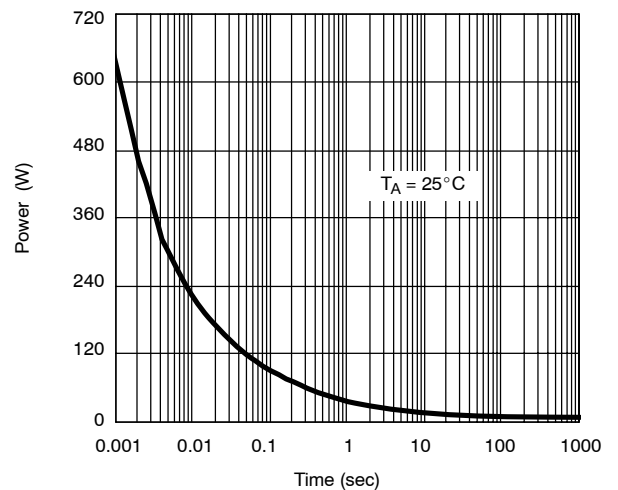
**On-Resistance vs. Gate-to-Source Voltage**



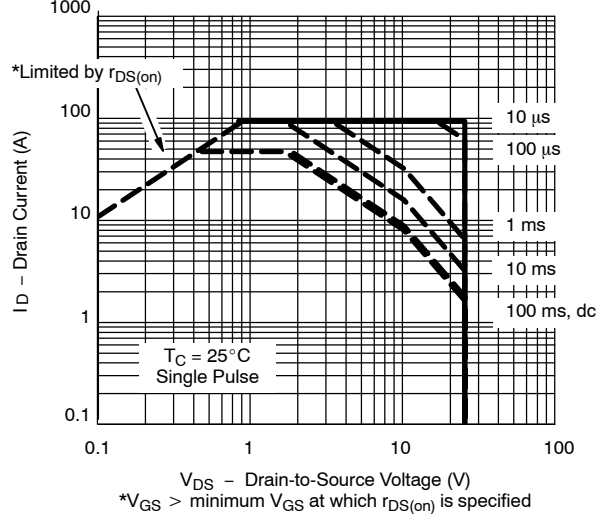
**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



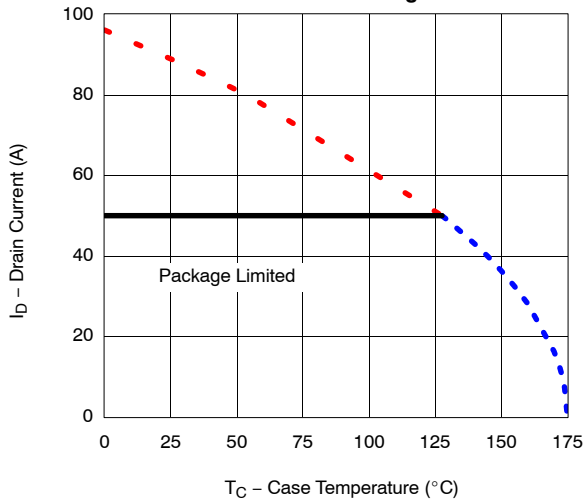
**Safe Operating Area, Junction-to-Case**



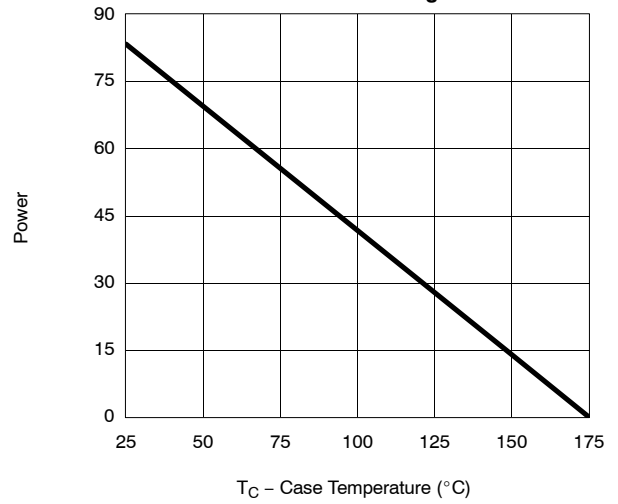


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

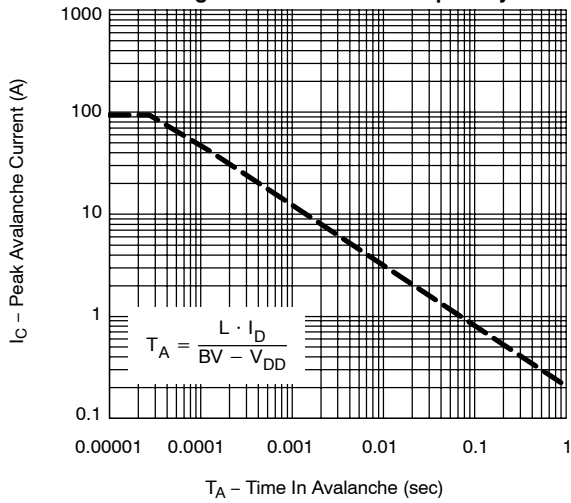
Current De-Rating\*



Power De-Rating



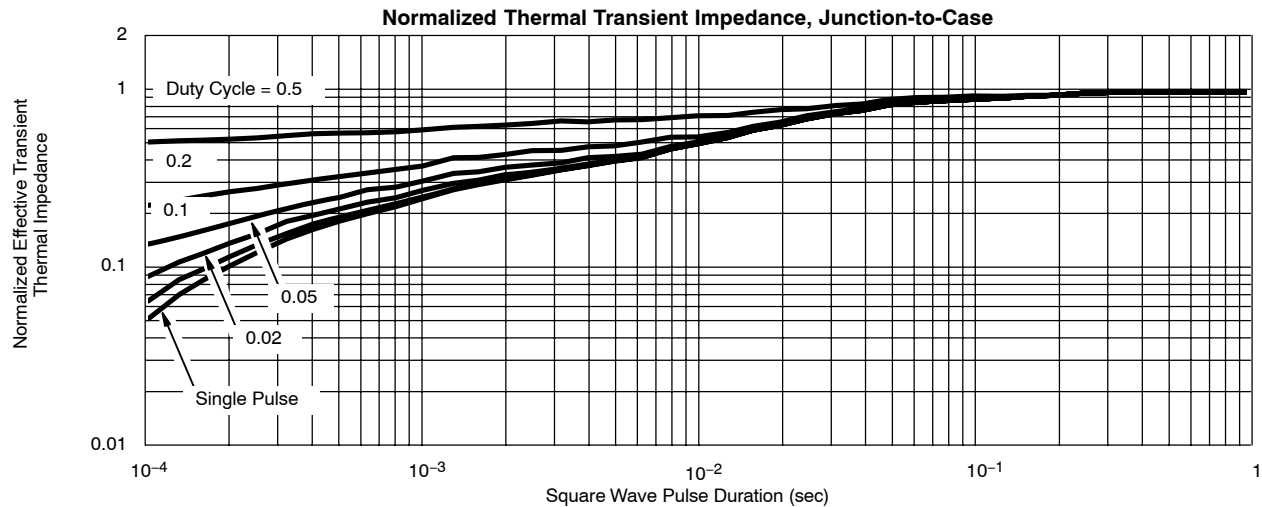
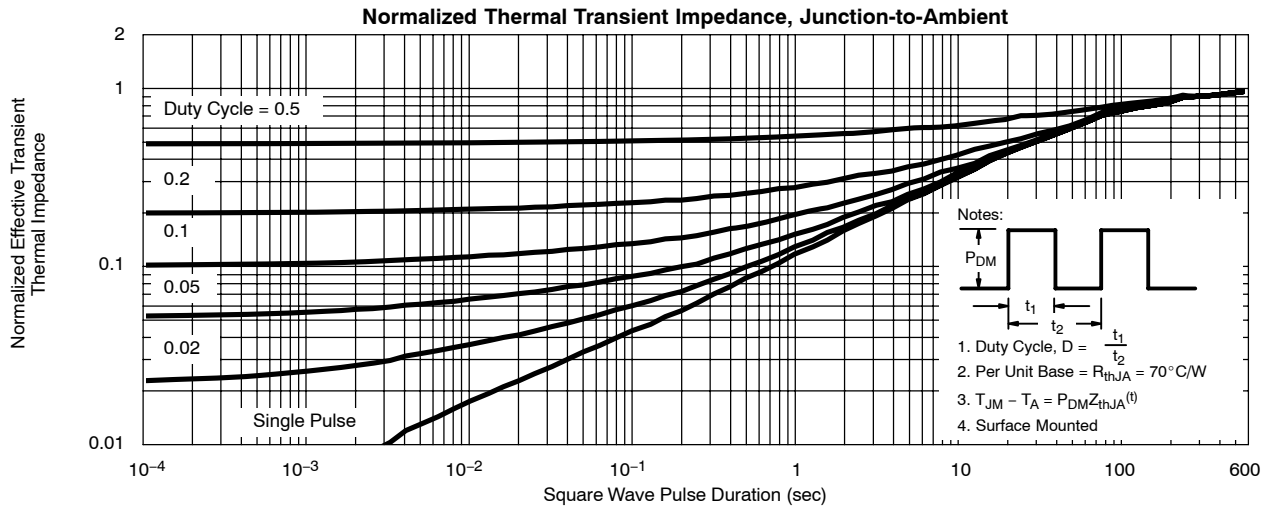
Single Pulse Avalanche Capability



$$T_A = \frac{L \cdot I_D}{BV - V_{DD}}$$

\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



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