

# SRAM

# 32K X 8 LOW POWER CMOS STATIC RAM

## FEATURES

- High speed access time: 50/70/85/100ns
- Power supply current : Operating :35mA(max)  
Standby : 5uA
- Power supply : 2.7V to 3.6V
- Fully static operation – No clock or refreshing required
- All inputs and outputs directly LVTTTL compatible
- Common I/O capability
- Data retention voltage : 1.5V (min)
- Available packages :28-pin SOP ,TSOP-I (8x13.4mm forward type and reverse type).
- Operating temperature :
  - 0 ~ +70 °C
  - -40 ~ +85 °C

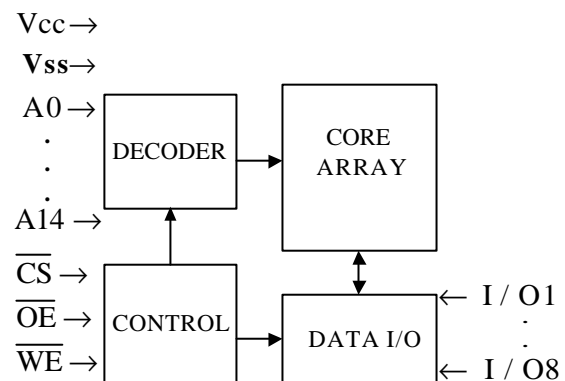
## PART NUMBER EXAMPLES

PART NO.	PACKAGE CODE	Operating Temperature
T15V256A-70D	D=SOP	0 ~ +70 °C
T15V256A-85P	P=	
T15V256A-85R	TSOP-I(Forward)	
	R= TSOP-I(Reverse)	
T15V256A-70DI	D=SOP	-40 ~ +85 °C
T15V256A-85PI	P=	
T15V256A-85RI	TSOP-I(Forward)	
	R= TSOP-I(Reverse)	

## GENERAL DESCRIPTION

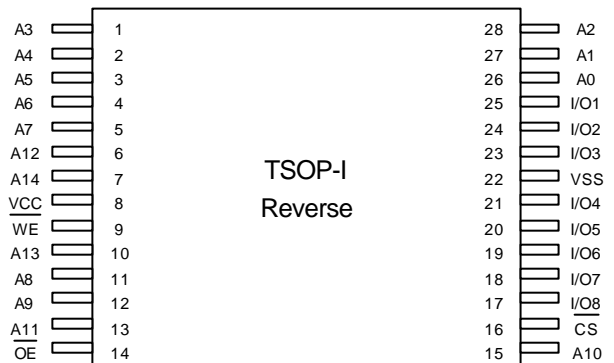
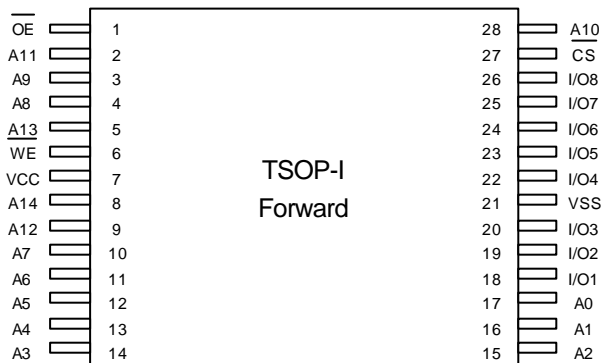
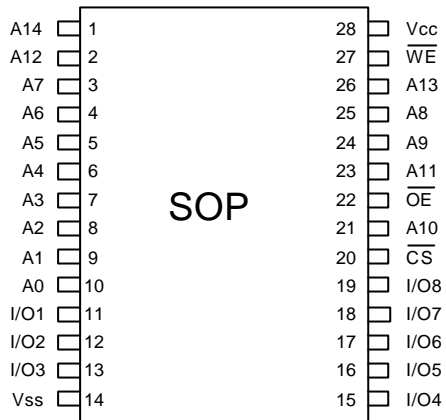
The T15V256A is a low power and low voltage CMOS static RAM. organized as 32,768 x 8 bits that operates on a 2.7V to 3.6V power supply. Data retention is guaranteed at a power supply voltage as low as 1.5V. This device is packaged in a standard 28-pin SOP or TSOP-I forward and reverse type.

## BLOCK DIAGRAM



**PIN CONFIGURATION**

**(Top View)**



**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CS	Chip Select Inputs
WE	Write Enable
OE	Output Enable
Vcc	Power Supply
Vss	Ground

**DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS**

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to + 4.6	V
Inputs to Vss Potential	-0.5 to Vcc +0.5	V
Power Dissipation	0.7	W
Storage Temperature	-60 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	2.7	-	3.6	V
Input Voltage, low	V <sub>IL</sub>	-0.3	-	0.6	V
Input Voltage, high	V <sub>IH</sub>	2.4	-	Vcc+0.3	V
Ambient Temperature	T <sub>A</sub>	0/-40	-	+75/+85	°C

**TRUTH TABLE**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	Power
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Disable	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

**OPERATING CHARACTERISTICS**

(Vcc = 2.7V to 3.6V, Vss = 0V, Ta = 0 ~ +70 °C /-40 to 85°C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Leakage Current	I <sub>LI</sub>	Vin=Vss to Vcc	-	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> =Vss to Vcc, $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-	-	1	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = + 2.1mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 1.0mA	2.2	-	-	V	
Operating Power Supply Current	I <sub>cc</sub>	$\overline{CS} = V_{IL}$ , I/O=0mA Cycle = MIN. Duty = 100%	-50	-	-	35	mA
			-70	-	-	30	mA
			-85	-	-	25	mA
			-100	-	-	20	mA
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS} = V_{IH}$ , Cycle=min, Duty=100%	-	-	0.3	mA	
	I <sub>SBI</sub>	$\overline{CS} \geq V_{cc}-0.2V$	-	-	5	uA	

**CAPACITANCE**

(V<sub>CC</sub> = 2.7V to 3.6V, T<sub>a</sub> = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/ Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

**Note:** These parameters are sampled but not 100% tested.

**AC TEST CONDITIONS**

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.4V
Output Load	See Fig. 1,2

**AC TEST LOADS AND WAVEFORM**

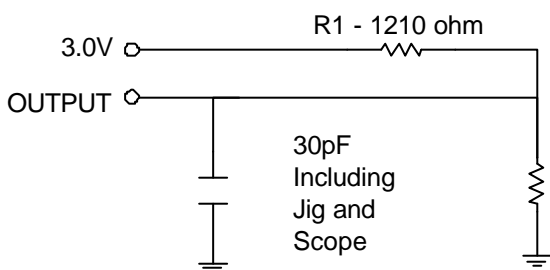
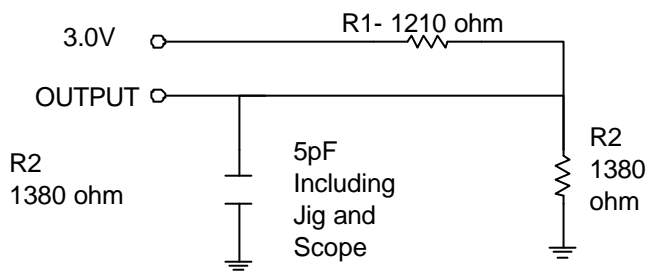


Fig 1



(For T<sub>CLZ</sub> T<sub>OLZ</sub> T<sub>CHZ</sub> T<sub>OHZ</sub> T<sub>WHZ</sub> T<sub>OW</sub>)

Fig 2

**AC CHARACTERISTICS**

 (V<sub>CC</sub>=2.7V to 3.6V, V<sub>SS</sub> = 0V, Ta = 0 ~ +70 °C /-40 to 85°C)

**(1) READ CYCLE**

PARAMETER	SYM.	-50ns		-70ns		-85ns		-100ns		UNIT
		MIN	MAX	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	tRC	50	-	70	-	85	-	100	-	ns
Address Access Time	tAA	-	50	-	70	-	85	-	100	ns
Chip Select Access Time	tACS	-	50	-	70	-	85	-	100	ns
Output Enable to Output Valid	tAOE	-	25	-	35	-	40	-	50	ns
Chip Selection to Output in Low Z	tCLZ*	7	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	tOLZ*	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	tCHZ*	-	20	-	25	-	30	-	30	ns
Output Disable to Output in High Z	tOHZ*	-	20	-	25	-	30	-	30	ns
Output Hold from Address Change	tOH	10	-	10	-	10	-	10	-	ns

\* These parameters are measured with 5pF test load.

**(2)WRITE CYCLE**

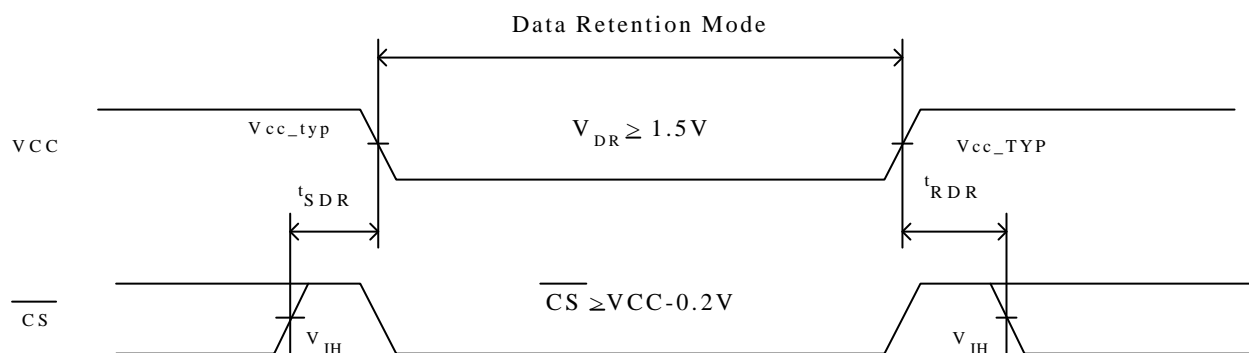
PARAMETER	SYM.	-50ns		-70ns		-85ns		-100ns		UNIT
		MIN	MAX	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	tWC	50	-	70	-	85	-	100	-	ns
Chip Selection to End of Write	tCW	40	-	60	-	70	-	80	-	ns
Address Valid to End of Write	tAW	40	-	60	-	70	-	80	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Write Pulse Width	tWP	30	-	50	-	60	-	70	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Data Valid to End of Write	tDW	25	-	30	-	35	-	40	-	ns
Data Hold from End of Write	tDH	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	tWHZ*	-	20	-	25	-	30	-	30	ns
Output Active from End of Write	tOW	5	-	5	-	5	-	5	-	ns

\* These parameters are measured with 5pF test load.

**DATA RETENTION CHARACTERISTICS**

Item	Symbol	Test Condition	Min	Typ	max	unit
Vcc for data retention	V <sub>DR</sub>	$\overline{CS} \approx V_{CC}-0.2V$	1.5	-	3.6	V
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0, \overline{CS} \approx V_{CC}-0.2V$	-		5	uA
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

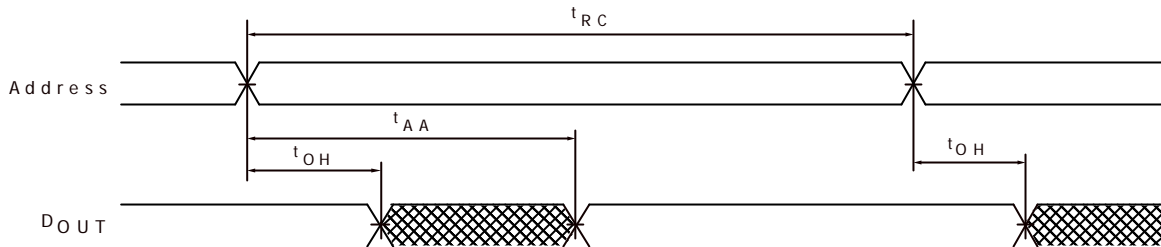
**DATA RETENTION WAVE FORM**



**TIMING WAVEFORMS**

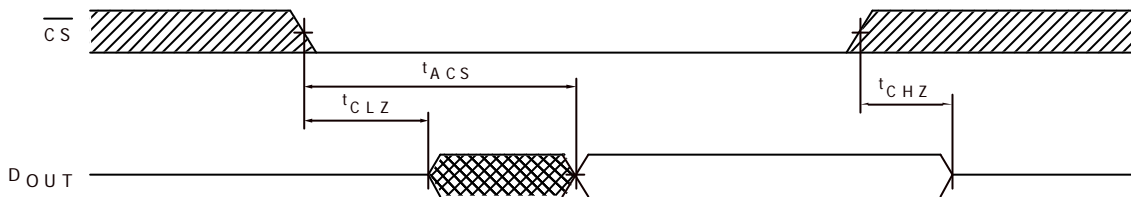
**READ CYCLE 1**

(Address Controlled)



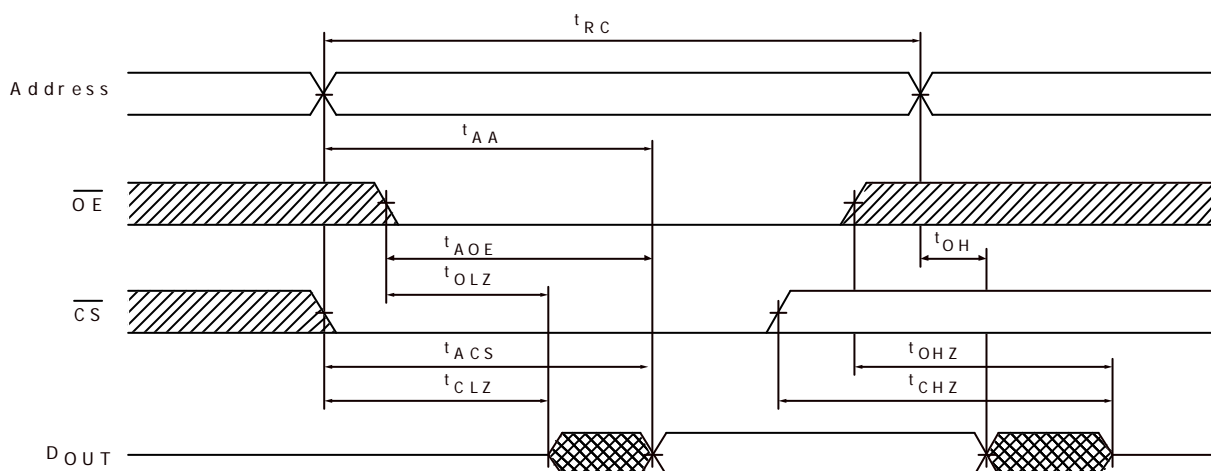
**READ CYCLE 2**



(Chip Select Controlled)



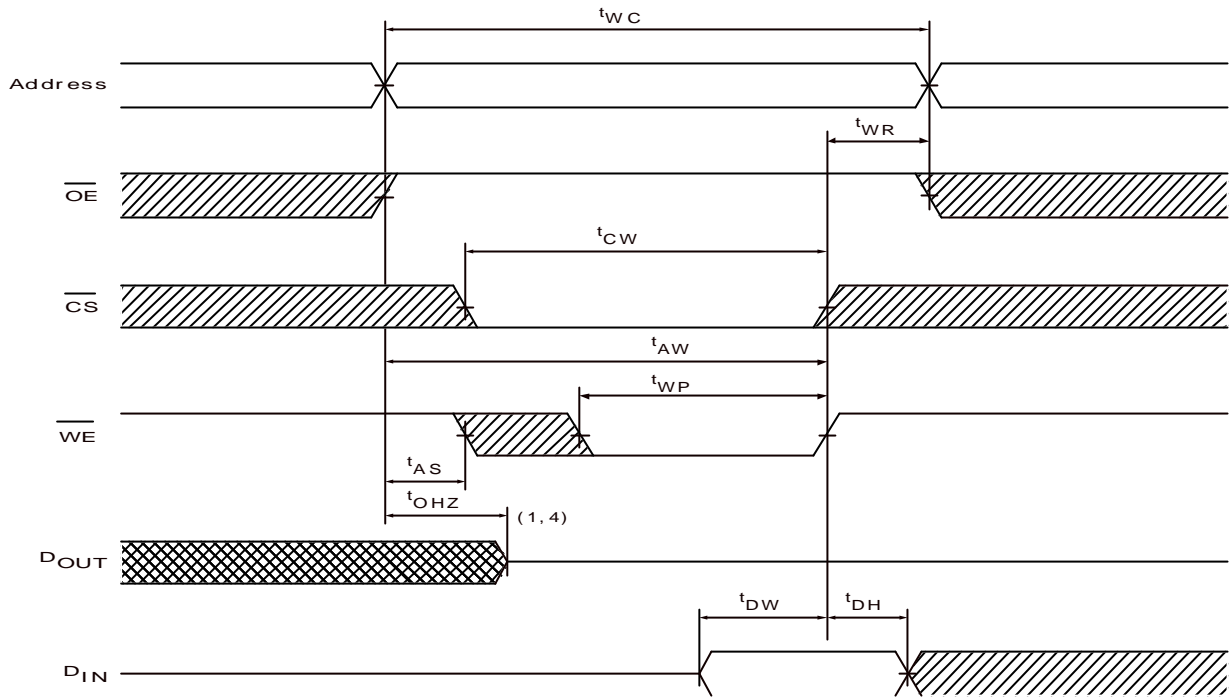
**READ CYCLE 3**

(Output Enable Controlled)

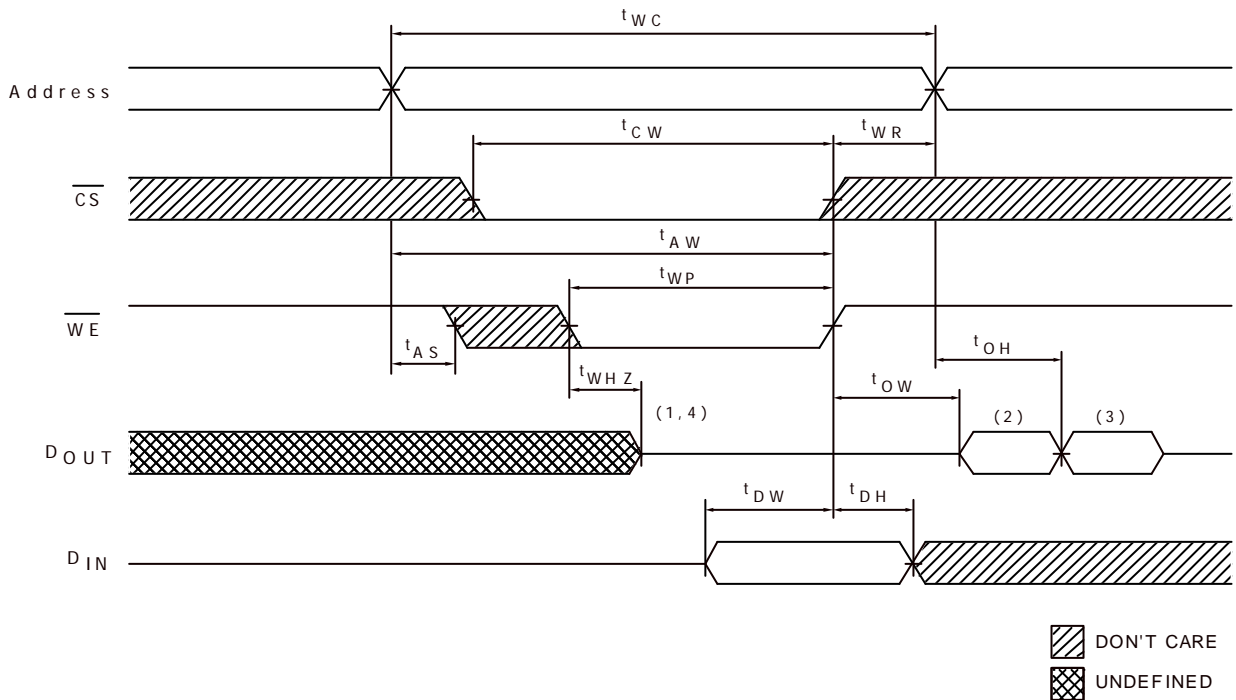


 DON'T CARE  
 UNDEFINED

**WRITE CYCLE 1 ( $\overline{OE}$  CLOCK)**



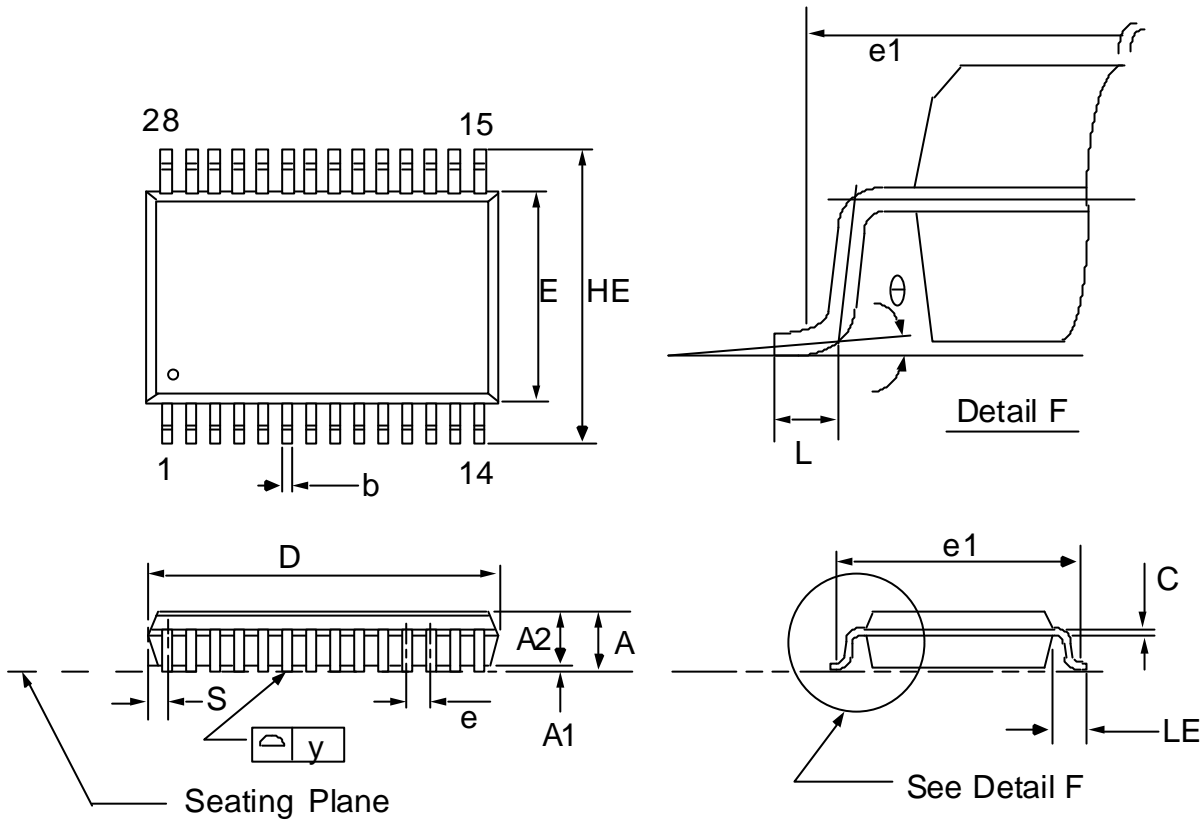
**WRITE CYCLE 2 ( $\overline{OE} = V_{IL}$  Fixed)**





- Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from  $D_{OUT}$  are the same as the data written to  $D_{IN}$  during the write cycle.
  3.  $D_{OUT}$  provides the read data for the next address.
  4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5\text{pF}$ . This parameter is guaranteed but not 100% tested.
  5. If  $\overline{OE}$  is low during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is high during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

**PACKAGE DIMENSIONS**  
**28-LEAD SOP**



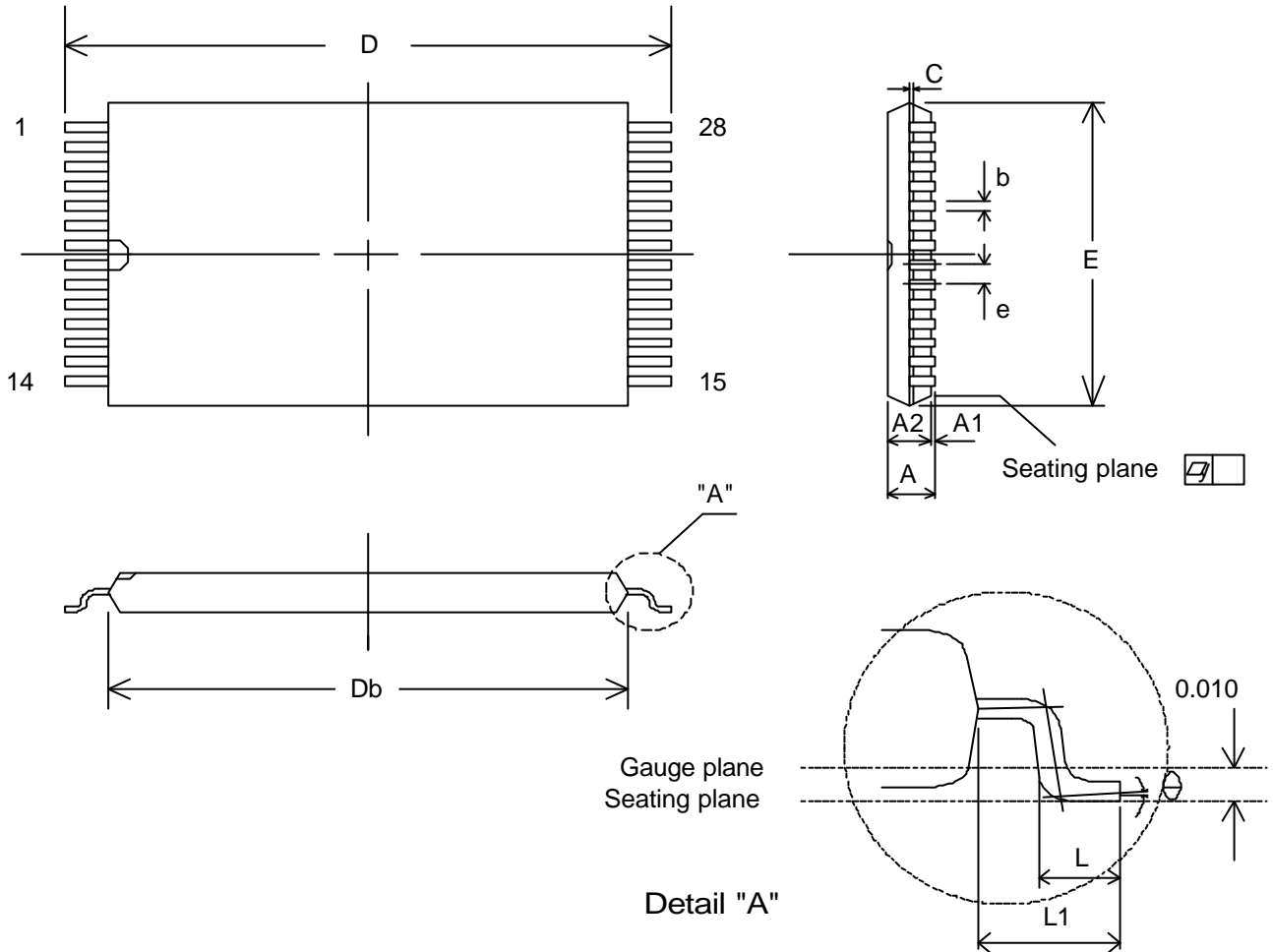
Symbol	Dimension in inches			Dimension in mm		
	min.	typ.	max	min.	typ.	max.
<b>A</b>	-	-	0.098	-	-	2.5
<b>A1</b>	0.01	-	-	0.25	-	-
<b>A2</b>	0.083	0.085	0.087	2.13	2.15	2.17
<b>b</b>	0.014	0.016	0.018	0.39	0.4	0.41
<b>C</b>	0.004	0.006	0.008	0.1	0.15	0.2
<b>D</b>	-	0.713	0.733	-	18.1	18.6
<b>E</b>	0.322	0.331	0.338	8.2	8.4	8.6
<b>e</b>	0.044	0.050	0.056	1.12	1.27	1.42
<b>HE</b>	0.453	0.465	0.476	11.5	11.8	12.1
<b>L</b>	0.026	0.033	0.041	0.65	0.85	1.05
<b>LE</b>	0.047	0.059	0.071	1.2	1.5	1.8
<b>S</b>	-	39	-	-	1.0	-
<b>y</b>	-	-	0.005	-	-	0.12
<b>q</b>	0°	-	10°	0°	-	10°

Notes :

1. Dimensions D max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion / intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. controlling dimension : inches
5. general appearance spec should be based on final visual inspection spec.

**PACKAGE DIMENSIONS**

**28-LEAD TSOP-I FORWARD AND REVERSE (8X13.4mm)**



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max.)	1.20(max.)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.008(typ.)	0.20(typ.)
c	0.006(typ.)	0.15(typ.)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022(typ.)	0.55(typ.)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.004(max.)	0.10(max.)
θ	0°~5°	0°~5°