Features

- 80C52 Compatible
  - 8051 pin and instruction compatible
  - Four 8-bit I/O ports + 2 I/O I2C Interface pins
  - Three 16-bit timer/counters
  - 256 bytes scratch pad RAM
  - 10 Interrupt sources with 4 priority levels
  - Dual Data Pointer
- Variable length MOVX for slow RAM/peripherals
- ISP (In System Programming) using standard V_{CC} power supply.
- Boot ROM contains low level FLASH programming routines and a default serial loader
- High-Speed Architecture
  - 40 MHz in standard mode
  - 20 MHz in X2 mode (6 clocks/machine cycle)
- 32-Kbytes on-chip FLASH program / data Memory
  - Byte and page (128 bytes) erase and write
  - 10k write cycles
  - On-chip 1024 bytes expanded RAM (XRAM)
  - Software selectable size (0, 256, 512, 768, 1024 bytes)
  - 256 bytes selected at reset for T87C51RB2/RC2 compatibility
- Keyboard interrupt interface on port P1
- 400-Kbits/s Multimaster I^2C Interface
- SPI Interface (Master / Slave Mode)
- Sub clock 32kHz crystal oscillator
- 8-bit clock prescaler
- Improved X2 mode with independant selection for CPU and each peripheral
- Programmable Counter Array 5 Channels with:
  - High Speed Output,
  - Compare / Capture,
  - Pulse Width Modulator,
  - Watchdog Timer Capabilities
- Asynchronous port reset
- Full duplex Enhanced UART
- Dedicated Baud Rate Generator for UART
- Low EMI (inhibit ALE)
- Hardware Watchdog Timer (One-time enabled with Reset-Out)
- Power control modes:
  - Idle Mode.
  - Power-down mode.
  - Power-Off Flag.
- Power supply: 4.5V to 5.5V or 2.7V to 3.6V
- Temperature ranges: Commercial (0 to +70°C) and industrial (-40°C to +85°C).
- Packages: PLC44, VQFP44

Description

T89C51IC2 is a high performance FLASH version of the 80C51 8-bit microcontrollers. It contains a 32-Kbytes Flash memory block for program and data.

The 32-Kbytes FLASH memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard V_{CC} pin.

The T89C51IC2 retains all features of the 80C52 with 256 bytes of internal RAM, a 7-source 4-level interrupt controller and three timer/counters.

8-bit Microcontroller with Flash and I^2C Interface

T89C51IC2

Summary

Rev. C – 3-Dec-01

In addition, the T89C51IC2 has a 32kHz Subsidiary clock Oscillator, a Programmable Counter Array, an XRAM of 1024 byte, a Hardware Watchdog Timer, a Keyboard Interface, a I2C Interface, a SPI Interface, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 mode).

The fully static design of the T89C51IC2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

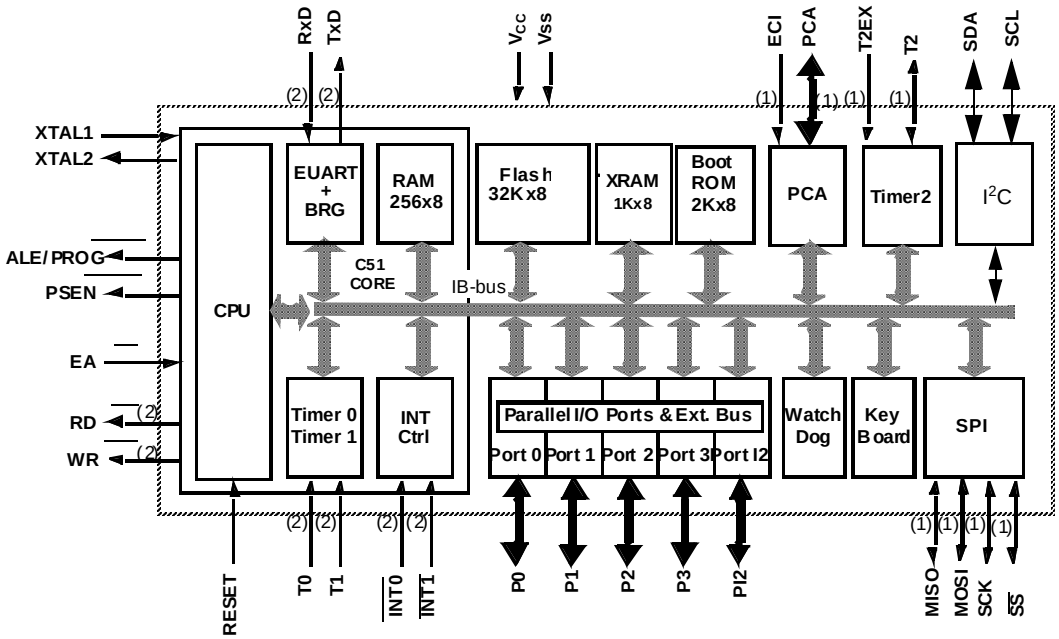
The T89C51IC2 has 2 software-selectable modes of reduced activity and 8 bit clock prescaler for further reduction in power consumption. In the Idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

The added features of the T89C51IC2 make it more powerful for applications that need pulse width modulation, high speed I/O and counting capabilities such as alarms, motor control, corded phones, smart card readers.

Table 1. Memory Size

PLCC44 VQFP44 1.4	Flash (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
T89C51IC2	32k	1024	1280	34

Block Diagram



(1): Alternate function of Port 1
(2): Alternate function of Port 3

SFR Mapping

The Special Function Registers (SFRs) of the T89C51IC2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3, PI2
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- PCA (Programmable Counter Array) registers: CCON, CCAPMx, CL, CH, CCAPxH, CCAPxL (x: 0 to 4)
- Power and clock control registers: PCON
- Hardware Watchdog Timer registers: WDTRST, WDTPRG
- Interrupt system registers: IE0, IPL0, IPH0, IE1, IPL1, IPH1
- Keyboard Interface registers: KBE, KBF, KBLS
- SPI registers: SPCON, SPSTR, SPDAT
- I2C Interface registers: SSCON, SSCS, SSDAT, SSADR
- BRG (Baud Rate Generator) registers: BRL, BDRCON
- Flash register: FCON
- Clock Prescaler register: CKRL
- 32Khz Sub Clock Oscillator registers: CKSEL, OSSCON
- Others: AUXR, AUXR1, CKCON0, CKCON1

Table 2. SFR mapping

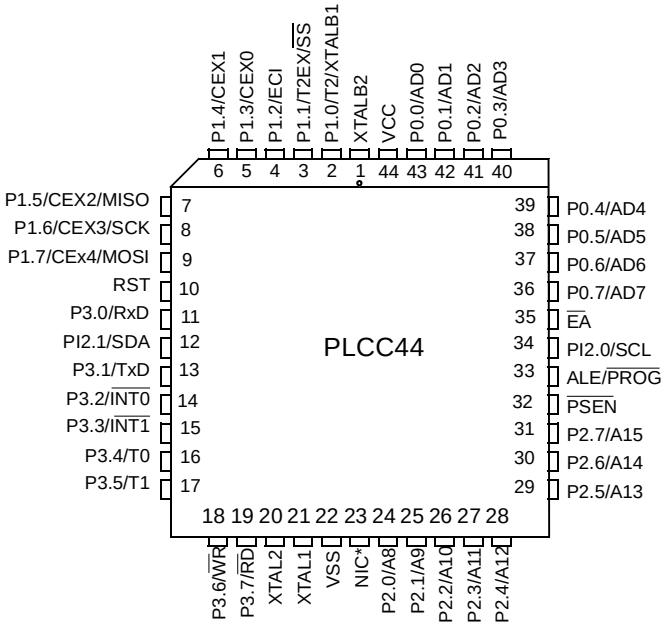
Table below shows all SFRs with their address and their reset value.

	Bit addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON (1) XXXX 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	PI2 bit addressable XXXX XX11			SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX			C7h
B8h	IPL0 X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111	IE1 XXXX X000	IPL1 XXXX X000	IPH1 XXXX X111				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000						CKCON1 XXXX XXX0	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111			SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110	CKRL 1111 1111	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 0000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL XXXX XXX0	OSSCON XXXX X001	PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

(1) FCON access is reserved for the FLASH API and ISP software.

Pin Configurations



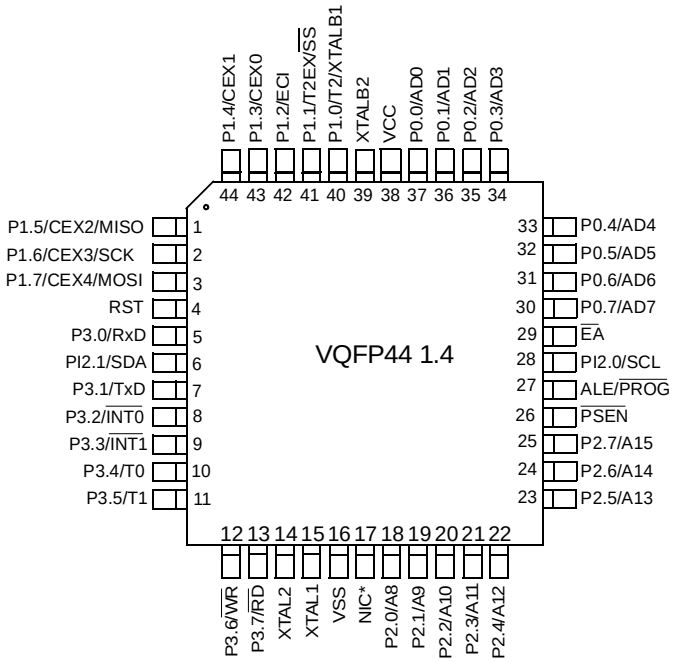


Table 1. Pin Description for 40/44 pin packages

Mnemonic	Pin Number		Type	Name and Function
	PLCC44	VQFP44 1.4		
V_{SS}	22	16	I	**Ground:** 0V reference
V_{CC}	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 must be polarized to V_{CC} or V_{SS} in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for T89C51IC2 Port 1 include:
	2	40	I/O	**P1.0**: Input / Output
			I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
			I	**XTALB1 (P1.0):** Sub Clock input to the inverting oscillator amplifier
	3	41	I/O	**P1.1:** Input / Output
			I	**T2EX:** Timer/Counter 2 Reload/Capture/Direction Control
			I	**$\overline{SS}$:** SPI Slave Select
	4	42	I/O	**P1.2:** Input / Output
			I	**ECI:** External Clock for the PCA
	5	43	I/O	**P1.3:** Input / Output
			I/O	**CEX0:** Capture/Compare External I/O for PCA module 0
	6	44	I/O	**P1.4:** Input / Output
			I/O	**CEX1:** Capture/Compare External I/O for PCA module 1
	7	1	I/O	**P1.5:** Input / Output
			I/O	**CEX2:** Capture/Compare External I/O for PCA module 2
			I/O	**MISO:** SPI Master Input Slave Output line When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.
	8	2	I/O	**P1.6:** Input / Output
			I/O	**CEX3:** Capture/Compare External I/O for PCA module 3
			I/O	**SCK:** SPI Serial Clock **SCK outputs clock to the slave peripheral**
	9	3	I/O	**P1.7:** Input / Output:

Mnemonic	Pin Number		Type	Name and Function
	PLCC44	VQFP44 1.4		
			I/O	**CEX4:** Capture/Compare External I/O for PCA module 4
			I/O	**MOSI:** SPI Master Output Slave Input line When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.
XTALA1	21	15	I	**Crystal A 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTALA2	20	14	O	**Crystal A 2:** Output from the inverting oscillator amplifier
XTALB1	2	40	I	**Crystal B 1: (**Sub Clock) Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTALB2	1	39	O	**Crystal B 2:** (Sub Clock) Output from the inverting oscillator amplifier
P2.0-P2.7	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for 16Kb devices P2.0 to P2.6 for 32Kb devices
P3.0-P3.7	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	11	5	I	**RXD (P3.0):** Serial input port
	13	7	O	**TXD (P3.1):** Serial output port
	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	16	10	I	**T0 (P3.4):** Timer 0 external input
	17	11	I	**T1 (P3.5):** Timer 1 external input
	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
PI2.0-PI2.1	34, 12	28, 6		**Port I2:** Port I2 is an open drain. It can be used as inputs (must be polarized to Vcc with external resistor to prevent any parasitic current consumption).
	34	28	I/O	**SCL (PI2.0): I2C Serial Clock** SCL output the serial clock to slave peripherals SCL input the serial clock from master
	12	6	I/O	**SDA (PI2.1): I2C Serial Data** SDA is the bidirectional I2C data line

Mnemonic	Pin Number		Type	Name and Function
	PLCC44	VQFP44 1.4		
RST	10	4	I/O	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}. This pin is an output when the hardware watchdog forces a system reset.
ALE/$\overline{PROG}$	33	27	O (I)	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	32	26	O	**Program Strobe ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
EA	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH (RD). If security level 1 is programmed, $\overline{EA}$ will be internally latched on Reset.

Ordering Information

Table 2. Possible order entries

Part Number	Flash Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
T89C51IC2-SLSCM	32 Kbytes	5V	Commercial	20 MHz	PLCC44	Stick
T89C51IC2-SLSIM	32 Kbytes	5V	Industrial	20 MHz	PLCC44	Stick
T89C51IC2-SLSIL	32 Kbytes	3V	Industrial	20 MHz	PLCC44	Stick
T89C51IC2-RLTIM	32 Kbytes	5V	Industrial	20 MHz	VQFP44	Tray
T89C51IC2-RLTIL	32 Kbytes	3V	Commercial	20 MHz	VQFP44	Tray

Note: Purchase of Atmel I^2C components conveys a license under the Philips I^2C Patent's right to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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