Test Board for chip evaluation and Layout recommendations

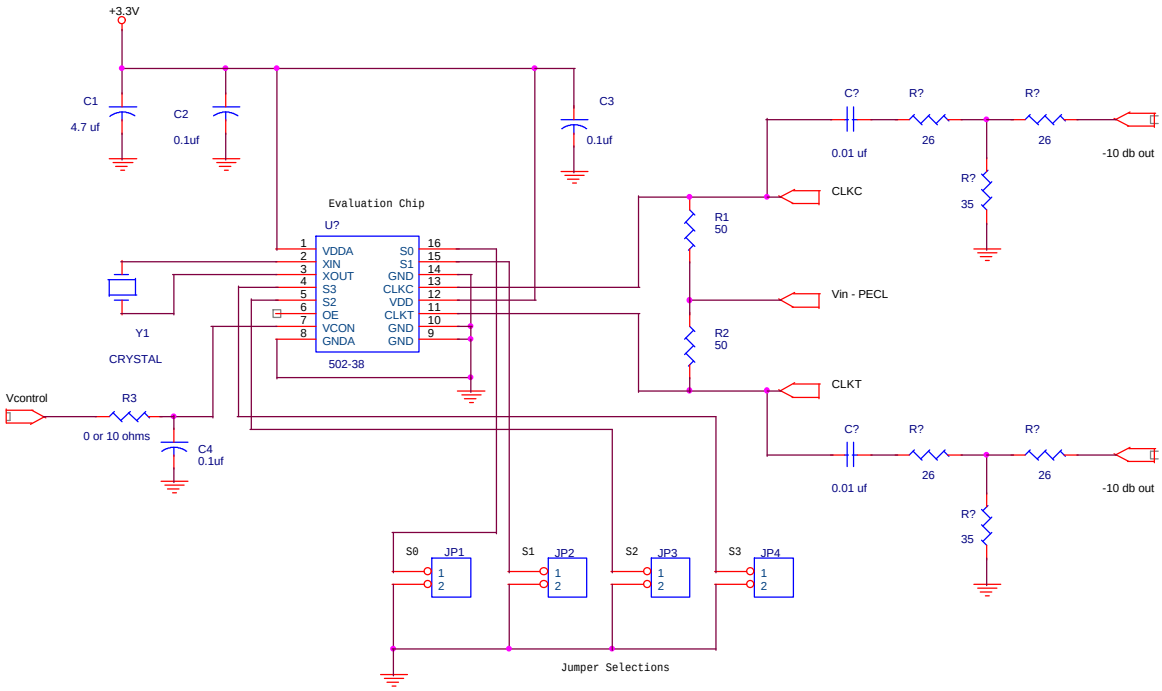
A generic test board for the PLL502-3x and PLL520-0x/-1x/-2x/-3x/-4x/-7x

In order to provide an example of recommended layout for PLL502-3x and PLL520-xx products, PhaseLink provides a generic test board for these parts. Test boards are available for both TSSOP and SOIC 16 pin components.

In addition, the test board is designed to simplify the testing of the PLL502-3x and PLL520-xx parts. It includes selection jumpers allowing the user to easily configure the selector pins (connecting them to GND or leaving them unconnected) as necessary. Depending on the parts under evaluation, these selector pins allow the user to enable or disable the phase locked loop, or even select a multiplier value (see the datasheet of each part for details).

General Layout recommendations

While this test board achieves satisfactory decoupling results, best results are achieved when the chip or die are laid out into the final PCB, following the recommendations indicated in the data sheet.



NOTE:

1. For PECL and PECL outputs: 50Ω resistors (R1 and R2) should be installed.
2. For CMOS output: 50Ω resistors (R1 and R2) should be removed.

In particular, it is essential to include decoupling (by-pass) capacitors as close to the chip as possible in order to minimize noise sensitivity from the power-supply and thus achieve best phase noise and jitter performance. The generic test board provides positions for by-pass capacitors (C1, C2, C3) in order to decouple VDD and GND. An additional by-pass capacitor (C4) is provisioned in order to optimize the signal path coming in from Vcontrol.

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1. Selection Jumpers

Four selection jumpers (JP1 to JP4) are present, allowing to easily connect pins 16, 15, 4 and 5 to GND, respectively (jumper on), or likewise to leave them unconnected (jumper off). For simplicity, the board is marked S0 to S3 to identify the jumpers. The correct connection of pins 4, 5 and 15, 16 is indicated on the datasheets.

2. PECL and LVDS output

In order to simplify the testing of LVDS and PECL outputs, the board already includes two 50Ω resistors (R1 and R2) in series between the OUT and OUTB pins. When using PECL, a biasing of voltage of VDD – 2V must be connected at the middle point between R1 and R2.

In addition, the test board provides access to the output clock via probes or coaxial transmission lines.

In case probes are used, care must be taken to use very low capacitance probes in order to not deteriorate the output waveform at high frequency. It is recommended to use probes of loading values of 0.7pF or below.

In case transmission lines are used, the test board includes a -10dB attenuation segment before a matched 50Ω micro-stripline. It is recommended to connect the coaxial transmission lines to SMA connectors soldered at the end of the micro-striplines. Transmission lines will provide better phasenoise performance than simple probes.

3. CMOS output

If the parts under evaluation are CMOS outputs, the 50Ω resistors required for PECL and LVDS should be removed.