



## FOUR BANDS DIGITAL CONTROLLED GRAPHIC EQUALIZER

- VOLUME CONTROL IN 0.375dB STEP
- FOUR BANDS STEREO GRAPHIC EQUALIZER
- CENTER FREQUENCY, BANDWIDTH, MAX BOOST/CUT DEFINED BY EXTERNAL COMPONENTS
- $\pm 14$ dB CUT/BOOST CONTROL IN 2dB/STEP
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW DISTORTION
- VERY LOW NOISE AND DC STEPPING BY USE OF A MIXED BIPOLAR/CMOS TECHNOLOGY

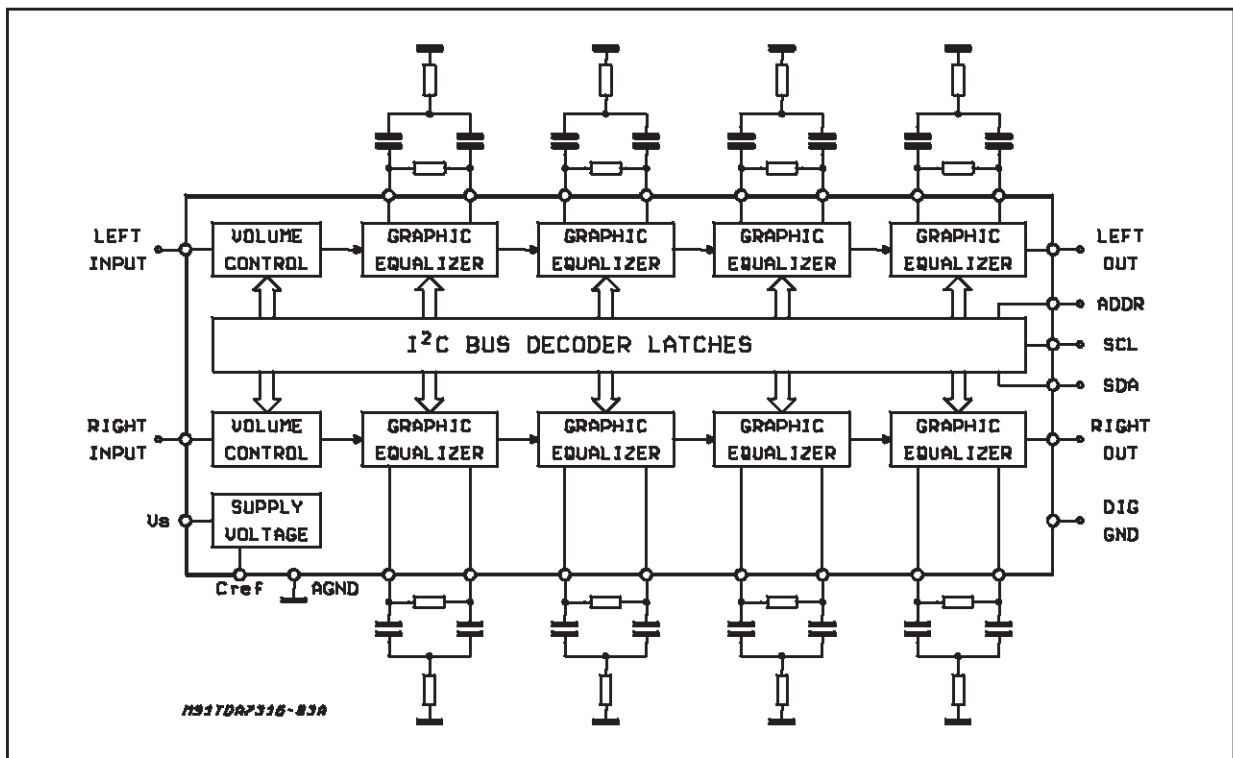


### DESCRIPTION

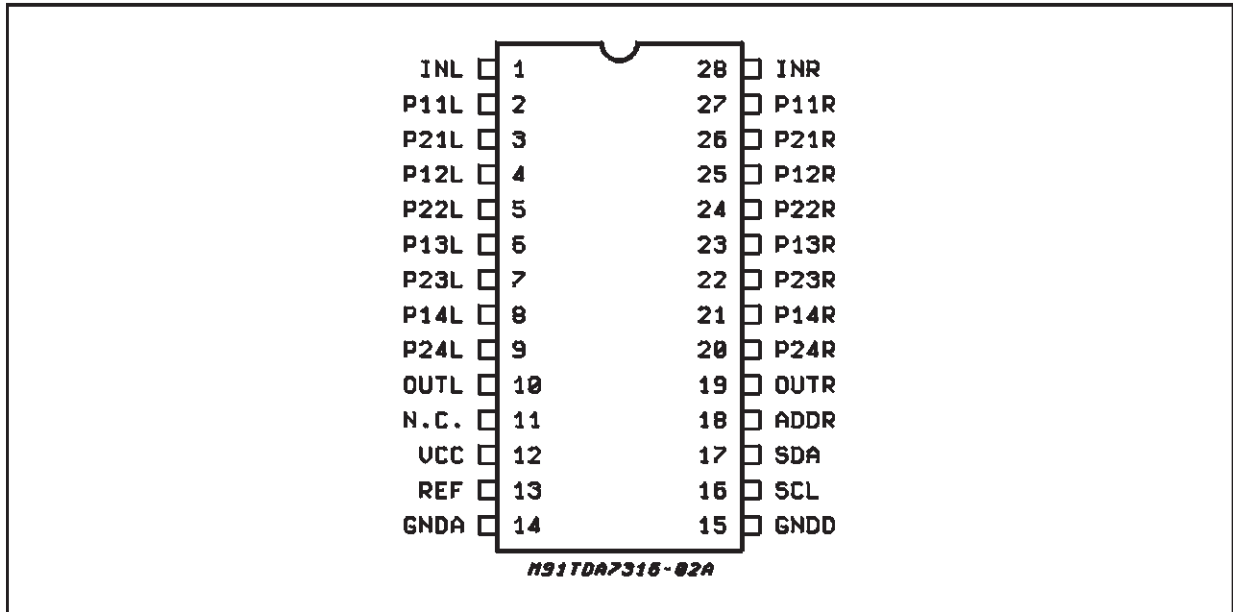
The TDA7316 is a monolithic, digitally controlled graphic equalizer realized in BiCMOS mixed technology. The stereo signal, before any filtering, can be at-

tenuated down to  $-17.625$ dB in 0.375dB step. All the functions can be programmed via serial bus making easy to build a  $\mu$ P controlled system. Signal path is designed for very low noise and distortion.

### BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	Supply Voltage	10.2	V
$T_{op}$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-55 to +150	°C
$R_{tjvins}$	Thermal Resistance Junction pins	max 85	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}C$ ,  $V_S = 9V$ ,  $R_L = 10K\Omega$ ,  $R_g = 600\Omega$ ,  $f = 1KHz$   $V_{IN} = 1V_{rms}$ , all controls in flat position ( $AV = 0dB$ ) unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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SUPPLY

$V_S$	Supply Voltage		6	9	10	V
$I_S$	Supply Current		8	14	20	mA
SVR	Ripple Rejection		60	80		dB

## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT						
$R_I$	Input Resistance		20	30	40	K $\Omega$
$V_{IN\ max}$	Max Input Signal	THD = 0.3%	2.0	2.5		$V_{RMS}$
$IN_S$	Input Separation (1)		80	100		dB

## VOLUME CONTROL

$C_{RANGE}$	Control Range			17.625		dB
$A_{V\ MIN}$	Min. Attenuation		-0.5	0	0.5	dB
$A_{V\ MAX}$	Max. Attenuation		16.7	17.625	18.6	dB
$A_{STEP}$	Step Resolution		0.175	0.375	0.575	dB
$E_A$	Attenuation Set Error		-1.0		1	dB
$E_T$	Tracking Error				0.5	dB
$V_{DC}$	DC Steps	adjacent attenuation steps		0	3.0	mV

## GRAPHIC EQUALIZER

THD	Distortion			0.01	0.1	%
$C_s$	Channel Separation		80	100		dB
$e_{NO}$	Output Noise	BW = 20Hz to 20KHz flat, $A_V = 0dB$		8	20	$\mu V$
		A curve		6		$\mu V$
		BW = 20Hz to 20KHz $A_V = 0dB$ All bands = max. boost All bands = max. cut		24 6		$\mu V$ $\mu V$
S/N	Signal to Noise Ratio	$A_V = 0dB; V_{ref} = 1V_{RMS}$		100		dB
$B_{step}$	Step Resolution		1	2	3	dB
$C_{RANGE}$	Control Range	max boost/cut	$\pm 12$	$\pm 14$	$\pm 16$	dB
VDC	DC Steps	Adiacent Control Steps		0.5	3	mV

## AUDIO OUTPUTS

$V_O$	Output Voltage		2	2.5		$V_{RMS}$
$R_L$	Output Load Resistance		2			K $\Omega$
$C_L$	Output Load Capacitance				10	nF
$R_O$	Output Resistance		5	10	20	$\Omega$
$V_{OUT}$	DC Voltage Level		4.2	4.5	4.8	V

## BUS INPUTS

$V_{IL}$	Input Low Voltage				1	V
$V_{IH}$	Input High Voltage		3			V
$I_{IN}$	Input Current		-5		+5	$\mu A$
$V_O$	Output Voltage SDA Acknowledge	$I_O = 1.6mA$			0.4	V

ADDRESS PIN (Internal 50K $\Omega$  pull down resistor)

$V_{IL}$	Input Low Voltage				1	V
$V_{IH}$	Input High Voltage		$V_{CC} - 1V$			V

NOTE1: The selected input is grounded thre the 2.2 $\mu F$  capacitor

**DEVICE DESCRIPTION**

The TDA7316 is a four bands, digitally controlled stereo Graphic Equalizer.

The device is intended for high quality audio application in Hi-Fi, TV and car radio systems where feature like low noise and THD are key factors. A mixed Bipolar Cmos Technology allows:

Cmos analog switches for pop free commutations, high frequency op.amp. (GWB = 10MHz) and high linearity polysilicon resistor for THD = 0.01 (at Vin = 1Vrms) and a S/N ratio of 102dB. The internal Block Diagram is shown on page 1.

The first stage is a volume control. The control range is 0 to -17.625dB with 0.375dBstep.

The very high resolution (0.375dB step) allows the implementation of closed loop amplitude control system completely free from any acoustical effect (stepping variation and pumping effect).

The volume control is followed by a serial four bands equalizer. Each filtering cell is the biquad cell shown in fig. 1

The internal resistor string is fixing the boost/cut value while the buffer makes the Q (quality factor) and central frequency, set by external components, fully independent from the internal resistors. Each filtering cell is realized using only 4 external components (2 capacitors and 2 resistors) allowing a flexible selection of centre frequency fo, Q factor and gain. Here below the basic formulae and the key features of each band pass filter are reported:

- fo = center frequency
- Gv = gain/loss at the center frequency fo
- Gv = 20log(Av)

$$Q = \frac{f_0}{f_2 - f_1}$$

where f2, f1 = 3dB Bandwidth limits.

$$A_v = \frac{(R_2 \cdot C_2) + (R_2 \cdot C_1) + (R_1 \cdot C_1)}{(R_2 \cdot C_1) + (R_2 \cdot C_2)}$$

$$Q = \frac{\sqrt{(R_1 \cdot C_1 \cdot R_2 \cdot C_2)}}{(R_2 \cdot C_1) + (R_2 \cdot C_2)}$$

$$f_0 = \frac{1}{2\pi \cdot \sqrt{(R_1 \cdot R_2 \cdot C_1 \cdot C_2)}}$$

If C1 is fixed, then:

$$C_2 = \frac{Q^2}{A_v - 1 - Q^2} \cdot C_1$$

$$R_2 = \frac{1}{2\pi \cdot C_1 \cdot f_0 \cdot \frac{(A_v - 1) \cdot Q}{(A_v - 1 - Q^2)}}$$

$$R_1 = \frac{(A_v - 1)^2}{A_v - 1 - Q^2} \cdot R_2$$

Likewise, the components values can be determined byfixing one of the other three parameters. Referring to fig. 1 the suggested R2 value should be higher than 2KΩ in order to have a good THD (internal op. amp. current limit).

Viceversa the R1 value should be equal or lower than 51KΩ in order to keep the "click"(DC step) very low.

A typical application is shown by fig. 2

**Fig. 1**

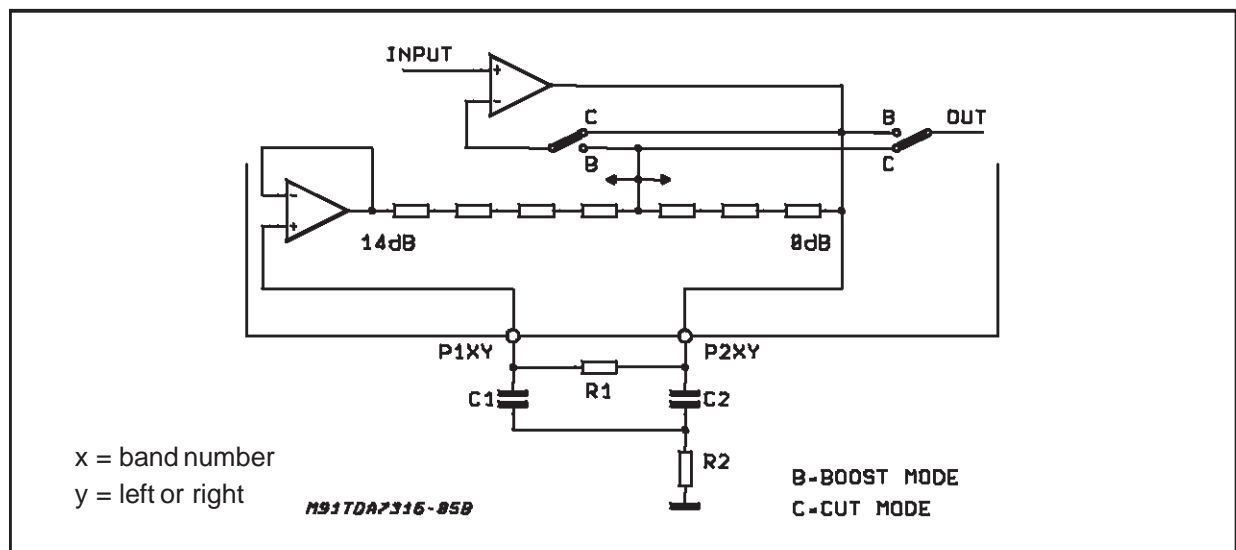
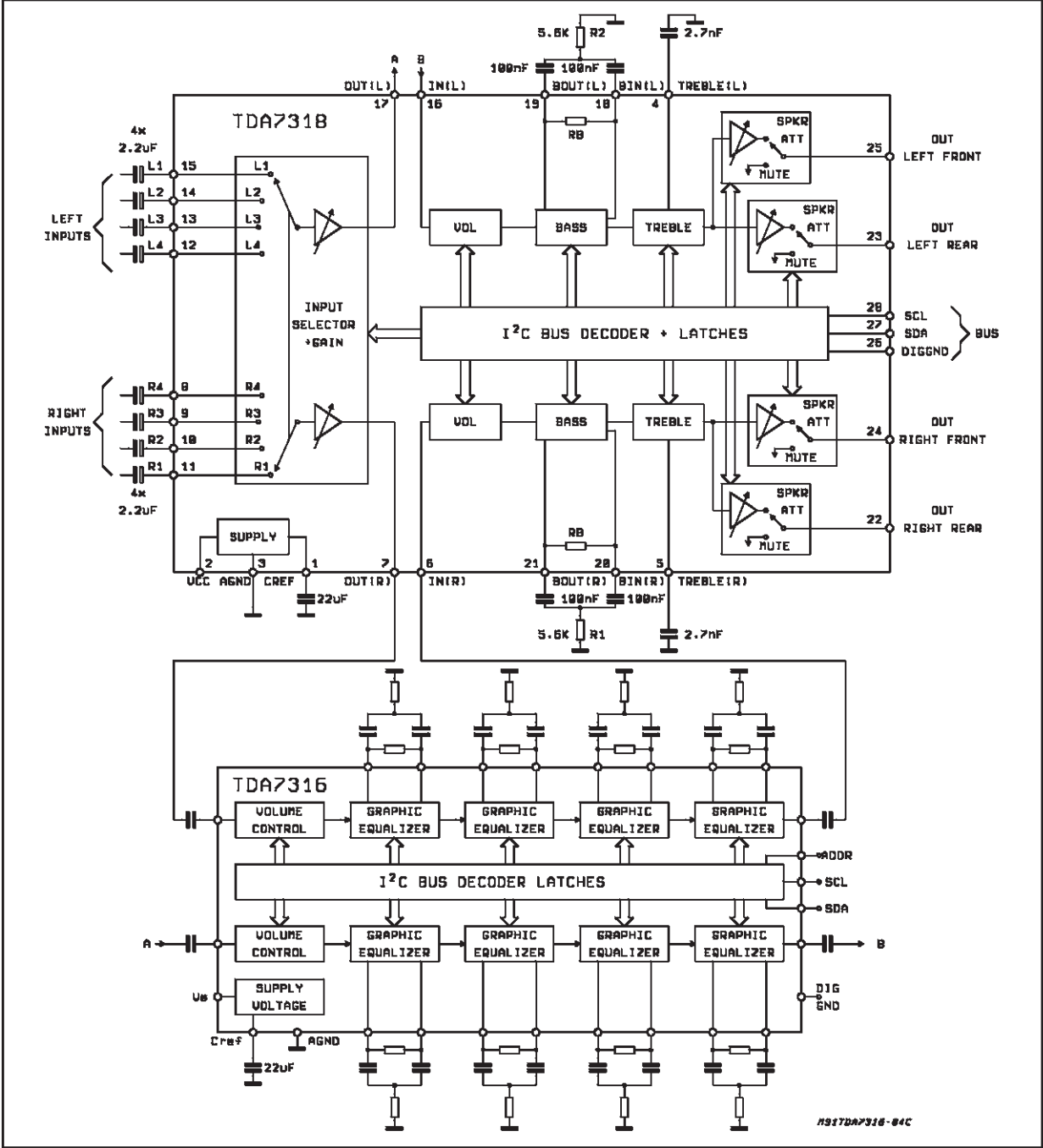


Figure 2: Application Circuit



A five bands graphic equalizer is implemented using the 4 bands of the TDA7316 plus a fifth band obtained from the bass control circuit of the TDA7318 (or another audioprocessor of the SGS-THOMSON 731X family). Applications requiring higher number of external equalizer bands could be implemented by cascading 2 or more TDA7316 devices. In fact the dedicated ADDR pin allows 2 addresses selection. Anyway, the ad-

dress of the graphic equalizer is different from the audioprocessor one. For example, 9 bands are implemented by using of 2 TDA7316 plus an audioprocessor (TDA731X family).

In case one filtering cell is not needed, a short circuit must be provided between the P1xy and P2xy pins.



**I<sup>2</sup>C BUS INTERFACE**

Data transmission from microprocessor to the TDA7316 and viceversa takes place thru the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

**Data Validity**

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

**Start and Stop Conditions**

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

**Byte Format**

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

**Acknowledge**

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

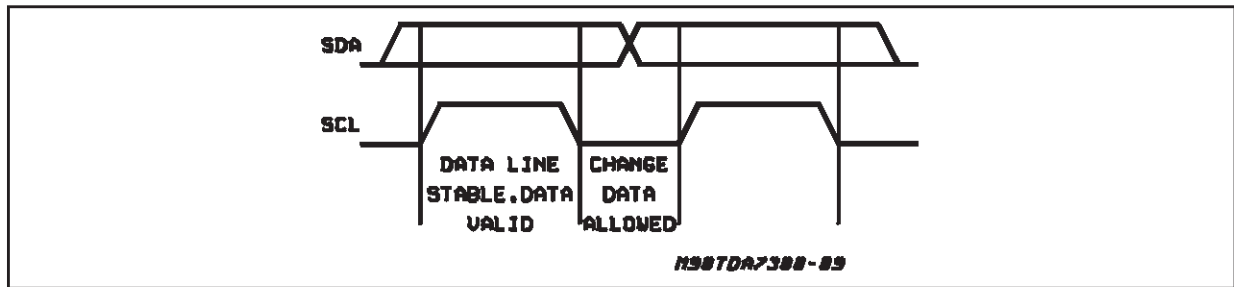
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

**Transmission without Acknowledge**

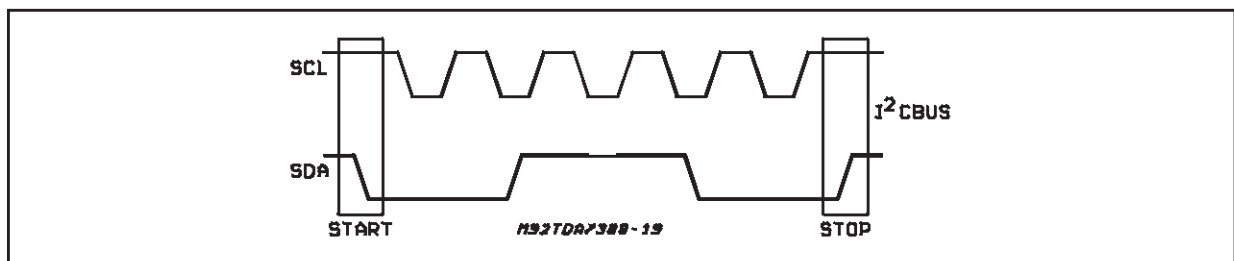
Avoiding to detect the acknowledge of the audioprocessor, the  $\mu$ P can use a simpler transmission: simply it generates the 9th clock pulse without checking the slave acknowledging, and then sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

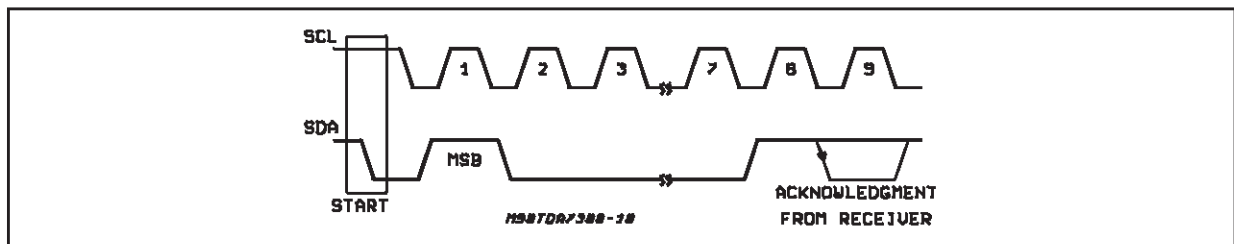
**Figure 3:** Data Validity on the I<sup>2</sup>C BUS



**Figure 4:** Timing Diagram of I<sup>2</sup>C BUS



**Figure 5:** Acknowledge on the I<sup>2</sup>C BUS



**SOFTWARE SPECIFICATION**

**Interface Protocol**

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7316

address (the 8th bit of the byte must be 0). The TDA7316 must always acknowledge at the end of each transmitted byte.

- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge  
 S = Start  
 P = Stop

MAX CLOCK SPEED 100kbits/s

**SOFTWARE SPECIFICATION**

Chip address (84 or 86 Hex)

1	0	0	0	0	1	A	0
MSB							LSB

A = Logic level on pin ADDR  
 A = 1 if ADDR pin = open  
 A = 0 if ADDR pin = connected to ground

**SOFTWARE SPECIFICATION (continued)**

DATA BYTES (detailed description)

**Volume**

MSB					LSB			FUNCTION
0	X	B2	B1	B0	A2	A1	A0	Volume 0.375dB steps
					0	0	0	0
					0	0	1	-0.375
					0	1	0	-0.75
					0	1	1	-1.125
					1	0	0	-1.5
					1	0	1	-1.875
					1	1	0	-2.25
					1	1	1	-2.625
0	X	B2	B1	B0	A2	A1	A0	Volume -3dB steps
		0	0	0				0
		0	0	1				-3
		0	1	0				-6
		0	1	1				-9
		1	0	0				-12
		1	0	1				-15

## TDA7316

### Graphic Equalizer

MSB				LSB			FUNCTION	
1	D3	D2	D1	D0	S2	C1	C0	
	0	0	1					Band 1
	0	1	0					Band 2
	0	1	1					Band 3
	1	0	0					Band 4
	D3	D2	D1	1	C2	C1	C0	cut
	D3	D2	D1	0	C2	C1	C0	Boost
					0	0	0	0dB
					0	0	1	2dB
					0	1	0	4dB
					0	1	1	6dB
					1	0	0	8dB
					1	0	1	10dB
					1	1	0	12dB
					1	1	1	14dB

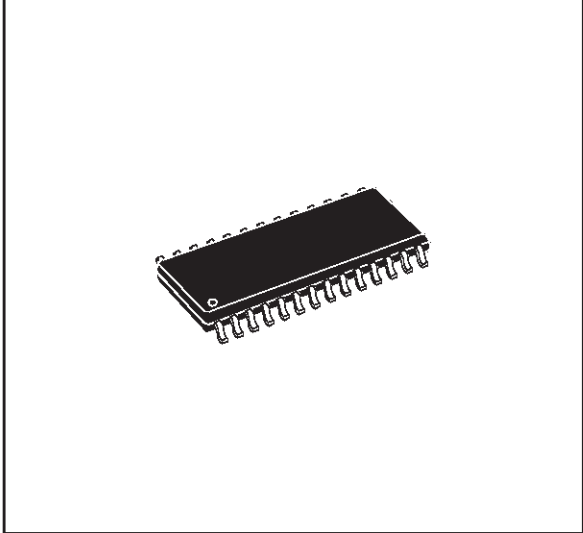
AX = 0.375dB steps, BX = 3dB steps, CX = 2dB steps, X = dont'care

STATUS AFTER POWER-ON RESET	
Volume	-17.25dB
Graphic equalizer bands	-12dB

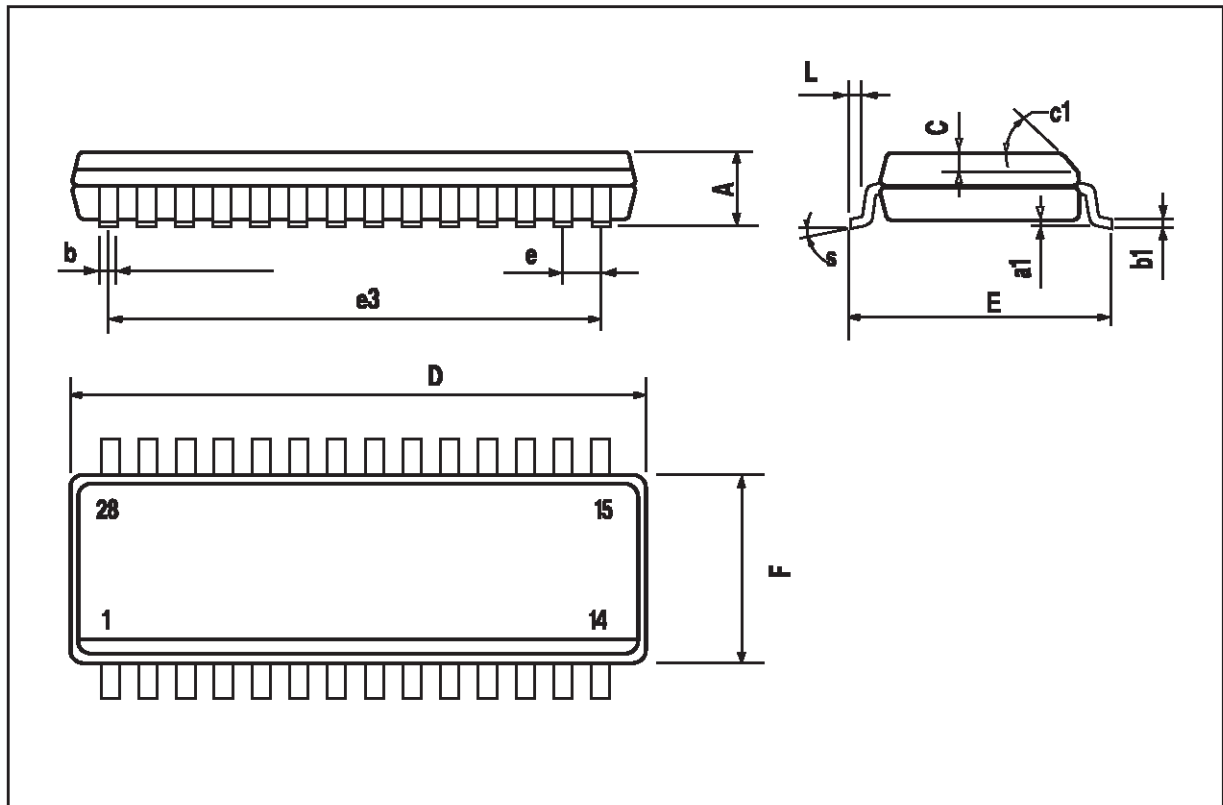


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO28**



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