Melexis
Microelectronic Integrated Systems

TH8082

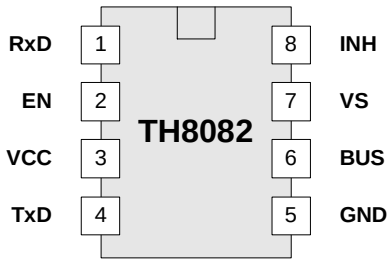
Single LIN Bus Transceiver

Features and Benefits

- Single wire LIN transceiver
- Compatible to LIN Protocol Specification, Rev. 1.1
- Compatible to ISO9141 functions
- Control Output for voltage regulator
- Up to 20 kbps bus speed
- Low RFI due to slew rate control
- Fully integrated receiver filter
- Protection against load dump, jump start
- Bus terminals proof against short-circuits and transients in the automotive environment
- Very low (25 µA) typical power consumption in sleep mode
- Thermal overload and short circuit protection
- High impendance Bus pin in case of loss of ground and undervoltage condition
- ± 4kV ESD protection on bus pin

Pin Diagram

SOIC8NB



Ordering Information

Part No.	***Temperature Range***	***Package***
TH8082 JDC	-40ºC...125ºC	SOIC8, 150mil

General Description

The TH8082 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which use the network. The TH8082 is designed in accordance to the physical layer definition of the LIN Protocol Specification , Rev. 1.2 . The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the TH8082 in the recessive state it's particularly suitable for ECU applications with hard standby current requirements. An advanced sleep mode capability allows a shutdown of the whole application . The included wake-up function detects incoming dominant bus messages and enables the voltage regulator.

Functional Diagram

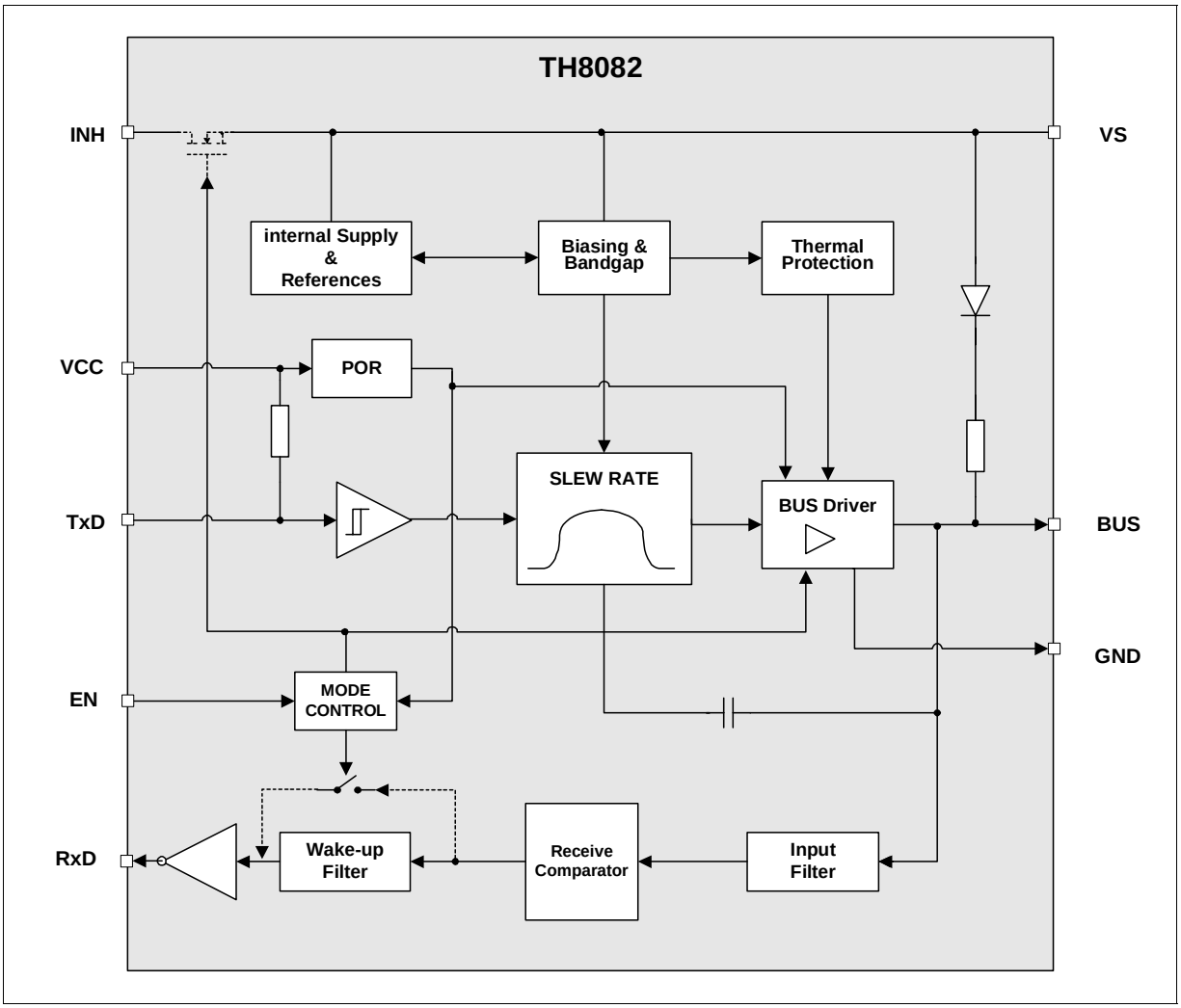


Figure 1 - Block Diagram

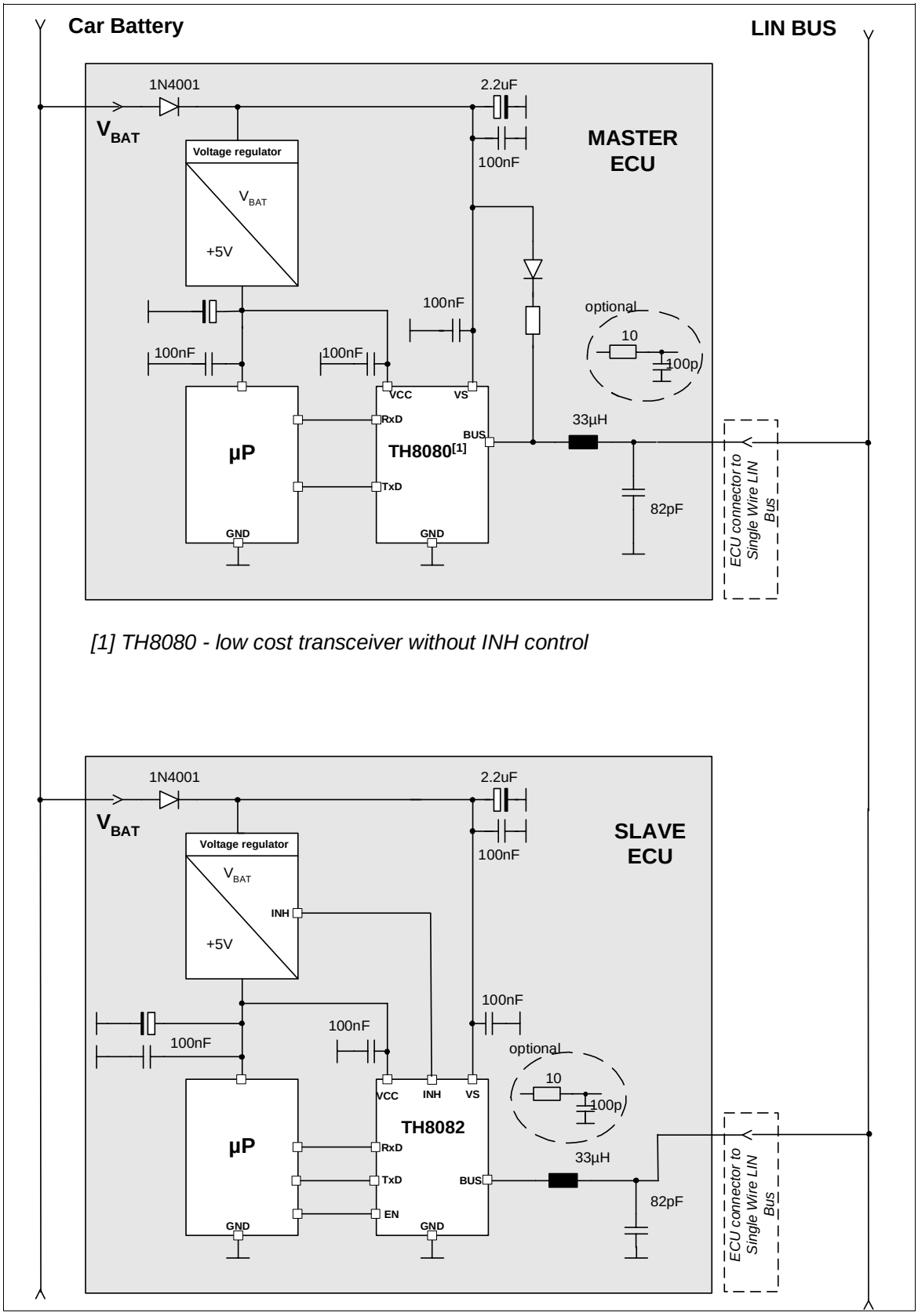
Functional Description

After *power on* the chip automatically enters the *V_{BAT}-stanby mode* . In this intermediate mode the INH output will become HIGH (V_S) and therefore the voltage regulator will provide the V_{CC} - supply . The transceiver will remain the V_{BAT}-stanby mode until the controller sets it to *normal operation* (EN = High) . Only in this mode bus communication is possible. The TH8082 switches itself in the V_{BAT}-stanby mode if V_{CC} is missing or below the threshold.
The *sleep mode* (EN = LOW) can only be reached from normal mode and permits a very low power consumtion because the transceiver and even the external voltage regulator get disabled. If the V_{CC} has been switched off a wake-up request from the bus line will cause the TH8082 to enter the V_{BAT}-stanby mode (V_{CC} is present again) and sets the RxD output to low until the device enters the normal operation mode (active LOW interrupt at RxD). If the INH pin is not connected to the regulator or the inhibitable external regulator is not the one that provides the V_{CC} – supply, the normal mode is directly accessilble by a logic high on the EN pin.
In order to prevent an unintended wake-up caused by disturbances of the automotiv environment incoming dominant signals from the bus have to exceed the wake–up delay time.

Mode Control of TH8082

EN	VCC	Comment	INH	RxD
0	0	V_{BAT}-standby , power on	Vs	0
0	1	V_{BAT}-standby , V_{CC} on , wake up condition after power on	Vs	Active LOW wake-up interrupt
1	1	Normal mode , V_{CC} on	Vs	1 = recessive bus 0 = dominant bus
1	0	V_{BAT}-standby , VCC missing (V_{CC}<V_{CCUV})	Vs	V_{CC}
0	0	Sleep mode, switch to V_{BAT}-standby in case of wake-up request	floating	Active LOW wake-up interrupt if V_{CC} is present
0	1	Sleep mode, regulator not disabled, switch to V_{BAT}-standby in case wake-up request, directly switch to normal mode with EN = 1	floating	Active LOW wake-up interrupt

Application Circuit



[1] TH8080 - low cost transceiver without INH control

Figure 2 - Application Circuit

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8082 is only specified within the limits shown in "Operating conditions".

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_S	6	18	V
Supply voltage	V_{CC}	4.5	5.5	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature [1]	T_{Jc}		+150	°C

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Unit
Batterry Supply Voltage	V_S	t < 1 min	-0.3	+30	V
Supply Voltage	V_{CC}		-0.3	+7	V
Short-term supply voltage	$V_{S.ld}$	Load dump; t<500ms		+40	V
Transient supply voltage	$V_{S.tr1}$	ISO 7637/1 pulse 1[1]	-150		V
Transient supply voltage	$V_{S.tr2}$	ISO 7637/1 pulses 2[1]		+100	V
Transient supply voltage	$V_{S.tr3}$	ISO 7637/1 pulses 3A, 3B	-150	+150	V
BUS voltage	V_{BUS}	t < 500 ms, V_S = 20 V V_S = 20 V	-20 -40	+40	V
Transient bus voltage	$V_{BUS.tr1}$	ISO 7637/1 pulse 1 [2]	-150		V
Transient bus voltage	$V_{BUS.tr2}$	ISO 7637/1 pulses 2 [2]		+100	V
Transient bus voltage	$V_{BUS.tr3}$	ISO 7637/1 pulses 3A, 3B [2]	-150	+150	V
DC voltage on pins TxD, RxD	V_{DC}		-0.3	+7	V
ESD capability of pin BUS	ESD_{BUSHB}	Human body model, equivalent	-4	+4	kV
ESD capability of any other pins	ESD_{HB}	Human body model, equivalent	-2	+2	kV
Maximum latch – up free current at any Pin	I_{LATCH}		-500	+500	mA
Maximum power dissipation	P_{tot}	At T_{amb} = +125 °C		197	mW
Thermal impedance	Θ_{JA}	in free air		152	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

Static Characteristics

(V_S = 6 to 18V, V_{CC}= 4.5 to 5.5V, T_A = -40 to +125°C, unless otherwise specified)
All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PIN VS,VCC						
Supply current, dominant	I_{Sd}	V_S = 18V,V_{CC} = 5.5V, TxD=L			50	µA
Supply current, dominant	I_{CCd}	V_S = 18V,V_{CC} = 5.5V, TxD=L			1	mA
Supply current, recessive	I_{Sr}	V_S = 18V,V_{CC} = 5.5V TxD = H		8	20	µA
Supply current, recessive	I_{CCr}	V_S = 18V,V_{CC} = 5.5V TxD = H		20	30	µA
V_{CC} undervoltage lockout	V_{CC_UV}	EN = H, TxD = L	2.75		4.3	V
Supply current, sleep mode	I_{Ss1}	V_S = 18V,V_{CC} = 0V TxD open		25	50	µA
PIN BUS / TRANSMITTER						
Bus output voltage, dominant	V_{ol_BUS}	TxD=L , I_{BUS} = 40mA,V_S > 7.3V			1.2	V
Bus output voltage, recessive	V_{oh_BUS}	TxD=open	0.8* V_S + 0.7			V
Bus short circuit current	I_{BUS_SHORT}	TxD=L , V_{BUS} > 1.2V, V_S > 7.3V	40		200	mA
Bus input current, recessive	I_{BUS_leakp}	TxD open ,V_{BUS} = Vs	-20		20	µA
Bus reverse polarity curr., rec.	I_{BUS_leakn}	Loss of GND ,V_S =12V, V_{BUS}=0	-1		1	mA
Bus pull up resistor	R_{BUS_pu}	TxD open, V_{BUS}=0	20	30	47	kΩ
PIN BUS / RECEIVER						
Bus input threshold, recessive to dominant	V_{ihBUS_rd}	TxD open , -8V<V_{BUS} < V_{ihBUS_rd}	0.4x V_S	0.45* V_S		V
Bus input threshold, dominant to recessive	V_{ihBUS_rd}	TxD open , V_{ihBUS_rd} <V_{BUS} < 18V		0.55* V_S	0.6*V_S	V
Bus input hysteresis	V_{BUS_hys}		20			mV
PIN TXD, EN						
High level input voltage	V_{ih}	Rising edge			0.7* V_{CC}	V
Low level input voltage	V_{il}	Falling edge	0.3* V_{CC}			V
TxD pull up current, high level	I_{IH_TXD}	V_{TxD} = 4V	-125	-50	-25	µA
TxD pull up current, low level	I_{IL_TXD}	V_{TxD} = 1V	-500	-250	-100	µA
EN pull down current, high level	I_{IH_EN}	V_{EN} = 4V, V_{CC} = 0V	50	125	250	µA
EN pull down current, low level	I_{IL_EN}	V_{EN} = 1V, V_{CC} = 0V	12	25	50	µA

Static Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PIN RXD						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 1.25mA			0.9	V
High level output voltage	V_{oh_rxd}	I_{RxD} = -250µA	V_{CC} -0.9			V
PIN INH						
High level output voltage	V_{oh_INH}	I_{RxD} = -180µA	V_S -0.8V	V_S -0.5V		V
Leakage current	V_{INH_lk}	EN = L, V_{INH} = 0V	-5		5	µA
Thermal protection						
Thermal shutdown	T_{sd}		150		180	°C
Hysteresis	T_{hys}		5		25	°C

Dynamic Characteristics

All dynamic values of the table below refer to the test-schematic schown in Figure - Timing Diagram
$6V \leq V_S \leq 18V$, $-40°C \leq T_A \leq 125°C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slew rate falling edge	t_{SRF}	80% < VBUS < 20% , minimum & maximum bus load	-3	-2	-1	V/µs
Slew rate rising edge	t_{SRR}	20% < VBUS < 80% , minimum bus load [1]	1	2	3	V/µs
Propagation delay transmitter (TxD->BUS)	t_{trans_pdf}	TxD high to low transition[2]			4	µs
Propagation delay transmitter (TxD->BUS)	t_{trans_pdr}	TxD low to high transition[2]			4	µs
Propagation delay transmitter symmetry	t_{trans_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Propagation delay receiver (BUS->RxD)	t_{rec_pdf}	BUS recessive to dominant [2]			6	µs
Propagation delay receiver (BUS->RxD)	t_{rec_pdr}	BUS dominant to recessive[2]			6	µs
Propagation delay receiver symmetry	t_{rec_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Receiver debounce time	t_{rec_deb}	BUS rising & falling edge[3]	1.2		3.1	µs
Wake-up filter time	t_{wu}	BUS rising & falling edge[4]	25		90	µs
EN debauncing time	t_{en_deb}	Normal to sleep mode]	10	20	40	µs

[1] Minimum slew rate of the rising edge is determined by the network time constant

[2] See timing diagram figure 3

[3] See timing diagram figure 4

[4] See timing diagram figure 5

Timing Diagrams

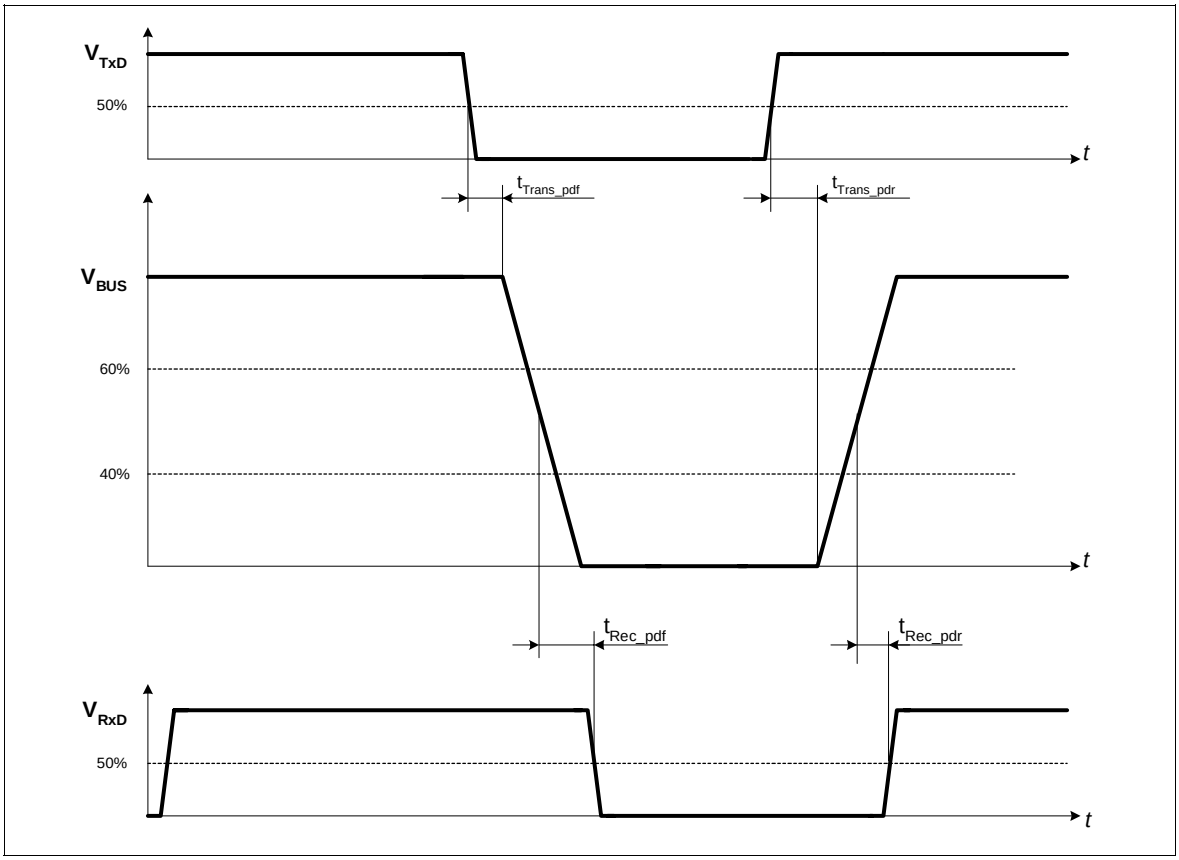


Figure 3 - Input/Output Timing

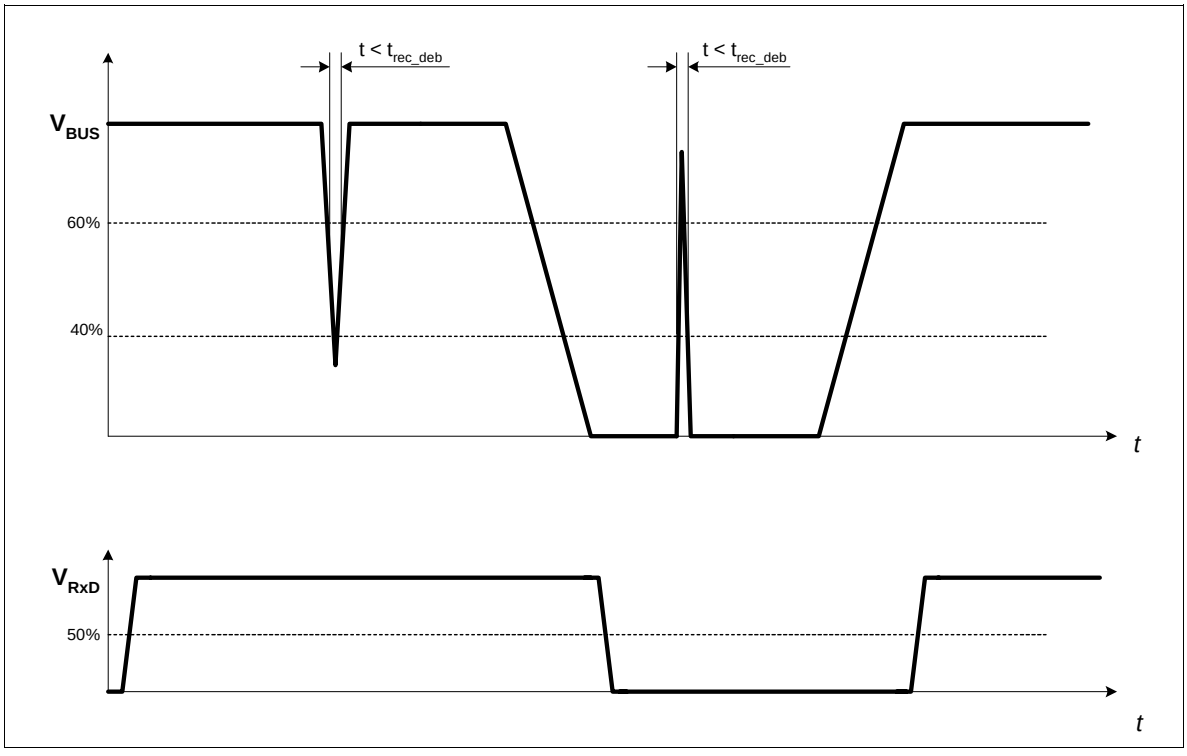


Figure 4 - Receiver Debouncing Filter

Timing Diagrams (continued)

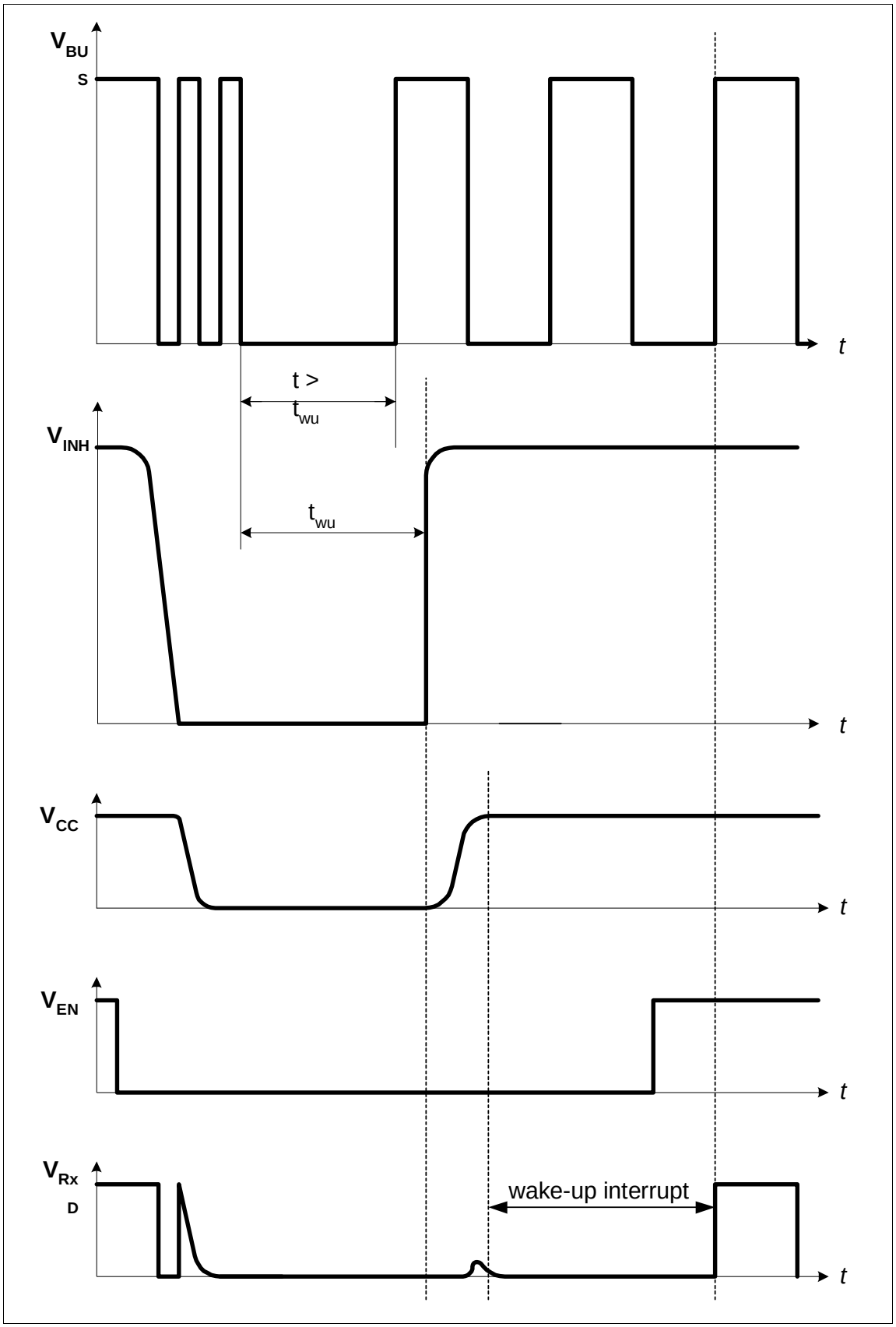


Figure 5 - Sleep mode and wake up procedure

Test Circuit for Dynamic Characteristics

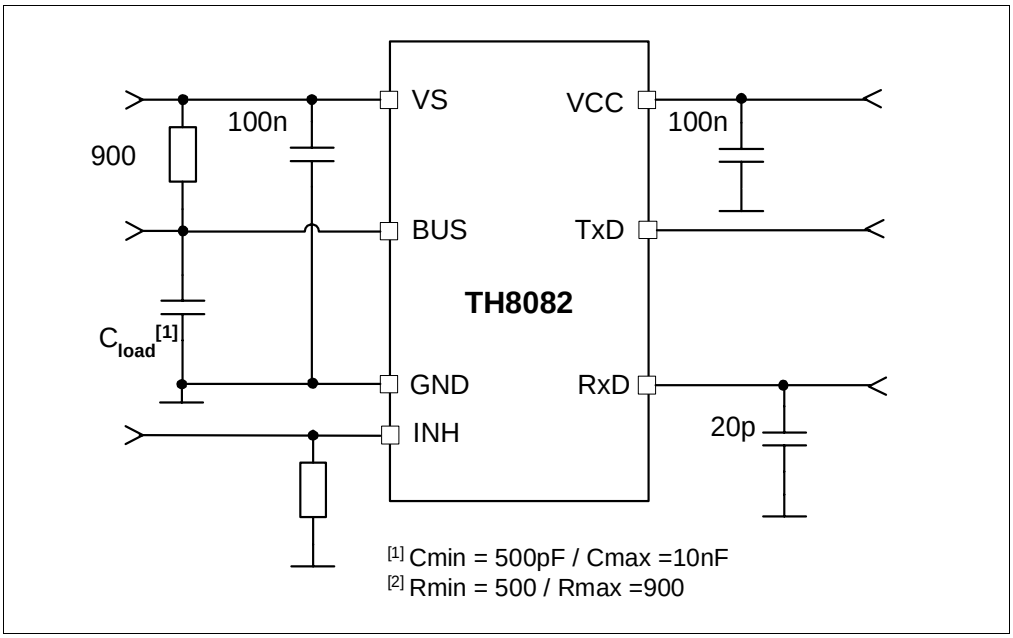


Figure 5 - Test Circuit for Dynamic Characteristics

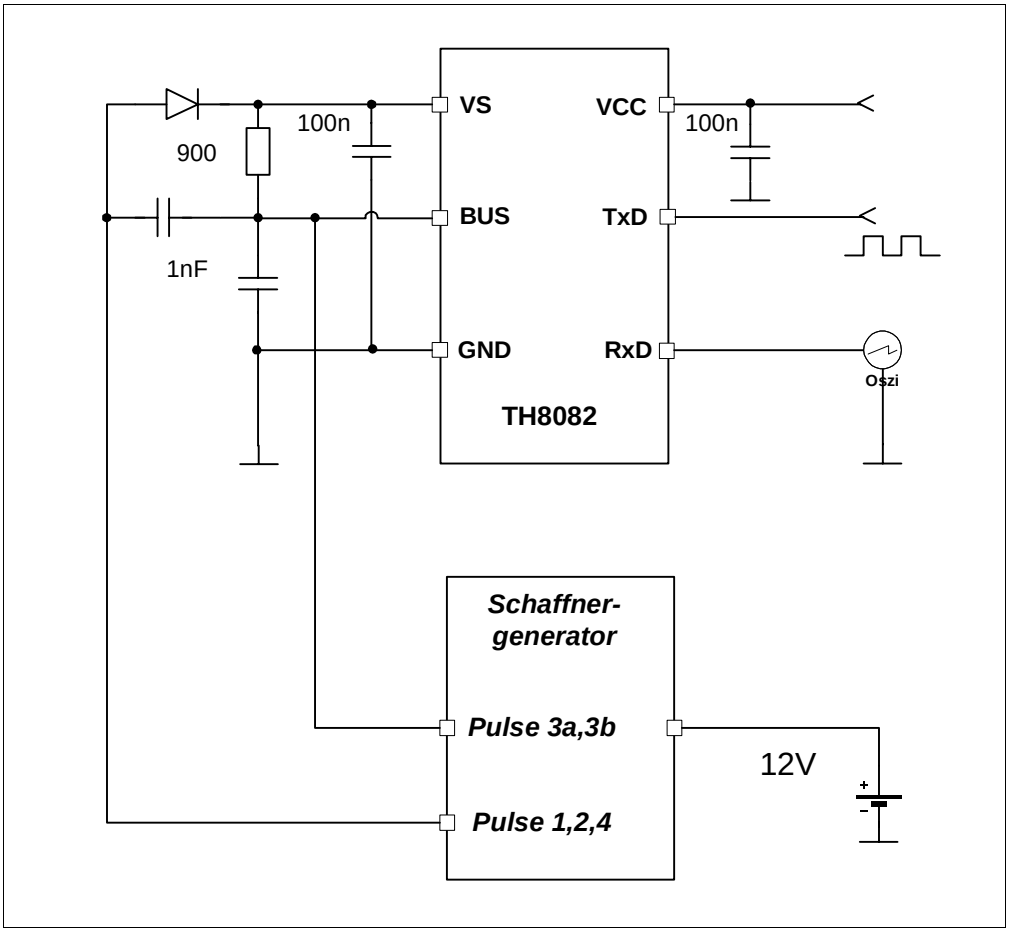
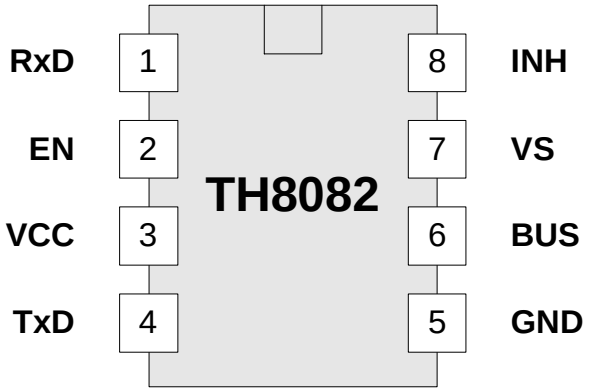


Figure 6 - Test Circuit for Automotive Transients

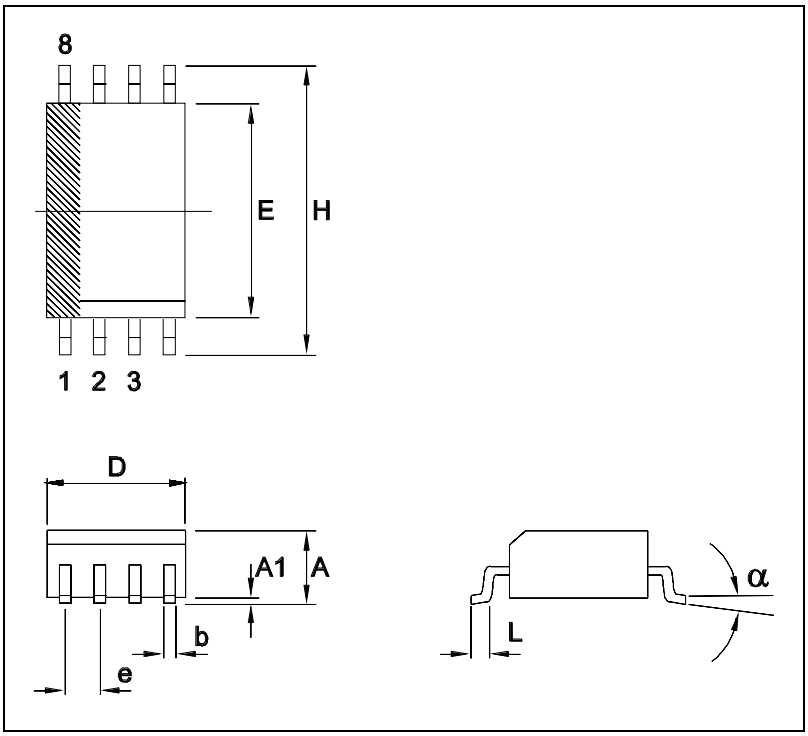
Pin Description



Pin	Name	I/O	Function
1	RXD	O	Receive data from BUS to core, LOW in dominant state
2	EN	I	Enables the normal operation mode when HIGH
3	VCC		5V supply input
4	TXD	I	Transmit data from core to BUS, LOW in dominant state
5	GND		Ground
6	BUS	I/O	Single wire bus pin, LOW in dominant state
7	VS		Battery input voltage
8	INH	O	Control output for voltage regulator

Mechanical Specifications

SOIC8 Package Dimensions



Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**α**
min	4.8	3.80	10.00	5.80	0.10	1.27	0.33	0.40	0°
max	5.0	4.00	10.65	6.20	0.25		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004”									
min	0.189	0.150	0.228	0.053	0.004	0.050	0.013	0.016	0°
max	0.197	0.157	0.244	0.069	0.010		0.020	0.050	8°

Notes

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