CMOS 4-BIT MICROCONTROLLER

TMP47C858F

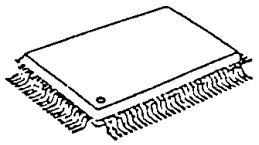
The 47C858 is a high performance 4-bit single chip microcomputer based on the TLCS-470 series. The 47C858 has plentiful operating modes (SLOW, SLEEP, HOLD) intended to save the power, with LCD driver and DTMF generator which are highly suitable for application in telephones.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C858F	8192 x 8-bit	512 x 4-bit	QFP100	TMP47C058G

FEATURES

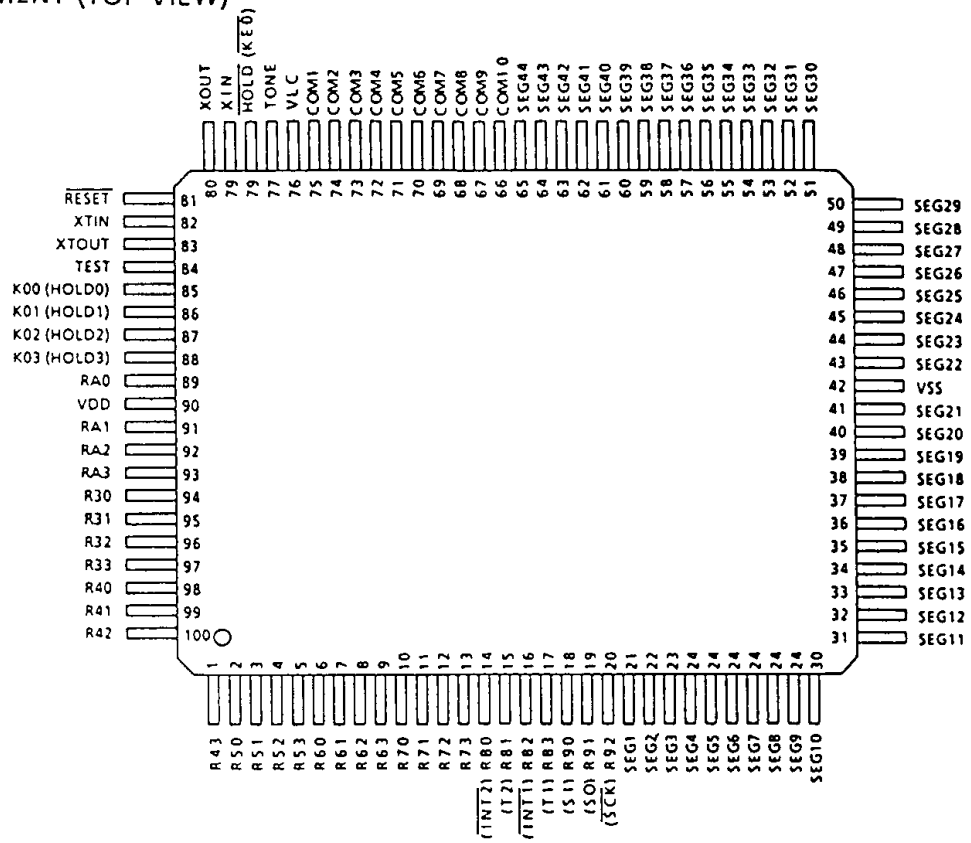
- ◆4-bit signal chip mocrocomputer
- ◆Instruction execution time:
  8.3μs (at 960KHz), 244μs (at 32.8KHz)
- ◆Low voltage operation: 2.7V min.
- ◆92 basic instrutions
- ◆Table look-up instructions
- ◆Subroutine nesting: 15 levels max.
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latchs each, and multiple interrupt control is available.
- ◆I/O port (36pins)
  - Input 2ports 5pins
  - I/O 8ports 31pins
- ◆Interval Timer (22 stages)
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 8-bit buffer
  External/internal clock, and leading/trailing edge shift, and 4/8-bit mode
- ◆LCD driver
  LCD direct drive is available (440 dots display, 1/10 duty)
- ◆DTMF (Dual Tone Multi Frequency) output
  - DTMF output with one instrution
  - Single tone output function
- ◆Dual-clock operation
  High-speed/Low-power-consumption operating mode
- ◆HOLD function
  - Battery/Capacitor back-up
- ◆SLEEP function
  - Battery/Capacitor back-up
  - LCD is displaying

QFP100

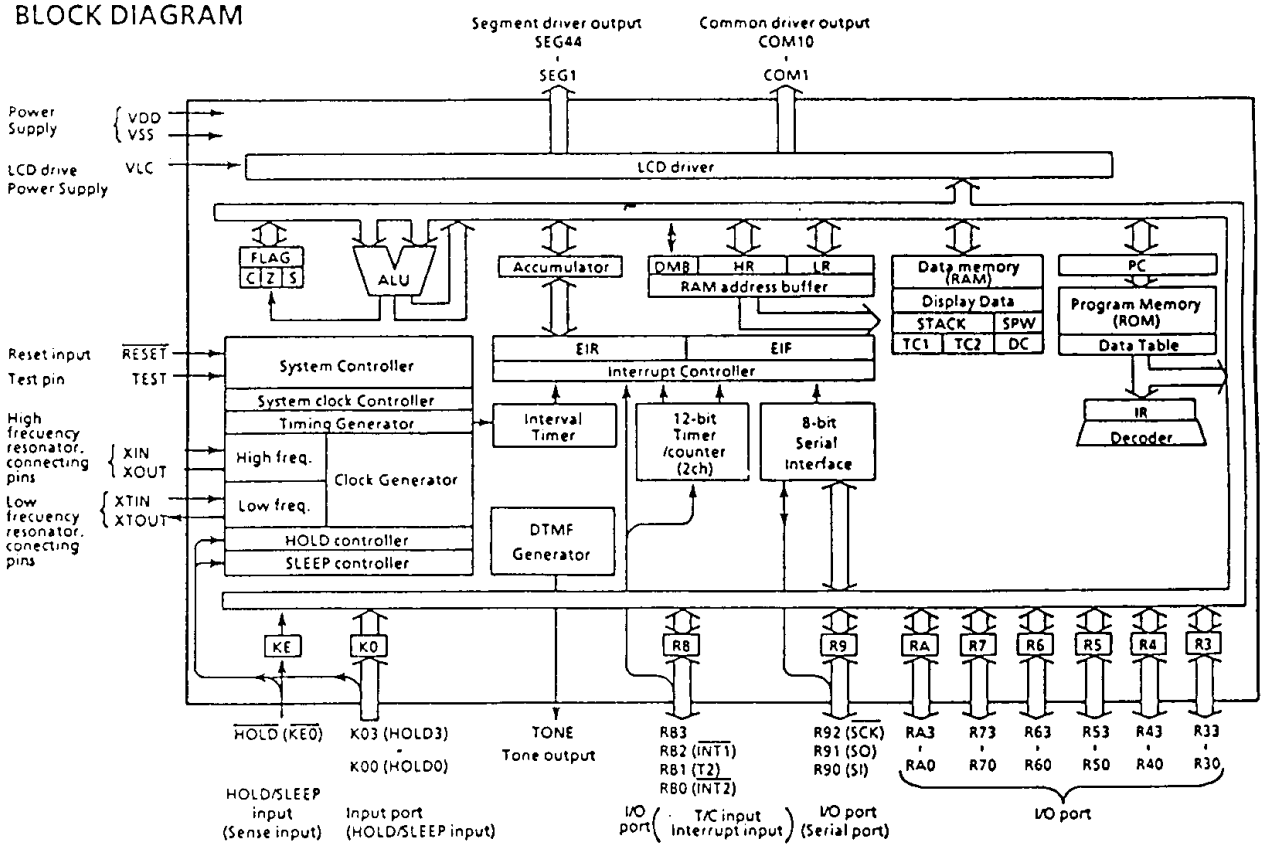


PIN ASSIGNMENT (TOP VIEW)

QFP100



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) ⋮ K00 (HOLD0)	Input (Input)	4-bit input port	HOLD and SLEEP request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
RA3 - RA0	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
SEG44 - SEG1	Output	LCD segment driver output	
COM10 - COM1		LCD common driver output	
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins (High frequency). For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
XTIN	Input	Oscillator connecting pins (Low frequency). For inputting external clock, XTIN is used and XTOUT is opened.	
XTOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD and SLEEP request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 2.7V to 6.0V	
VSS		0V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C858 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C800, the technical data sheets for the 47C800 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) CPU Core Functions

Except for the systemcontrol circuit, the CPU core functions are the same as those of the 47C800.

(2) Periferal Hardware Functions

① I/O Ports
② Interval Timer
③ Timer/Counter
④ One-second Signal Detection Circuit
⑤ LCD Driver
⑥ DTMF Generator
⑦ Serial Interface

The following are explanations of functions ① and④—⑥which have been added to the 47C858 or which are different from those of the 47C800, and the system clock control circuit.

2 CPU CORE FUNCTIONS

2. 1 SYSTEM CONTROL CIRCUIT

It is possible to shift from the SLOW operating mode to the SLEEP operating mode to further reduce power consumption and still maintain the internal status. In the SLEEP mode, all operations execpt for the timing generator(TG) binary counter and LCD driver are suspended.

2.1.1 System Clock Controller

The system clock controller starts or stops the high-frequency and low-frequency clock oscillator and switches between the basic clocks. The operating mode is generally divided into the single-clock mode and the dual-clock mode, which are controlled by command.

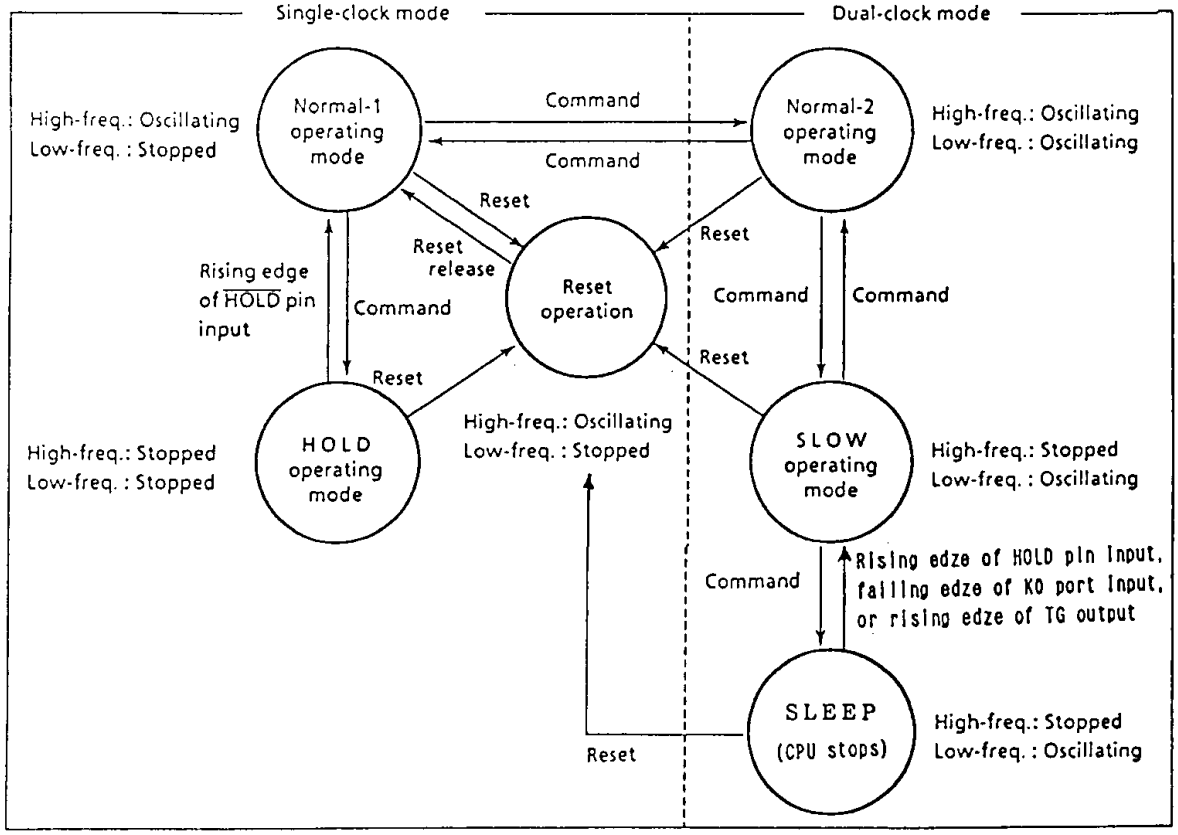


Figure 2-1 Operating Mode Transition Diagram

(1) Control of System Clock

The system clock is controlled by the command register(OP16). Dureing a reset, the command register is reset to "0" and the single clock mode is selected. Oscillation of the low-frepuency clock is started in the single clock mode by setting bit 3 of OP13.

System clock control

(Port address:OP16 Initial value:*000)

3	2	1	0
	DCLK		DWUT

DCLK	Operating mode selection
00:Single-clock mode(Normal-1)	
01:Dual-clock mode(Normal-2)	
10:Reserved	
11:Dual-clock mode(SLOW)	

DWUT	Warm-up time selection	Note2.
	Example:	fc=960KHz fs=32.8KHz時
0:	$2^8/fs+2^9/fc$ [sec] ·····	8.3[ms]
1:	$2^{11}/fs+2^9/fc$ ·····	63.0

Low-frepuency oscillation control

(Port address:OP13 Initial value:000*)

3	2	1	0
ESC	(SWU)		

ESC	Low-frepuency oscillation control	Note3.
0:Oscillation stops		
1:Oscillation starts		

Note1. *; don't care
fc=High-frepuency clock[Hz]
fs=Low-frequency clock[Hz]

Note2. It is valid only at switching from the SLOW to the Normal-2.

Note3. It is valid only in the Normal-1 operating mode

Figure 2-2. System Clock Control Command Register

2.1.2 Operating Mode

There are two operating modes:the Single-clock mode and the Dual-clock mode.

(1) Single-clock Mode

Canceling a reset starts the Normal-1 operating mode. Oscillation of the low-frequency clock can be started and stopped in this mode. To shift to the Dual-clock mode, start oscillation with the low-frequency oscillation control command register(OP13) and then switch to the Norma-2 operating mode with the system clock control command register (OP16).

There is also a HOLD operating mode used for low power consumption operation. To switch to HOLD operation, stop oscillation of the low-frequency clock(OP13) and then switch with the HOLD operation mode command register(OP10).

(2) Dual-clock Mode

In the Dual-clock mode, the instruction cycle is normally generated with the high-frequency clock(fc) and then the Normal-2 operating mode is used. When necessary, the SLOW operating mode can be used by generating the low-frequency clock(fs). In addition, the SLEEP operation mode, in which all operations except the low-frequency clock and LCD driver are suspended, can also be used. Switching between Normal-2 operation,SLOW operation and SLEEP operation in the Dual-clock mode is explained below. During a reset, the command register is initialized to the Single-clock mode. At this time, the low-frequency clock is not being oscillated; therefore, start oscillation of the low-frequency clock first and then switch to Normal-2 operation in the Dual-clock mode.

a)Switching from the Normal-2 operation to the SLOW operation

Setting DCLK(bit2 of OP16) to "1" switches to SLOW operation, but several seconds are required for low-frequency clock oscillation to stabilize. Consequently, when there is a possibility of switching to SLOW operation immediately after shifting to Normal-2 operation, it is necessary to wait until oscillation of the low-frequency clock stabilizes. Oscillation of the high-frequency clock will stop at this time.

b)Returning from the SLOW operation to the Normal-2 operation

When DCLK(bit 2 of OP16) is cleared to "0", the warm-up time for resetting to DWUT(bit 0 of of OP16) is set at the same time. Normal-2 operation starts after the set warm-up time has elapsed.

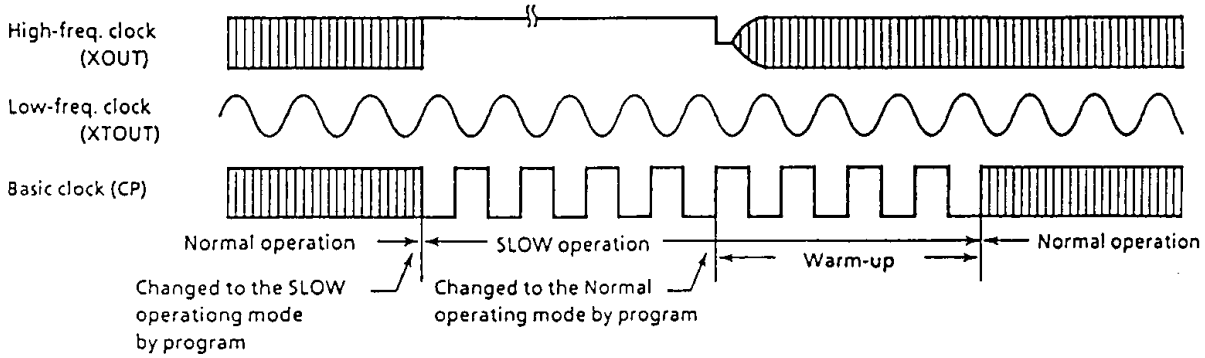


Figure 2-3. System Clock Swithing Timing

c)Shifting from the SLOW operation to the SLEEP operation

After selecting the return conditions using the return conditions selection register(OP13), shift to SLEEP operation (refer to the SLEEP operation mode explanation) by setting the command in the command register(OP10). Occurrence of the selected condition returns to SLOW operation.

Note1. The command register(OP10) is used for both HOLD operation control and SLEEP operation control. This register is used for HOLD operation control when accessed during Normal-1 operation and for SLEEP operation control when accessed during SLOW operation.

Note2. During SLOW operation and SLEEP operation, oscillation of the high-frequency clock is automatically halted to enable low power supply voltage operation and low power consumption operation. However, while less power is consumed by the oscillator and internal hardwaer, the amount of power consumed by the pin interface (dependent on external circuitry and programs) is not directly related to the low power consumption operation mode;therefore, caution is required during system design and interface circuit design. Also, the execution of instructions is not interrupted by switching to SLOW operation but, in some cases, there is influence on some of the peripheral hardwaer functions;therefore, refer to the explanations of the various operations.

HOLD operating mode control

(Port address:OP10 Initial value:*0**)

3	2	1	0
HLDMS		HWUT	

HLDMS	Mode select/HOLD operation start
01: Starts HOLD operation in edze sensitive release mode	
11: Starts HOLD operation in level sesitive release mode	
*0: Reserved	

HWUT	Warm-up time selection	
	Example: at fc=960KHz	
00: 2^{18}/fc[sec]	····· 273	[ms]
01: 2^{14}/fc	····· 17	
1*: Reserved		

Note1. *; don't care

Note2. Do not access command register OP10 unless the HOLD operation mode is being used

Figure 2-4. Command Register

2.1.3 HOLD Operation Mode

HOLD operation suspends system operation and holds the internal status immediately before the suspension with low power consumption. This mode is started by setting the command in the command register(OP10) in the Normal-1 operation mode, but it is necessary to stop the low-frequency clock(by clearing bit 3 of OP13) before accessing OP10. Hold control is possible not only from the HOLD pin but from the K0 port as well. Figure 2-5 shows the relationship between the KE port, KEO input data and the HOLD control signal. The KE port is assigned to the lowest bit of port address IPOE and is read as the result of the logical operation of the KEO pin and K0 pin input. When the KEO pin is"L"and all four K0 pins are "H", for example, the KEO input data is read as"1". "0"is read at all other times.

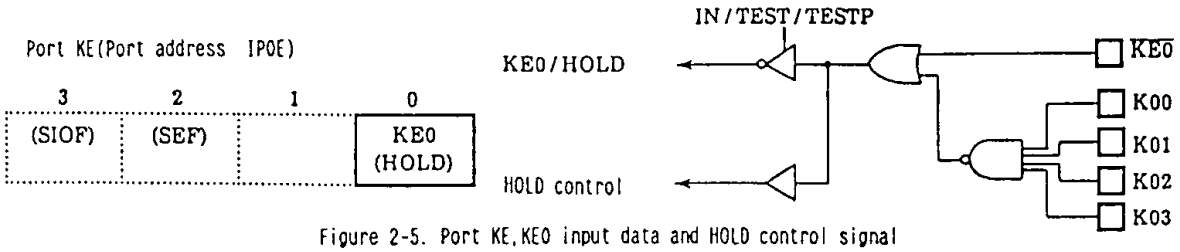


Figure 2-5. Port KE, KE0 input data and HOLD control signal

The HOLD operation mode is released when a hold control signal rise from "0" to "1" is sensed. Consepuently, if the hook switch is connected to the HOLD pin and the key switch is connected to the K0 pin, it is possible to release HOLD operation by either turning off the hook switch or by pressing a key. Thus, an on-hook dialing function can easily be implemented. Other than that, the HOLD operation mode is the same as for the 47C800. For details, refer to the 47C800 technical data.

2.1.4 SLEEP operation mode

The SLEEP operation mode suspends all SLOW operation operations except for the low-frequency clock, TG binary counter and LCD driver, and retains the internal status with low power consumption without stopping the clock function and LCD display.

SLEEP mode control

(Port address : 0P10 Initial value : ****)

3	2	1	0
SLPMS			

SLPMS	Mode selection and SLEEP operation starts
0111: Starts SLEEP operation in edge sensitive release mode	
1111: Starts SLEEP operation in level sensitive release mode	
The other codes are reserved	

Return conditions selection register

(Port address : 0P13 Initial value : 000*)

3	2	1	0
(ESC)	SWU		

SWU	Return conditions selection
00: HOLD and K0 pin input	
10: HOLD, K0 pin and 1 sec signal	
*1: HOLD, K0 pin and 15.625msec signal	

Figure 2-6. Command Register, Return Conditions Selection register.

Operation in the edge relese mode and level release mode is the same as in the HOLD operation mode. To start SLEEP operation, select the return conditions during SLOW operation with the return conditions selection register(0P13) and then set the start command in the command register(0P10). SLEEP operation is then return to SLOW operation when the conditions selected with the return conditions selection register occur.

Example: Starting SLEEP operation using the HOLD and K0 pin input, and the 1 sec signal as return condition.

```
LD      A, #0CH        ; Selects HOLD, K0 pin input and 1 sec signal
OUT     A, %0P13
LD      A, #7H         ; Starts SLEEP operation
OUT     A, %0P10
```

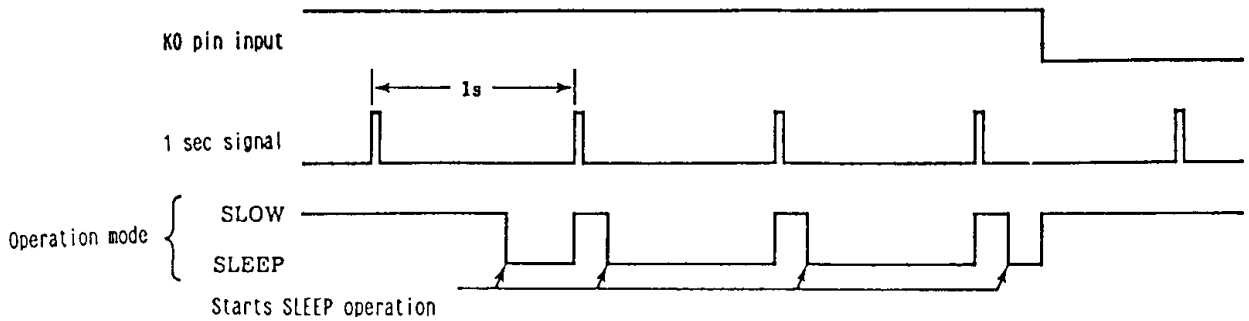


Figure 2-7 Return Conditions and operation Mode

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C452A has 10 ports (36 pins) each as follows :

① K0
② R4, R5, R6
③ R3, R7, RA
④ R8
⑤ R9
⑥ KE

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03-K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

Port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

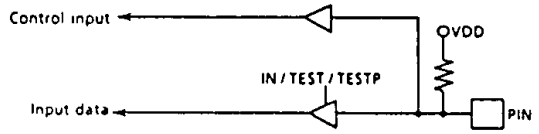


Figure 3-1. Port K0

(2) R3 (R33~R30), R7 (R73~R70), RA (RA3~RA0)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R• (Port address OP0• / IP0•)

3	2	1	0
R•3	R•2	R•1	R•0

•; 3, 7, A

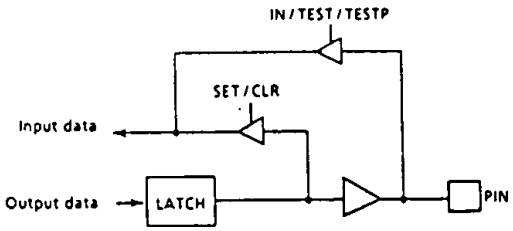


Figure 3-2. R3, R7, RA

3.2 One-second Signal Detection Circuit

A one-second signal detection circuit is built-in to enable clock functions. A flip-flop construction is used which is set by the rise (one second) of the TG final stage output and which is reset by accessing port address OP0D. The one-seconnd detection circuit can be used in Normal-2 operation, SLOW operation and SLEEP operation mode.

Example 1. Reads F/F

```
IN      %IP0D, A
```

Example 2. Resets F/F

```
OUT     A, %OP0D
```

One-second Monitor

(Port address : IP0D)

3	2	1	0
•	•	•	SSD

SSD	Detection of one-second
0: Reset	
1: Set	

Figure 3-3. One-second Monitor

Port Address (**)	Port		Input/Output instructions						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p,b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note 2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○	○	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	1 sec signal status	Resets F/F	○	○	○	–	–	–	–
0E	status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	Single tone control	–	○	–	–	–	–	–
13	Undefined	Slow clock/SLEEP operation control	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	LCD driver control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	Serial interface control 1	–	○	–	–	–	–	–
1F	Undefined	Serial interface control 2	–	○	–	–	–	–	–

Note 1. *"——" means the reserved state. Unavailable for the user program.*

Note 2. *The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ROW register and Column register.*

Table 3-1. Port Address Assignments and Available I/O Instructions

3.3 DTMF Generator

The 47C858 has a built-in DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF ; Dual Tone Multi Frequency)

3.3.1 Configuration of DTMF Generator

Figure 3-4 shows configuration of the DTMF generator. The 47C858 generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

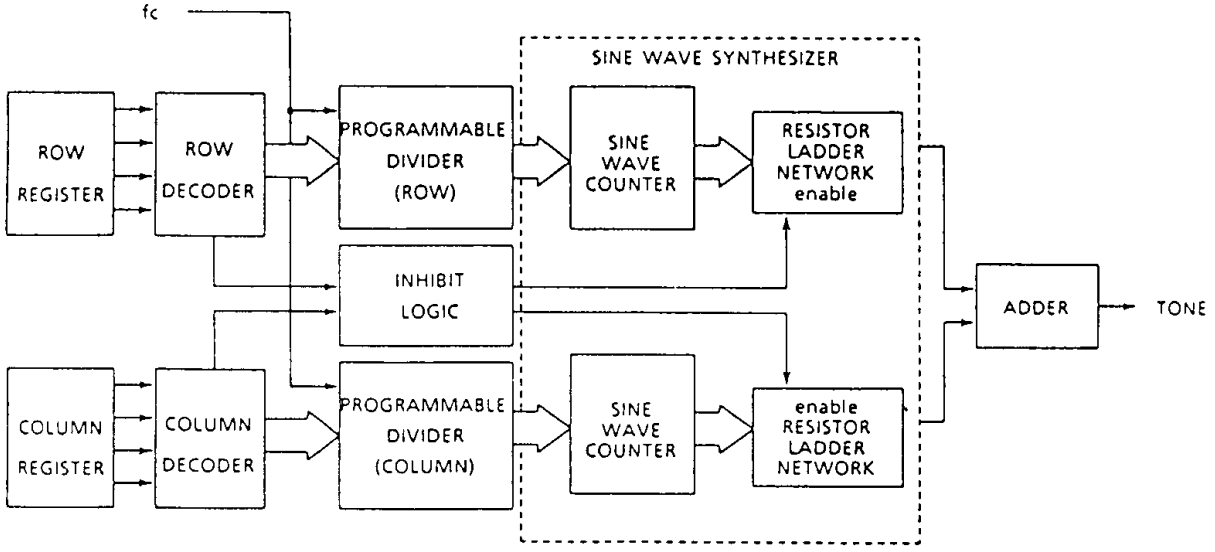
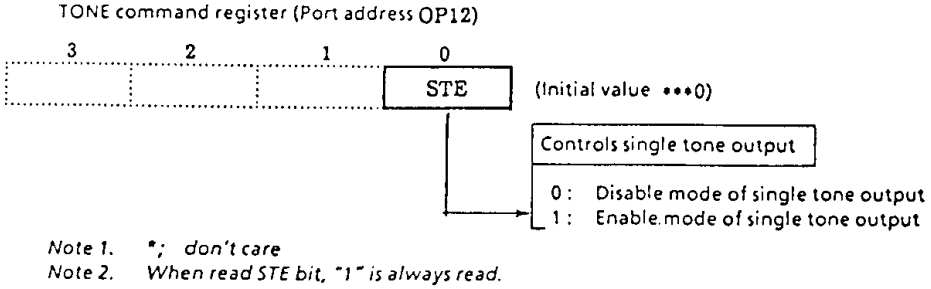


Figure 3-4. Configuration of DTMF Generator

3.3.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02) . And single tone is controlled by TONE command register (OP12). ROW register, COLUMN register and TONE command register are initialized to "0" during the reset.



Note 1. *; don't care*
Note 2. *When read STE bit, "1" is always read.*

Figure 3-5. TONE command register

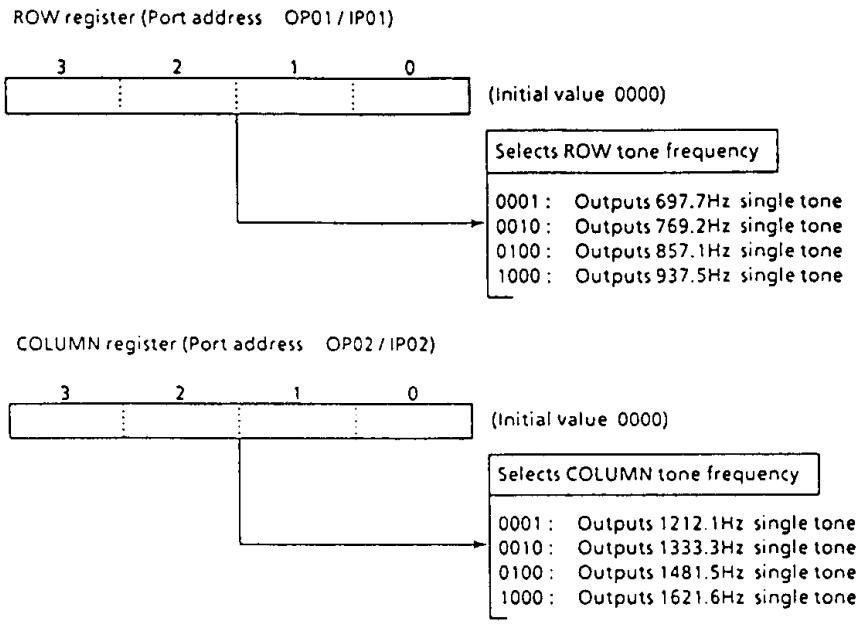


Figure 3-6. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-6 into the ROW and COLUMN registers. In the enable mode of single tone output and either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C858 has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1 : To output 1481.5Hz single tone

```
OUT     #8,%OP0D ; Sets the enable mode of single tone output.
OUT     #0,%OP01 ; Sets an ineffective code into ROW register.
OUT     #4,%OP02 ; Sets data "4" into COLUMN register
```

Example 2 : 8 bits data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM1 address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN registers, and dual tone is outputted.

```
LD      HL,#90H  ; HL←90H (Sets the address of the data memory)
OUTB    @HL      ; Sets the ROM data into the ROW and COLUMN register.
```

Table 3-2 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-3 shows the deviation between the 47C858 tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01/IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-2. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	- 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	- 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	- 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	- 0.70

Table 3-3. Tone output frequencies and Deviation from standard

3.3.3 Test mode for tone output

The 47C858 includes a test mode for checking tone output waveforms. Tones can be outputted by the curcuit shown in Figure 3-7. ROW data are inputted from the R4 port and COLUMN data are inputted from the R5 port, and any desired single or dual tones can be outputted by setting the frequency selection codes shown in Figure 3-6. Figure 3-8 shows a single tone waveform and Figure 3-9 shows a dual tone waveform.

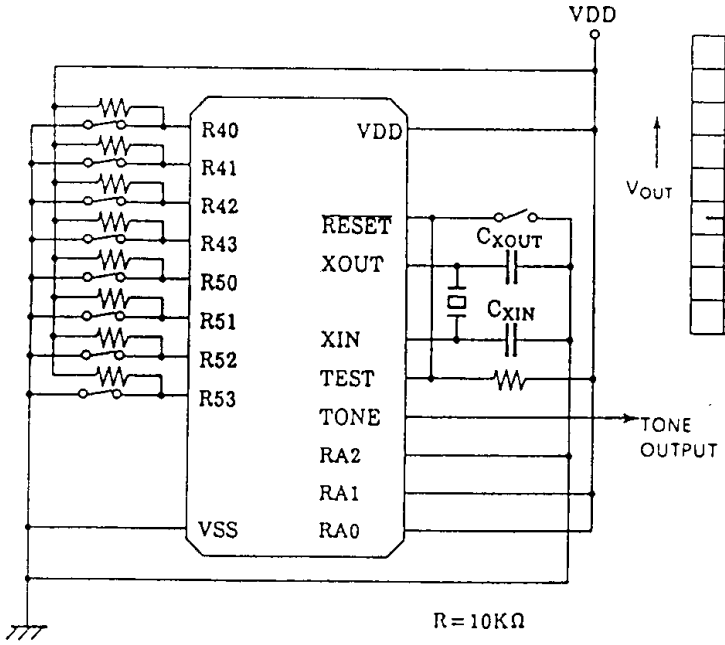


Figure 3-7. Tone test circuit

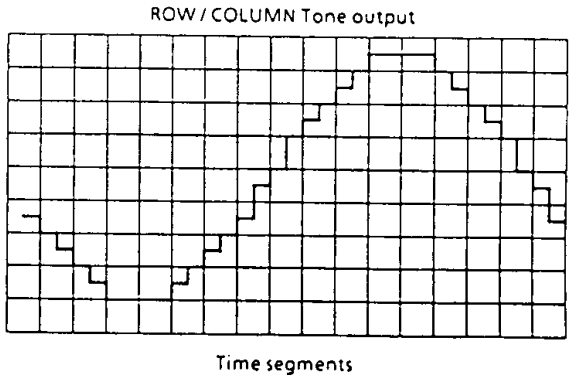


Figure 3-8. Single tone waveform

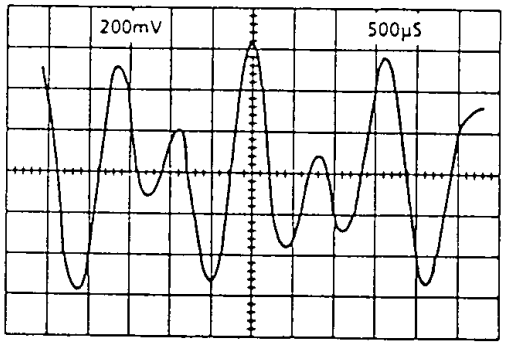


Figure 3-9. Dual tone waveform

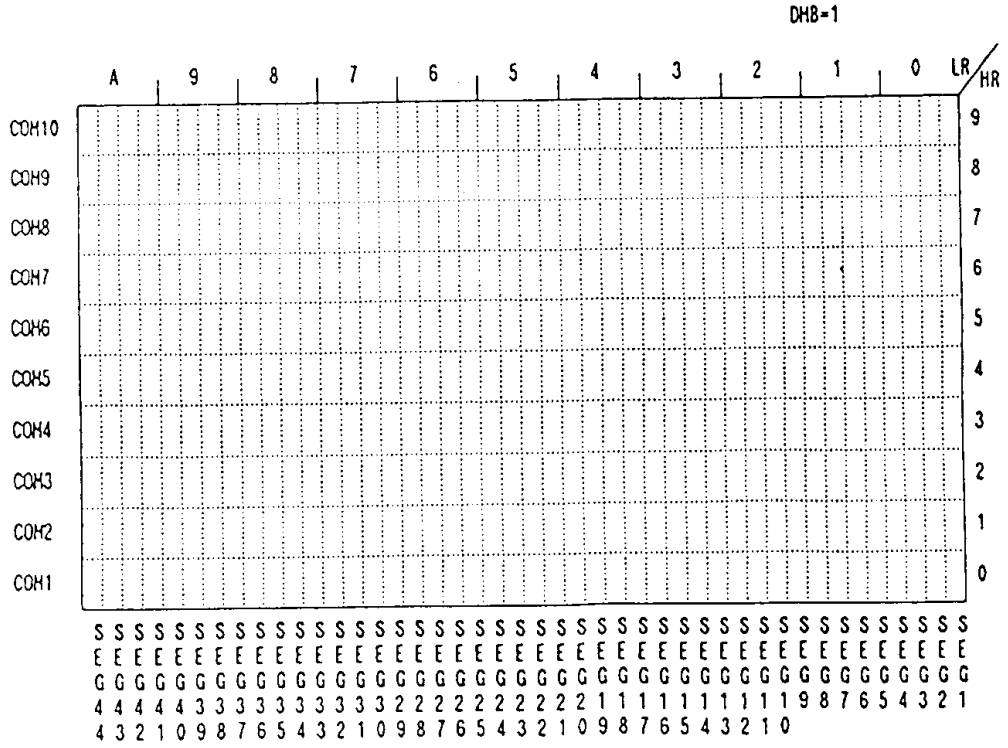
3.4 Display

3.4.1 Setting Display RAM

The data is stored in the display data area of RAM. Commands perform the processing which converts standard data into LCD display data (using mainly ROM data reference commands).

Display data is converted and stored in the area, and its data are automaticaly transfered to LCD drive circuit without any relation to program.

Each bit in the display data area of RAM and the LCD segment(dot) is in a one-to-one relationship.



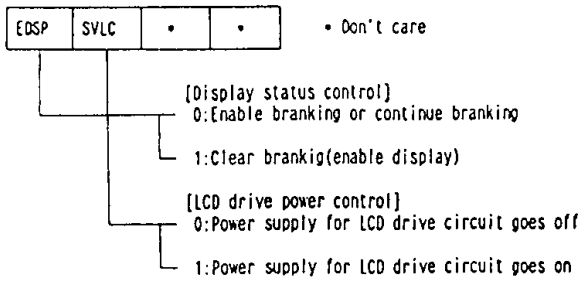
3.4.2 LCD Drive Control

There are 2-selecter circuit as LCD drive control.One is "Display status control", and the other is "LCD drive power control".

These code are selected by accessing the port resister address "OP1B".

(It is reset to "0" at initialization operation)

port resister address "OP1B"



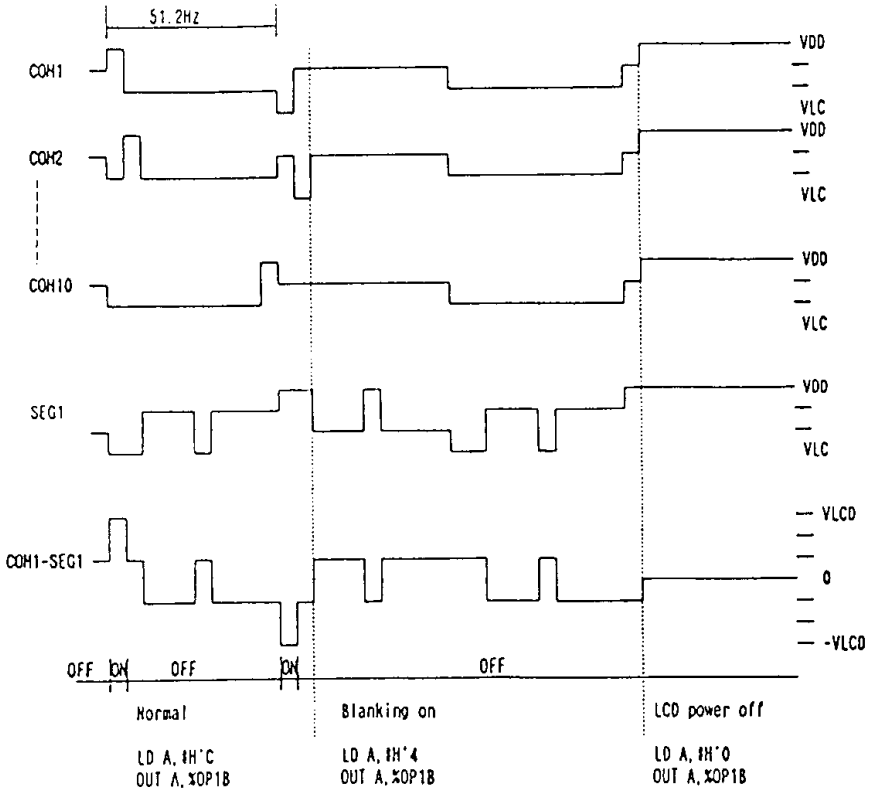
NOTE1:blanking-- COH1-COH10 goes into "non-light opration level". SEG1-SEG44 continues in normal operating status.

NOTE2:When the SVLC is "0", COH1-COH10 and SEG1-SEG44 go into VDD level.

Display output

Example of display output from the LCD drive circuit are given below.

(1/10 duty 1/3 bias)



Note: VLCD•VDD-VLC

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		− 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.7	6.0	V
			In the SLOW mode			
			in the SLEEPmode			
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		960		KHz
	fs	XTIN, XTOUT		30.0	34.0	KHz

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Segment Output Registance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} − V_{LC} = 3V	−	20	−	KΩ
Common Output Registance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS} fc = 960KHz	−	1.2	2.2	mA
	I_{DDT}		V_{DD} = 5.5V, V_{LC} = V_{SS} fc = 960KHz When tone is oscillating	−	3.0	5.0	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3V, V_{LC} = V_{SS} fs = 32.768KHz	−	30	60	μA
Supply Current (in the SLEEP mode)	I_{DDSP}			−	15	25	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.*

Note 3. *Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.*

Note 4. *$V_{O2/3}$; Shows 2/3 level output voltage.*
$V_{O1/3}$; Shows 1/3 level output voltage.

Note 5. *Supply Current I_{DD} ; V_{IN} = 5.3V/0.2V*
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.

Note 6. *Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).*

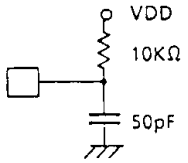
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = −30 to 60°C)

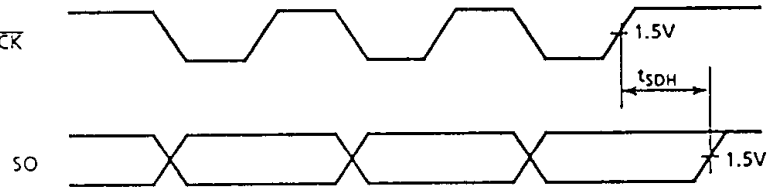
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	8.3			μs
		In the SLOW mode	235	—	267	μs
High level Clock pulse Width	t_{WCH}	External clock	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ − 300	—	—	ns

Note. Shift Data Hold Time :

External Circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



TONE OUTPUT CHARACTERISTICS

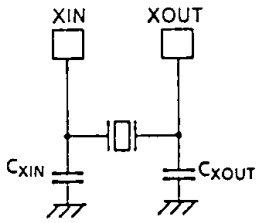
(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = −30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10KΩ, V_{DD} = 2.7V	125	185	250	mVrms
Pre-emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	Δf	Except error of osc. frequency	—	—	0.7	%

RECOMMENDED OSCILLATING CONDITIONS

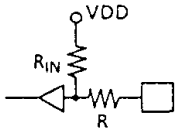
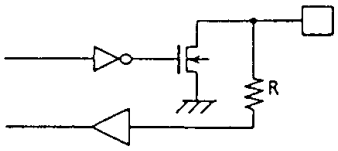
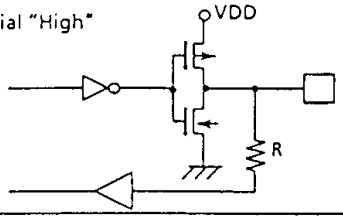
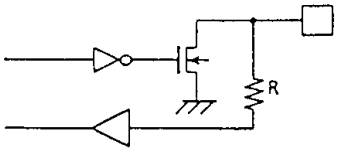
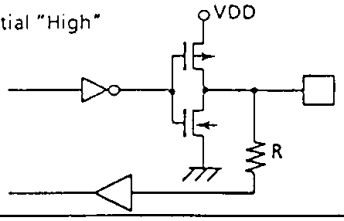
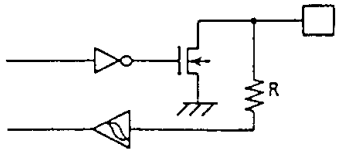
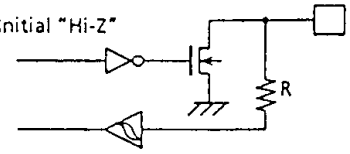
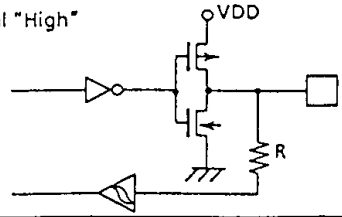
(V_{SS} = 0V, VDD = 2.7 to 6.0V, Topr = −30 to 60°C)

960KHz
Ceramic Resonator



(2) I/O Ports

The input/output circuitries of the 47C858 I/O ports are shown below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input		Pull-up resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R3 R4 R5 R6	I/O	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R7 RA	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R8	I/O		Sink open drain Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
R9	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1KΩ (typ.)