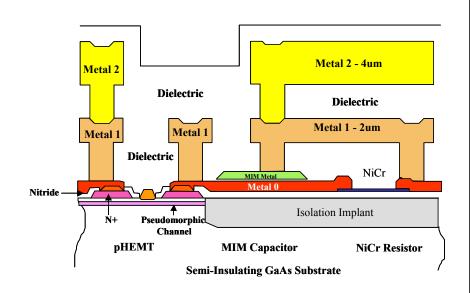


0.5 um pHEMT Foundry Service



0.5 um pHEMT Device Cross-Section

General Description

TriQuint's 0.5 µm pHEMT process is based on our production released 0.25 µm gate process. TQPHT substitutes lower cost optical lithography in place of e-beam and adds TriQuint's unique thick metal scheme. This process is targeted for high efficiency and linearity in power amplifiers, low noise amplifiers, and linear, low loss and high isolation RF switch applications. The TQPHT process offers a D-Mode pHEMT with a –0.8 V pinch off. The three metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost —effective die sizes.

Features

- D-Mode, -0.8 V Vp
- InGaAs Active Layer pHEMT Process
- 0.5 um Optical Lithography Gates
- 17 V D-G Breakdown Voltage
- High Density Interconnects:
 - 2 Global
 - I Local
- High-Q Passives
- Thin Film Resistors
- High Value Capacitors
- Backside Vias Optional
- Based on Production 0.25 μm pHEMT and Passives Processes
- TOM3 FET Models Available

Applications

- Highly Efficient and Linear Power Amplifiers
- Low Loss, High Isolation Switches for Wireless Transceivers and Basestations
- Higher Supply Voltage Applications
- Integrated RF Front Ends— LNA, SW, PA

Fully Released Production Process



0.5 um pHEMT Foundry Service

TQPHT Process Details

Process Details @ Vds = 3.0V				
Element	Parameter	Value	Units	
D-Mode pHEMT	Vp (1uA/um)	-0.8	V	
	ldss	200	mA/mm	
	ldh (lg=1ua/um)	500	mA/mm	
	Gm (50% ldss)	350	mS/mm	
	Breakdown, Vds	15 min	V	
	Ft @ 50% Idss	25	GHz	
	Fmax @ 50% Idss	90	GHz	
	Coff @Vds=0, Vgs= -2.5V	0.3	pF/mm	
	Ron @ Idss	1.8	Ohm-mm	
Common Process Element Details				
Gate Length		0.5	μm	
Interconnect		3	Metal Layers	
MIM Caps	Value	630	pF/mm2	
Resistors	NiCr	50	Ohms/sq	
	Bulk	285	Ohms/sq	
Vias		Yes		
Mask Layers	No Vias	12		
	With Vias	14		

Maximum Ratings

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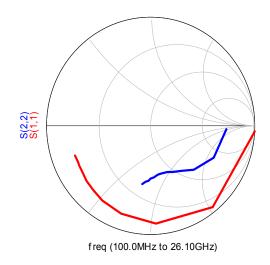
Storage Temperature Range	-65 to +150	Deg C
Operating Temperature Range	-55 to +150	Deg C
Transistor (Vs open; ldg = 1uA/um)	17	V
Capacitor	20	V

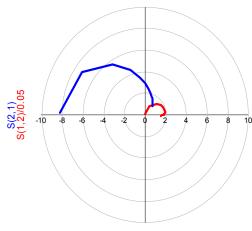


0.5 um pHEMT Foundry Service

S-Parameter Data:

300 um Device; Vds = 3.0V; 50% ldss

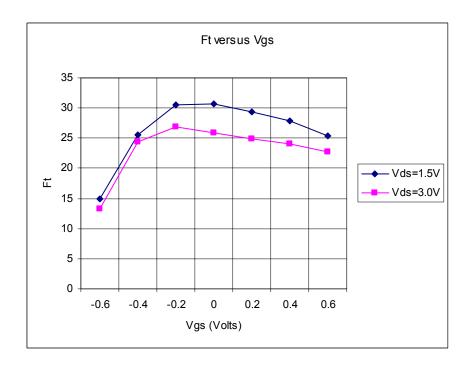




freq (100.0MHz to 26.10GHz)

Ft versus Vgs as a function of Vds: 300 um Device

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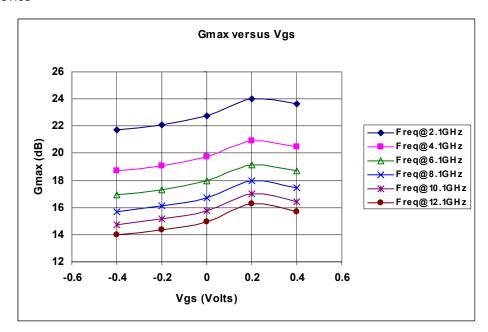




0.5 um pHEMT Foundry Service

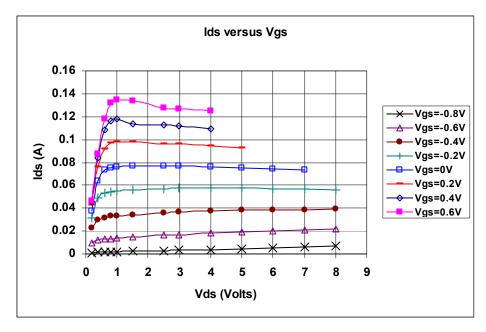
Gmax versus Vgs and Frequency:

300 um Device



I-V Characteristics:

300 um Device



TriQuint Semiconductor



0.5 um pHEMT Foundry Service

Prototyping and Development

- Prototype Development Quick Turn (PDQ):
 - Shared mask set
 - Run monthly
 - Hot Lot cycle time
- Prototype Wafer Option (PWO):
 - Customer-specific masks; Customer schedule
 - 2 wafers delivered
 - Hot Lot cycle time
 - With thinning and sawing; optional backside vias

Design Tool Status

- Complete Design Manual Now
- Device Library of circuit elements: FETs, diodes, thin film resistors, capacitors, inductors
- Design Kit for Agilent's ADS design environment
- Design Kit planned for AWR Microwave Office
- Layout Library in GSD II format
- Cadence Development Kit with PCells
- Layout Rule Sets for Design Rule Check
- Qualified package models for supported package styles

Training

- GaAs Design Classes:
 - Half-Day Introduction; Upon request
 - Four-Day Technical Training; Fall and Spring at TriQuint Oregon facility
- For Training & PDQ Schedules, please visit: www.triquint.com/foundry/

Process Qualification Status

- Mature process based on TQTx, 150-mm process
- Process released to production
- Full 150mm wafer Process Qualification complete
- For more information on Quality and Reliability, contact TriQuint or visit: www.triquint.com/manufacturing/QR/

Applications Support Services

- Tiling of GDSII stream files including PCM
- Design Rule Check services
- Layout Versus Schematic check services
- Packaging Development Engineering
- Test Development Engineering:
 - On-wafer
 - Packaged parts
- Thermal Analysis Engineering
- Yield Enhancement Engineering
- Part Qualification Services
- Failure Analysis

Manufacturing Services

Phone: 503-615-9000

Email: info@triquint.com

Fax: 503-615-8905

- Mask making
- Production 150-mm wafer fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Diesort Testing
- RF On-wafer testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative/ Distributor or Foundry Services Division for Additional information:

E-mail: sales@triquint.com Phone: (503) 615-9000 Fax: (503) 615-8905