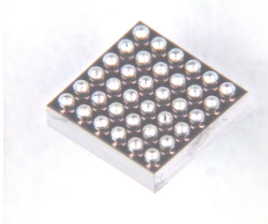
For information only

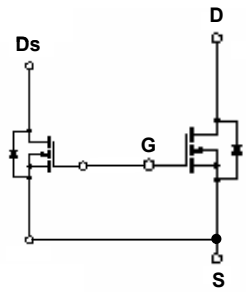
# DC-DC Converter Control and Synchronous AceFET™

# TS12N30CS – 30V Single N-Channel 4.5V Specified AceFET™

## General Description

Taiwan Semiconductor's new low cost, state of the art AceFET™ lateral MOSFET process technology in chipscale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low Qg X $R_{DS(ON)}$ figure of merit.



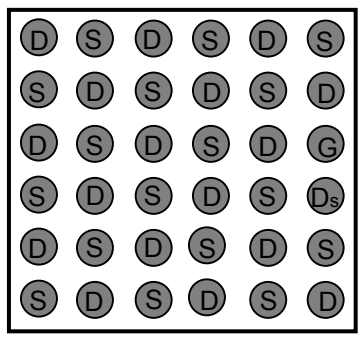



## Features

- 12A, 30V $R_{DS(ON)}$ = 6mΩ at 4.5 Volts
- 12A, 30V Qg = 15nC at 4.5 Volts
- Low profile package: less than 1mm height when mounted on PCB
- Occupies only 1/3 the area of SO-8.
- Excellent thermal characteristics.
- High power and current handling capability.
- Lead free solder balls available.

## AceFET™ for High Frequency DC-DC Converters

**Patent Pending**




**Bottom: Bump Side**

## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | ±12 | V |
| $I_D$ | Drain Current – Continuous | 6 | A |
| | – Pulsed | 25 | |
| $P_D$ | Power Dissipation (Steady State) | 2.2 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150 | ºC |

## Thermal Characteristics

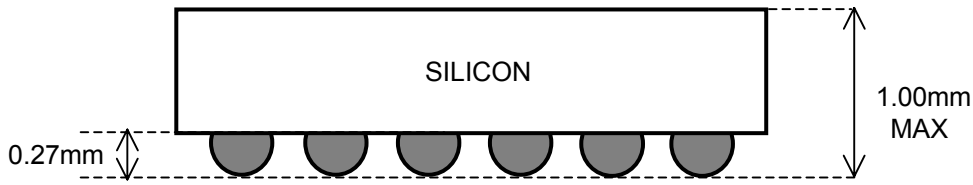
| | | | |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 56 | °C/W |
| $R_{\theta JR}$ | Thermal Resistance, Junction-to-Ball | 4.5 | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.6 | |

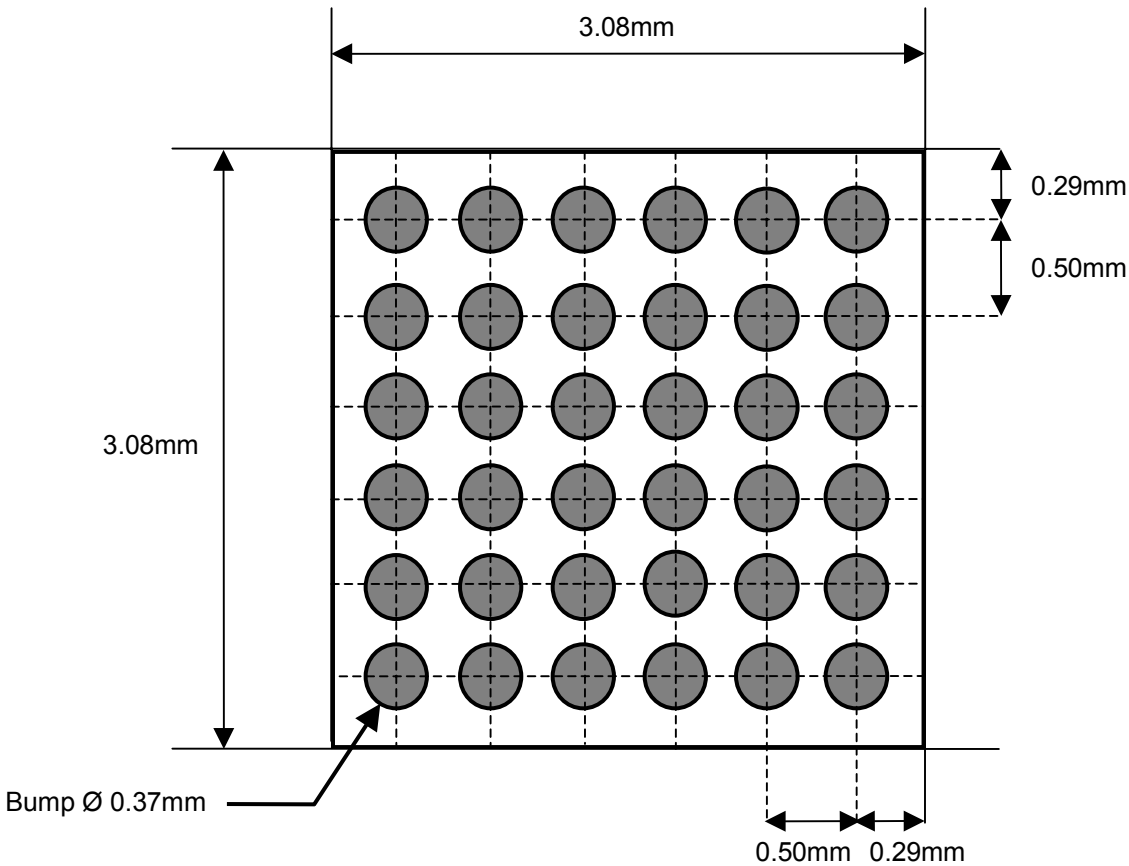
## Electrical Characteristics

$T_A$=25°C unless otherwise specified

| Symbol | Parameter | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$= 250 uA | 30 | | | V |
| $I_{GSS}$ | Gate-Body Leakage | $V_{GS}$ = ±12, $V_{DS}$=0V | | | ±150 | nA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | Tj = 150°C, $V_{DS}$ =30V , $V_{GS}$=0 V | | | 250 | uA |
| $I_{DDS}$ | Drain to Drain Sense Leakage | Tj = 150°C, $V_{DS}$ =30V , $V_{GS}$=0 V | | | 250 | uA |
| $R_{DS\,(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 12A | | 6 | | m□ |
| $R_{DSDS\,(on)}$ | Drain Sense On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 0.35A | | 210 | | m□ |
| $V_{GS\,(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$ , $I_D$ = 250uA | | 1.3 | | V |
| Qg | Total Gate Charge | $V_{DS}$ = 30V , $V_{GS}$ = 4.5V, $I_D$=12A | | 15 | | nC |
| Rg | Gate Resistance | $V_{DS}$ = 0V , f = 1MHz | | 0.4 | | Ohms |
| Coss | Output Capacitance | $V_{DS}$ = 30V , $V_{GS}$ = 0V, f = 1MHz | | 650 | | pF |
| Ciss | Input Capacitance | $V_{DS}$ = 30V , $V_{GS}$ = 0V, f = 1MHz | | 1500 | | pF |
| Crss | Reverse transfer capacitance | $V_{DS}$ = 30V , $V_{GS}$ = 0V, f = 1MHz | | 220 | | pF |
| trr | Reverse Recovery time<br>Source-Drain Diode | If = 12A , di/dt = 100A / us<br>Tj = 150°C | | | 40 | ns |
| $V_{SD}$ | Forward On-Voltage<br>Source-Drain Diode | $I_S$ = 12A, $V_{GS}$ = 0V | | 0.75 | | V |
| ID(on) | On-State Drain Current | $V_{GS}$ = 4.5V , $V_{DS}$ = 1V 25 | | | | A |
| Eas | Avalanche Energy UIS | Single Pulse 10us , $V_{DS}$> $BV_{DSS}$ | 2.5 | | | mJ |

## Dimensional Outline and Pad Layout




Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu

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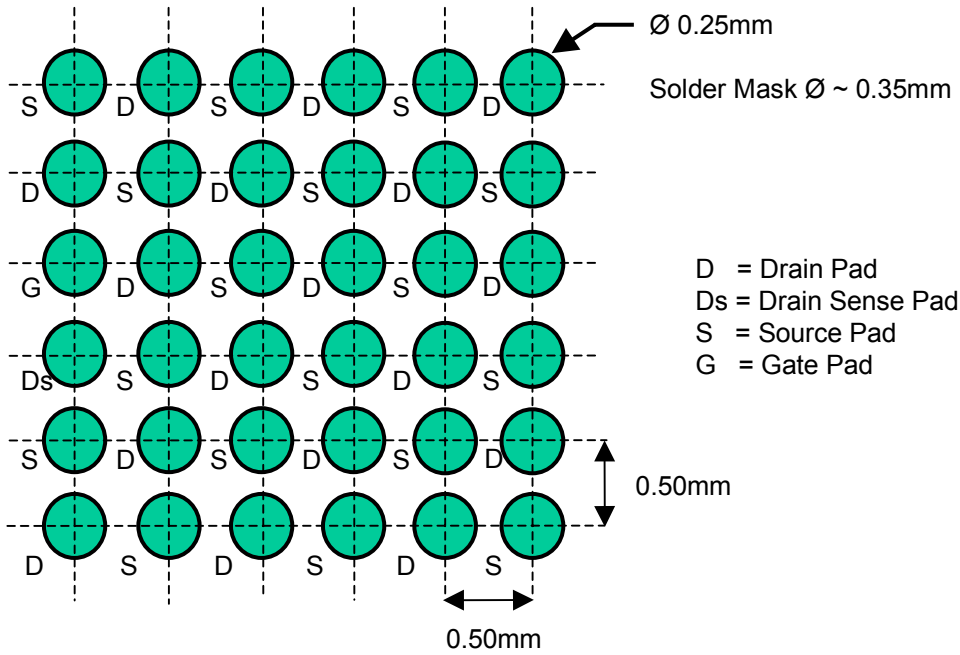
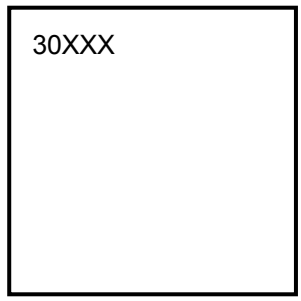



LAND PATTERN
RECOMMENDATION




MARK ON BACKSIDE OF DIE

XXX = Date/Lot Traceability Code