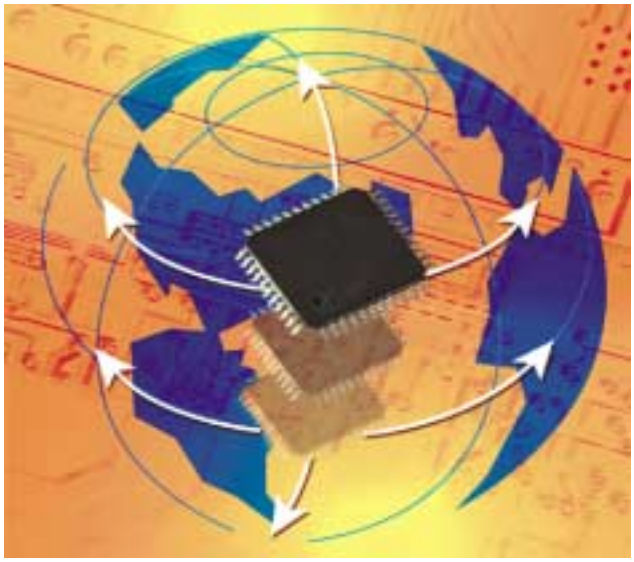
Qualification Package
TS87C51RD2 / TS83C51RD2
CMOS 0.5µm



TS87C51RD2 / TS83C51RD2
CMOS 0.5 µm
JUNE 2001

Qualpack TS87C51RD2/TS83C51RD2

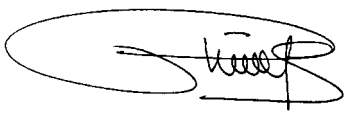
1 Contents

Qualpack TS87C51RD2/TS83C51RD2

2 General Information

Product Name:	TS87C51RD2
Function:	8 Bits Microcontroller, 64K bytes memory
	TS87C51RD2: 64k EPROM TS83C51RD2: 64k ROM
Wafer Process:	CMOS 0.5um
Available Package Types	PLCC 44, VQFP 44 1.4, PDIL 40, PLCC 68, VQFP 64 1.4
Other Forms:	Die, Wafer
Locations:	
Process Development,	ATMEL Nantes , France
Product Development	ATMEL Nantes , France
Wafer Plant	ATMEL Nantes , France
QC Responsibility	ATMEL Nantes, France
Probe Test	ATMEL Nantes , France
Assembly	Dependant upon Package
Final Test	Dependant upon Package
Lot Release	ATMEL Nantes, France
Shipment Control	GLOBAL LOGISTICS CENTER, Philippines
Quality Assurance	ATMEL Nantes, France
Reliability Testing	ATMEL Nantes, France
	ATMEL Nantes, France
Failure Analysis	ATMEL Nantes, France

Quality Assurance Management
ATMEL Nantes, France



Signed: Pascal LECUYER

Qualpack TS87C51RD2/TS83C51RD2

3 Technology Information

3.1 Wafer Process Technology

Process Type (Name):	Z94 (SCMOS3 Non Volatile - EPROM) Z92 (SCMOS3 - ROM)
Base Material:	Bulk
Wafer Thickness (final)	475µm
Wafer Diameter	150 mm
Number Of Masks	Z94: 22 Z92: 14
Gate Oxide (Logic transistors)	
Material	Silicon Dioxide
Thickness	110 A
Gate Oxide (EPROM cell)	
Material	Silicon Dioxide
Thickness	220 A
Polysilicon	
Number of Layers	2 (Z94), 1 (Z92)
Thickness Poly 1	2000A
Thickness Poly 2	3000A
Metal	
Number of Layers	2
Material:	AlCu
Layer 1 Thickness	5150A
Layer 2 Thickness	5150A
Layer 3 Thickness	7650A
Passivation	
Material	Z94: SiO2 / Nitride Oxide – Z92: SiO2 / Nitride
Thickness	Z94: 3000A / 15000A – Z92: 2600A / 6400A

3.2 Product Design

Die Size	4260µm * 4300µm (17.47mm2)
Pad Size Opening	80µm * 80µm
Logic Effective Channel Length	0.5µm
Gate Poly Width (min.)	0.50µm
Gate Poly Spacing (min.)	0.60µm
Metal 1 Width	0.60µm
Metal 1 Spacing	0.70µm
Metal 2 Width	0.80µm
Metal 2 Spacing	0.70µm
Metal 3 Width	0.80µm
Metal 3 Spacing	0.70µm
Contact size	0.60µm
Via 1 size	0.60µm
Via 2 size	0.60µm

Qualpack TS87C51RD2/TS83C51RD2

4 Qualification

4.1 Qualification Flow

General Requirements for Plastic packaged CMOS IC

Standard	Test Description	Qualification acceptance
MIL-STD 883D Method 1005	**Electrical Life Test (Early Failure Rate)** 12 hours 140°C / 5.75V	1/2000 - 12h
MIL-STD 883D Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 140°C / 5.75V Dynamic or Static	0/100 - 500h
MIL-STD 883D Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	0/3 per level
JEDEC 78	**Latch-up** 50mW power injection, 1.5 Vcc over voltage 125°C	0/5 per condition
Atmel Nantes PAQA0046	**MEMORY Data Retention** High Temperature Storage 165°C	0/50 - 500h
MIL-STD 883D Method 1010	**Temperature Cycling** 1000 cycles –65°C/150°C air/air	0/50 - 500c
Atmel Nantes PAQA0184	**Autoclave after Preconditioning** 144 hours 130°C/85%RH	0/50 - 72h
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH/5.5V	0/50 - 500h
EIA JESD22-A110	**HAST** 168 hours 130°C/85%RH/5.5V	0/50 - 168h
EIA JESD20-STD	**Resistance to Soldering Heat** Infra Red Stress 235°C/25s/3 times	0/10 per level
MIL-STD 883D Method 2003	**Solderability**	0/3
MIL-STD 883D Method 2015	**Marking Permanency**	0/3

4.2 Wafer Process Qualification

4.2.1 Process Module Reliability

This chapter contains all the information relative to the reliability of the SCMOS3 NV technology. Results presented in the following sections concern the reliability of the basic process steps which build up the technology.

4.2.1.1 Hot carrier qualification

STATIC NMOS DEGRADATION

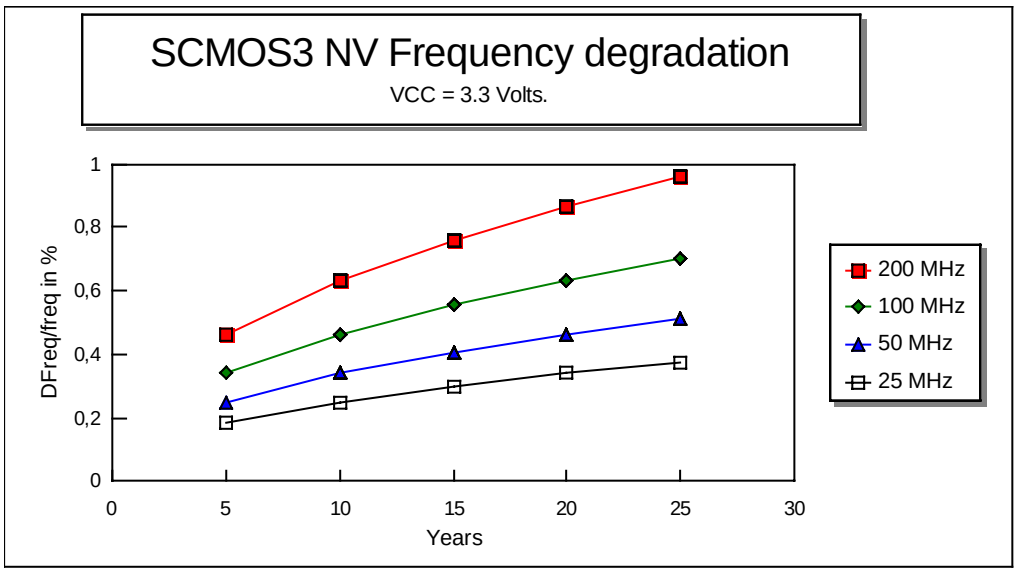
Channel length in µm	**0.5**	**0.55**	**0.6**	**0.65**	**0.7**	**0.5**
Process corner	Fast	Fast	Fast	Fast	Fast	Typical
Substrate current in µA/µm VD=5.5V, VG=2.25V	17	15	13.4	12.1	11.1	14.7
Substrate current in µA/µm VD=3.6V, VG=1.6V	0.35	0.3	0.25	0.22	0.2	0.3
Lifetime in seconds for 10% shift of Gm at VD=5.5V	3.2e3	3.7e3	4.2e3	4.7e3	5.2e3	3.8e3
Lifetime in seconds for 10% shift of Gm at VD=3.6V	8e7	10e7	12e7	14e7	16e7	10e7

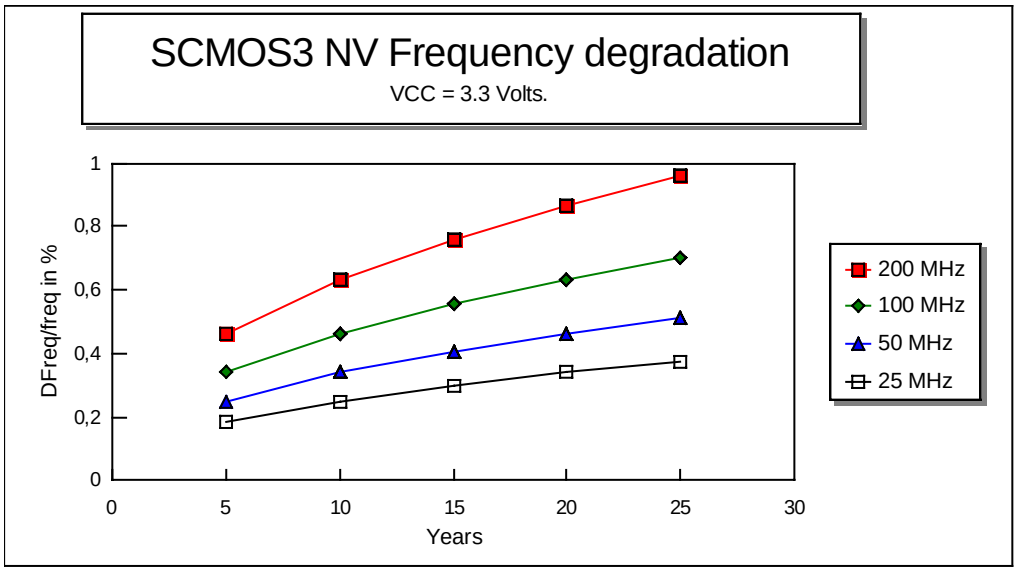
STATIC PMOS DEGRADATION

Channel length in µm	**0.5**	**0.55**	**0.6**	**0.65**	**0.7**	**0.5**
Process corner	Fast	Fast	Fast	Fast	Fast	Typical
Substrate current in µA/µm VD=5.5V, VG=2.25V	0.31	0.28	0.25	0.22	0.21	0.24
Substrate current in µA/µm VD=3.6V VG=1.25V	2.3e-3	1.9e-3	1.6e-3	1.4e-3	1.1e-3	1.6e-3
Lifetime in seconds for 10% shift of Gm at VD=5.5V	2.7e4	3.1e4	3.5e4	3.9e4	4.3e4	3.5e4
Lifetime in seconds for 10% shift of Gm at VD=3.6V	2e7	2.5e7	3e7	3.8e7	4.6e7	3.2e7

EXPERIMENTAL RESULTS IN DYNAMIC MODE : hot carrier degradation effects on inverter propagation time have been measured on oscillators running at 75 MHz at 7V and 6.5V. Accelerator factor in voltage is then carried out and expected degradation laws at 5V and 3.3V derived. The following graphs show the frequency degradation of oscillators running at 5V and 3.3V.

Qualpack TS87C51RD2/TS83C51RD2





4.2.1.2 Electro-migration

Characterization

Stresses of electro-migration are achieved for 1000 hours on 32 packaged metal line running on flat with a current density of $2x10^6$ A/cm² at a temperature of 200°C. Lines are declared to be failed for a shift of the initial resistance by 20%. Results are summarized in the table below.

Level	W/L/T(1)	Structure	Failures
Metal1	**2/2000/0.50**	**Ti/TiN/AlCu/TiN**	**no**
Metal2	**2/2000/0.50**	**Ti/TiN/AlCu/TiN**	**no**
Metal3	**2/2000/0.70**	**Ti/TiN/AlCu/TiN**	**no**

(1) W/L/T=Width/Length/Thickness of the metal line in microns

Lifetime projection

The objective of reliability is to reach less than 10 FIT on metal line within 10 years at a temperature of 150°C. As no failures have been found at 1000 hours in the above stress conditions a lifetime projection in FIT is meaningless.
However, assuming for AlCu metalization an activation energy in temperature Ea of 0.60eV and an activation in current with a power-law coefficient n of 2, the current density which guarantees no failures within 10 years at 150°C can be extrapolated.
With these assumptions the projected current density for no failures at 150°C within 10 years is calculated as $5x10^5$A/cm² which is much higher than the current density of $2x10^5$A/cm² specified in the design rules.

4.2.1.3 Time Dependent Dielectric Breakdown

4.2.1.3.1 Field oxide

QBD MEASUREMENT:

The critical charge, supported by the thin oxide and related to the extrinsic and intrinsic defects, is measured on TOX/P- and TOX/N- capacitors. The tested capacitor areas are varying from 4.10^{-4} to 5.10^{-2} cm². Two types of capacitors with poly overlaping the field oxide (DEC) and poly non overlaping the field oxide (INC) are measured. The distributions have been obtained from 750 measurements for each area and type of capacitors on 10 different lots.

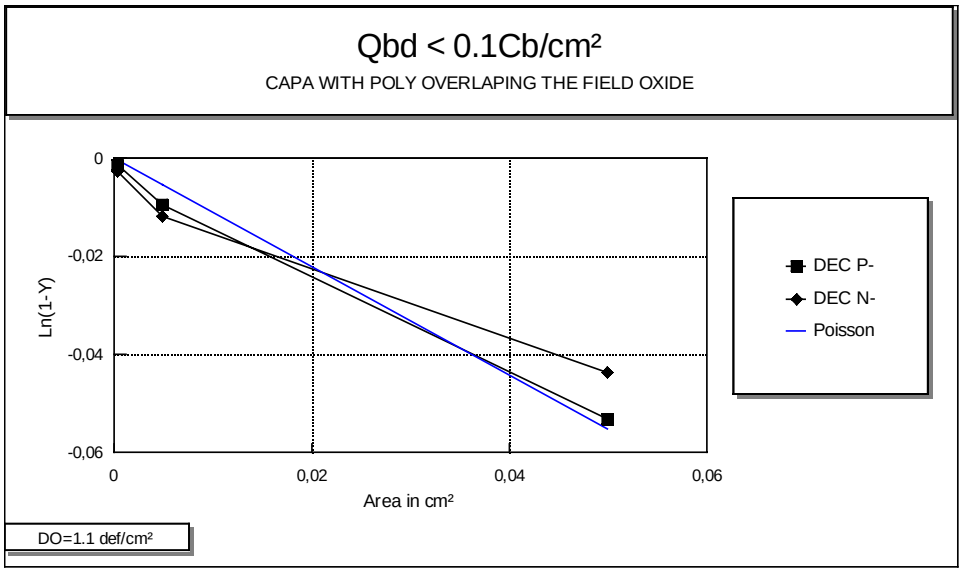
Extrinsic defects:

The two graphs here after represent the % of failures vs area for Qbd below or equal to 0.1 Cb/cm². The law of Poisson is used to determine the D0 defect density of the extrinsic defects:

$$Y=1-\exp(-\text{Area} * DO)$$

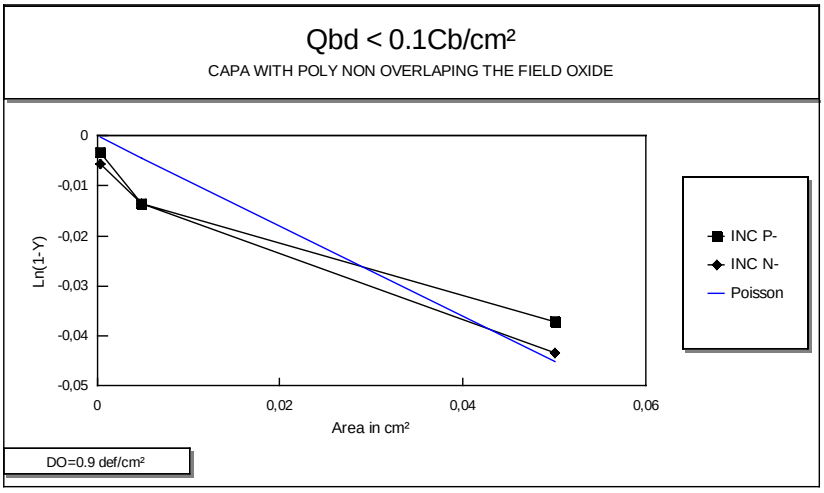
Poly overlaping the Field oxide on Tox/P- and Tox/N-:

The DO is found to be 1.1 def/cm². This result is in agreement with the goal for DO of 1 def/cm².



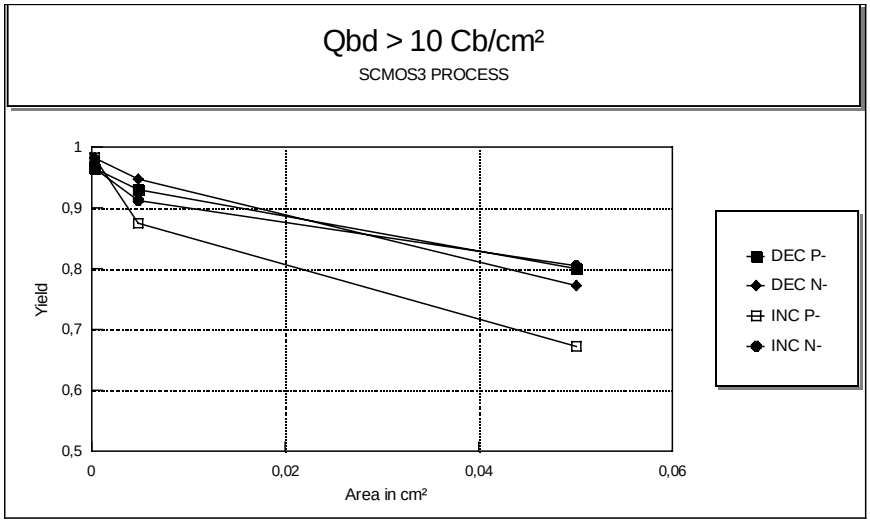
Poly non overlaping the Field oxide on Tox/P- and Tox/N-:

The DO is found to be 0.9def/cm². This result is in agreement with the goal for DO of 1 def/cm².



Intrinsic defects:

The graph here after represents the percentage of failure for a Qbd > 10 Cb/cm² vs the area. The worst case given by the bigest capacitors shows that 67% of the total distribution has a Qbd > 10 Cb/cm². This result guarantees a good reliability behaviour. The critical charge, supported by thin oxide and related to the extrinsic defects, is measured on TOX/P- capacitors of 42570µm² and TOX/N- capacitors of 85140µm². Following are the average results obtained on recent lots from a distribution of about 60 sites per wafer. The minimum specification limit is 10C/cm².



4.2.1.3.2 High Voltage MOS Gate oxide transistors

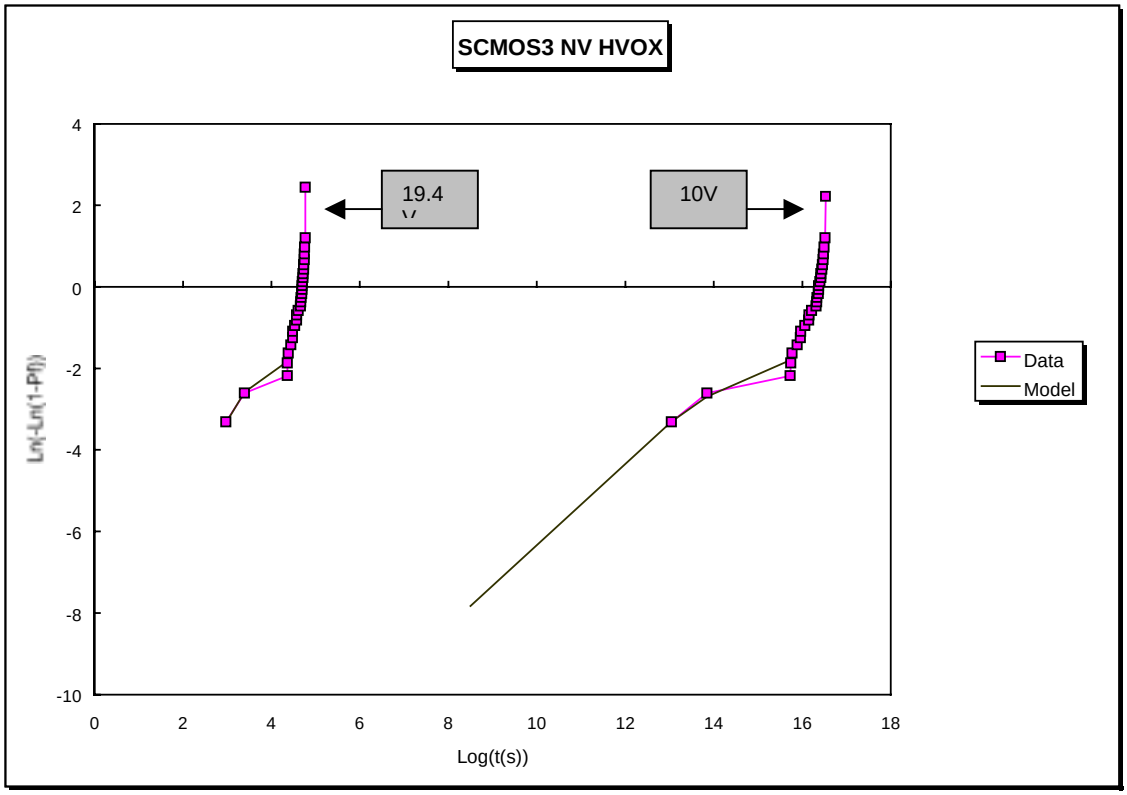
High voltage gate oxide transistors are used within the EPROM circuits to increase the external programming voltage up to 14.5 Volts. This operation is needed to reach the appropriate programming conditions. As a result, the maximum voltage between gate and source/drain of high voltage MOS transistors can be about 10 Volts .

The experiment consists of the application of an accelerated constant voltage stress until the breakdown of the oxide is reached. The time of the breakdown is then extrapolated for nominal voltage condition.

The capacitor is made with a 20nm oxide growth on P- substrate and the electrode is phosphorus doped poly : the capacitor area is 0.23 mm².
The Time Dependant Dielectric Breakdown is accelerated in voltage and temperature.The temperature is set to 150°C so no acceleration factor depending on temperature is needed for the extrapolation of product lifetime. An unique accelerated electrical field of 9 MV/cm (19.4V for this oxide thickness) has been applied.

The experiment has been performed on capacitors issued from 3 wafers coming from 3 different lots : a set of 28 capacitors has been stressed.

A cumulative plot of failures obtained first at 19.4V and the second one projected to 10V with the relevant model are presented on the following figure :



Qualpack TS87C51RD2/TS83C51RD2

The model predicts a failure level of about 1 ppm for 640 seconds at 150°C far above the specification of 0.01% then the High Voltage MOS gate oxide is qualified.

Conclusion:

The QBD results demonstrate high reliability level of SCMOS3 NV thin oxide.

Qualpack TS87C51RD2/TS83C51RD2

4.3 T87C51RD2 Qualification Tests

This section summarizes the cumulated package level qualification data of the TS87C51RD2.

4.3.1 Design tests

Lots	Device Type	Test Description	Step	Result	Comment
Z28303C Z34922E Z33543	**TS87C51RD2** PLCC44	EFR Dynamic Life Test	12h	0/900	EFR: 0 ppm
		LFR Dynamic Life Test	500h 1000h	0/300 0/300	LFR: 19 fit
		Data Retention 165°c	500h 1000h	0/150 0/150	
Z28882	**TS83C51RD2** DIL 40.6	ESD	3000v 4000v	0/3 0/3	Class 3
		Latch-up	50mW 7.5v	0/5 0/5	Latch-up free

4.3.2 Package tests

Lots	Device Type	Test Description	Step	Result	Comment
Z28303C Z34922E Z33543	**TS87C51RD2** PLCC44	85/85 Humidity	500h 1000h	0/150 0/150	
		Thermal Cycles	500c 1000c	0/150 0/150	
		Moisture preconditioning Level 1 Thermal Sh. -65°c/150°c HAST 130°c/85%rh	CSAM Test 15ts 72h 144h	0/30 0/180 0/150 0/150 0/150	Pass level 1 of JEDEC 20
Z25873C	PLCC44	Marking permanency (resistance to solvents)	-	0/3	
		Solderability	-	0/3	

4.3.3 Qualification status

The TS87C51RD2 and TS83C51RD2 have been qualified in July 1999.

5 Environmental Information

The Atmel Nantes Environmental Policy aims are :

- Reducing the use of harmful chemicals in its processes
- Reducing the content of harmful materials in its products
- Using re-cyclable materials wherever possible
- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by Atmel Nantes or its sub-contractors' process.

Atmel Nantes site is ISO14001 certified since May 2000.

Qualpack TS87C51RD2/TS83C51RD2

6 Other Data

6.1 ISO9001 and QS900 Certificates

CERTIFICAT AFAQ CERTIFICATE

N° QS/1999/12758

AFAQ certifie que le système qualité adopté par,
AFAQ certifies that the quality system developed by :

MHS SA

pour les activités suivantes,
for the following activities :

CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.

DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.

exercées sur le(s) site(s) suivant(s),
carried out in the following location(s) :

La Chantrerie BP 70602 F-44306 NANTES CEDEX 3

a été évalué conformément au code de déontologie de l'annexe B du QS-9000
et jugé conforme aux exigences des référentiels,
has been assessed in accordance with QS-9000 appendix B code of practice
and found to conform to the requirements of the standards :

ISO 9001 (1994) QS-9000 (03/98)

Le présent certificat, délivré dans les conditions fixées par AFAQ, est valable à dater du,
This certificate, delivered under AFAQ rules, is valid as from :

2000-07-18

(année-mois-jour) *jusqu'au / until** **2003-07-17** (year-month-day)

DG/X/0700.1-1997/10

LE PRÉSIDENT DU COMITÉ DE CERTIFICATION / *THE PRESIDENT OF THE CERTIFICATION COMMITTEE* — A. PIGEONNIER

LE DIRECTEUR GÉNÉRAL D'AFAQ / *THE MANAGING DIRECTOR OF AFAQ* — O. PEYRAT

LE REPRÉSENTANT DE L'ENTREPRISE / *ON BEHALF OF THE FIRM* — F. FAES

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AFAQ - 116, AVENUE ARISTIDE BRIAND - BP 40 / F-92224 BAGNEUX CEDEX FRANCE

6.2 Data Book Reference

The data sheet is available upon request to sales representative or upon direct access on ATMEL Wireless and Microcontrollers web site:

http://www.atmel-wm.com/

TS87C51RD2 8-bit Microcontroller

Address References
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