TSH343

280MHz Single-Supply Triple Video Buffer

- Bandwidth: 280MHz
- 5V single-supply operation
- Internal input DC level shifter
- No input capacitor required
- Internal gain of 6dB for a matching between 3 channels
- Very low harmonic distortion
- Slew rate: 780V/µs
- Specified for 150Ω and 100Ω loads
- Tested on 5V power supply
- Data min. and max. are tested during production

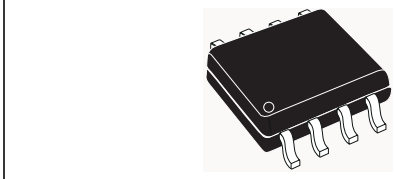
Description

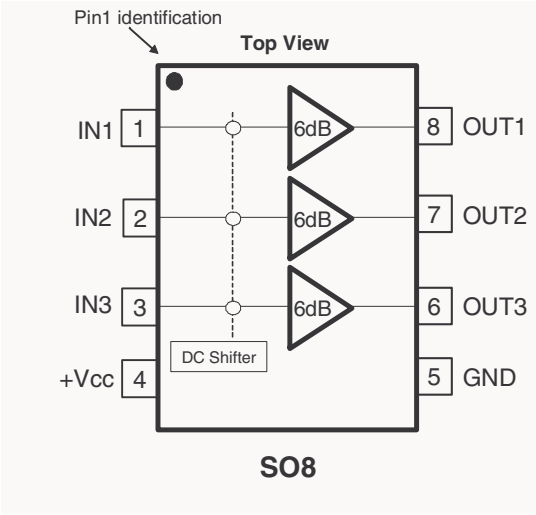
The TSH343 is a triple single-supply video buffer featuring an internal gain of 6dB and a large bandwidth of 280MHz.

The main advantage of this circuit is that its input DC level shifter allows for video signals on 75Ω video lines without damage to the synchronization tip of the video signal, while using a single 5V power supply with no input capacitor. The DC level shifter is internally fixed and optimized to keep the output video signals between low and high output rails in the best position for the greatest linearity. *Chapter 4* of this datasheet gives technical support when using the TSH343 as Y-Pb-Pr driver for video DAC output on a video line (see TSH344 for RGB signals).

The TSH343 is available in the compact SO8 plastic package for optimum space-saving.

Pin Connections (top view)





SO8

Applications

- High-end video systems
- High Definition TV (HDTV)
- Broadcast and graphic video
- Multimedia products

Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TSH343ID	-40°C to +85°C	SO-8	Tube	TSH343I
TSH343IDT			Tape & Reel	TSH343I

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{in}	Input Voltage Range (2)	0 to +1.4	V
T_{oper}	Operating Free Air Temperature Range	-40 to +85	°C
T_{std}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	SO8 Thermal Resistance Junction to Case	28	°C/W
R_{thja}	SO8 Thermal Resistance Junction to Ambient Area	157	°C/W
$P_{max.}$	Maximum Power Dissipation (@Ta=25°C) for Tj=150°C	800	mW
ESD	CDM: Charged Device Model HBM: Human Body Model MM: Machine Model	2 1.5 200	kV kV V

1. All voltage values, except differential voltage, are with respect to network terminal.
2. The magnitude of input and output voltage must never exceed V_{CC} +0.3V.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	3 to 5.5(1)	V

1. Tested in full production at 0V/5V single power supply

2 Electrical Characteristics

Table 3. V_{CC} = +5V Single Supply, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC Performance						
V_{DC}	Input DC shift	R_L = 150Ω, T_{amb}	0.4	0.6	0.8	mV
		-40°C < T_{amb} < +85°C		0.53		
I_{ib}	Input Bias Current	T_{amb} , input to GND		18.2	35	µA
		-40°C < T_{amb} < +85°C		20.7		
Rin	Input Resistance	T_{amb}		4		GΩ
Cin	Input Capacitance	T_{amb}		1		pF
I_{CC}	Supply Current per Buffer	no Load, input to GND		14.4	18	mA
		-40°C < T_{amb} < +85°C		14.9		
PSRR	Power Supply Rejection Ratio 20 log ($\Delta V_{out}/\Delta V_{CC}$) (see *Figure 25* and *Figure 26*)	input to GND, F = 1MHz C_{LF}=470nF C_{HF}=100uF		70		dB
G	DC Voltage Gain	R_L = 150Ω, V_{in} = 1V	1.92	1.99	2.05	V/V
DG	Variation of the DC Voltage Gain between inputs of 0.3V and 1V	Input step from 0.3V to 1V		0.26	0.8	%
MG_1	Gain Matching between 3 channels	Input = 1V		0.5	2	%
$MG_{0.3}$	Gain Matching between 3 channels	Input = 0.3V		0.5	2	%
Dynamic Performance and Output Characteristics						
Bw	-3dB Bandwidth	Small Signal V_{out} = 20mVp R_L = 150Ω	160	280		MHz
	Gain Flatness @ 0.1dB	Small Signal V_{out} = 20mVp R_L = 150Ω		65		
FPBW	Full Power Bandwidth	V_{out} = $2V_{p-p}$, V_{ICM} = 0.5V, R_L = 150Ω	130	200		MHz
D	Delay between each channel (see *Figure 30*)	0 to 30MHz		0.5		ns
SR	Slew Rate (1)	Input step from 0V to 1V, R_L = 150Ω	500	780		V/µs
V_{OH}	High Level Output Voltage	$V_{in\ DC}$ = +1.5V, R_L = 150Ω	3.7	3.9		V
V_{OL}	Low Level Output Voltage	R_L = 150Ω		40		mV
I_{OUT}	Output Current	V_{out} = 2V, T_{amb}	45	90		mA
		-40°C < T_{amb} < +85°C		82		
	Output Short Circuit Current (Isource)			100		mA

Table 3. V_{CC} = +5V Single Supply, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Noise and Distortion						
eN	Total Input Voltage Noise	F = 100kHz, R_{IN} = 50Ω		29		nV/√Hz
		10kHz to 30MHz 10kHz to 100MHz		158 290		µVrms
HD2	2nd Harmonic Distortion	V_{out} = 2Vp-p, R_L = 150Ω F= 10MHz F= 30MHz		 -58 -45		dBc
HD3	3rd Harmonic Distortion	V_{out} = 2Vp-p, R_L = 150Ω F= 10MHz F= 30MHz		 -72 -50		dBc

1. Non-tested value. Guaranteed value by design.

Figure 1. Frequency response

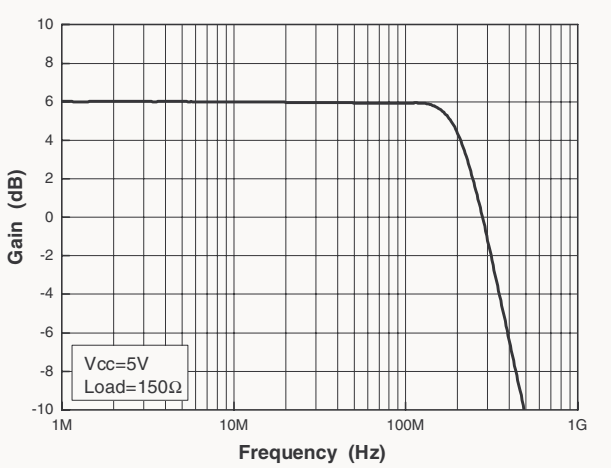


Figure 2. Gain flatness

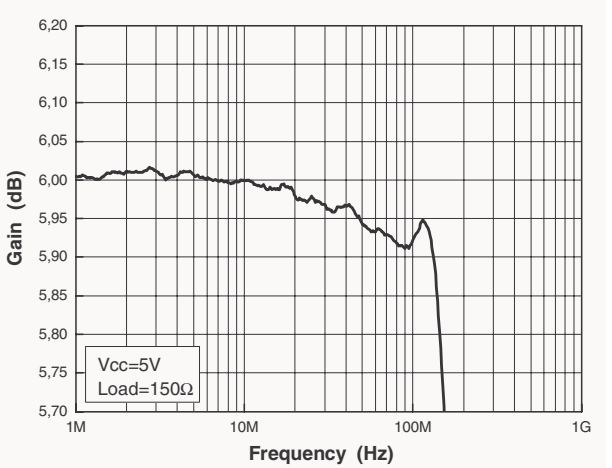


Figure 3. Cross-talk vs. frequency (amp1)

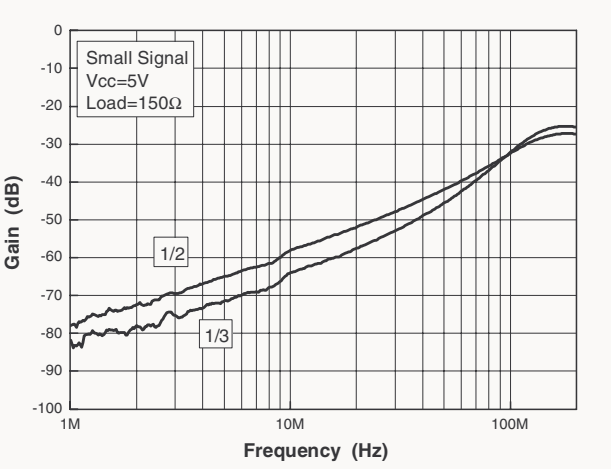


Figure 4. Cross-talk vs. frequency (amp2)

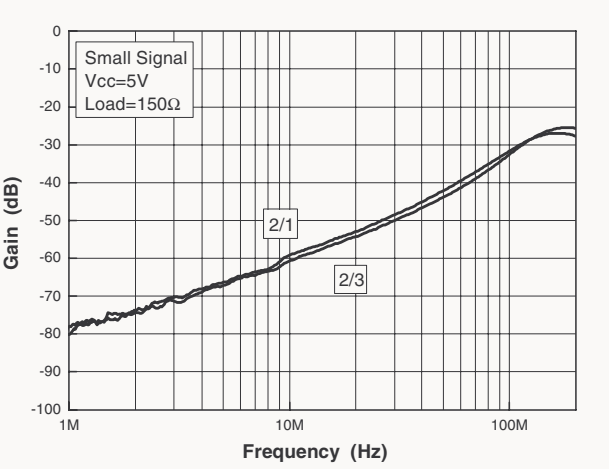


Figure 5. Cross-talk vs. frequency (amp3)

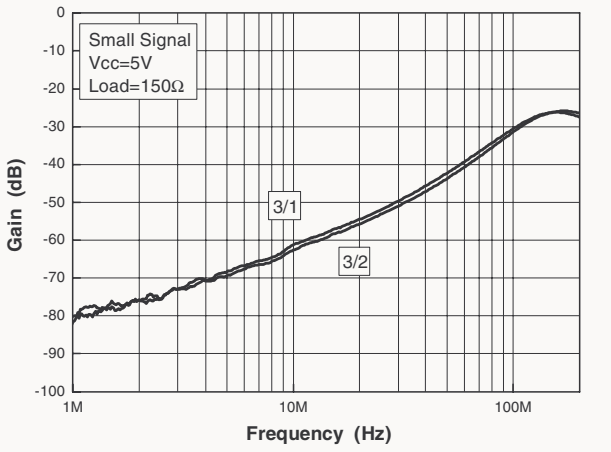


Figure 6. Input noise vs. frequency

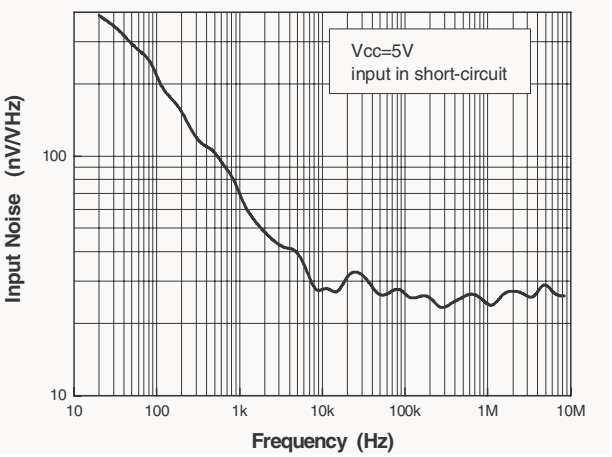


Figure 7. Distortion on 150Ω load - 10MHz

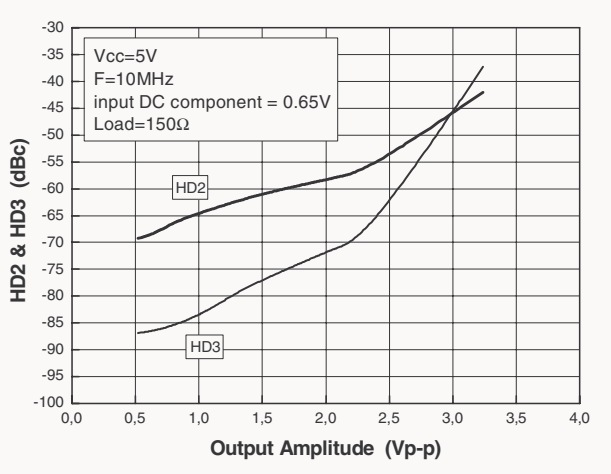


Figure 8. Distortion on 100Ω load - 10MHz

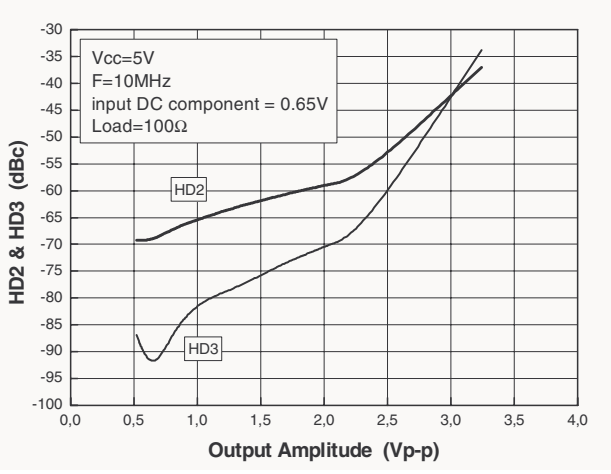


Figure 9. Distortion on 150Ω load - 30MHz

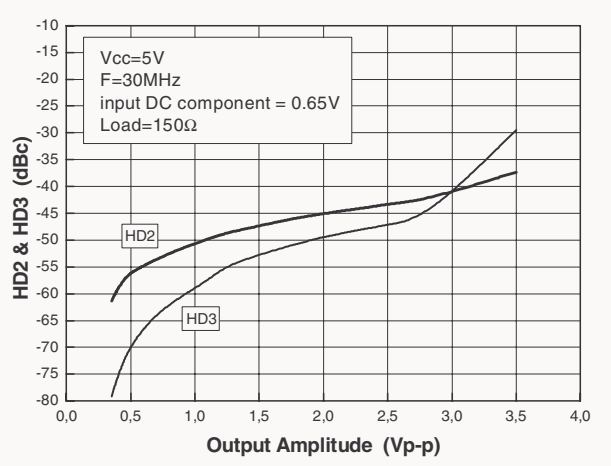


Figure 10. Distortion on 100Ω load - 30MHz

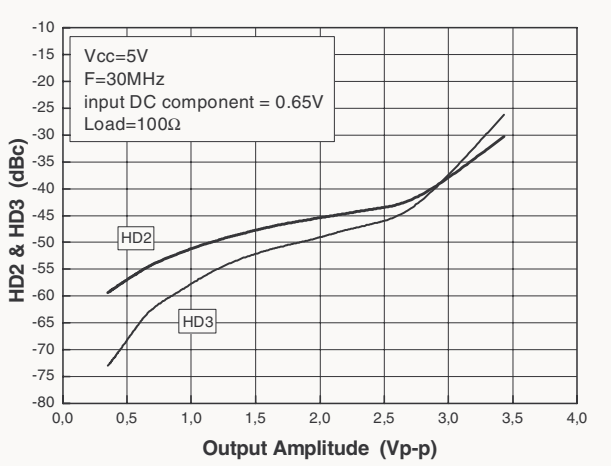


Figure 11. Output DC shift vs. frequency

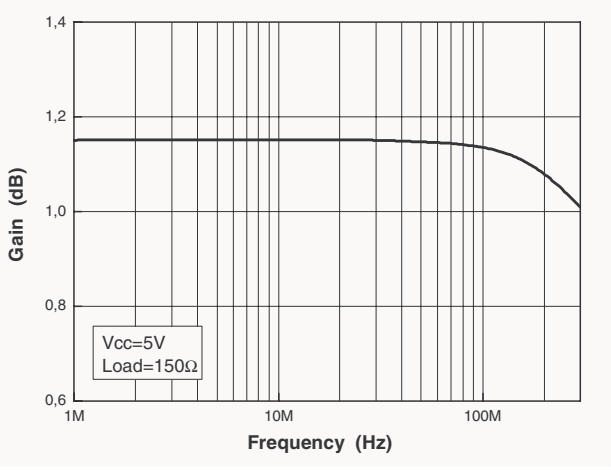


Figure 12. Slew rate

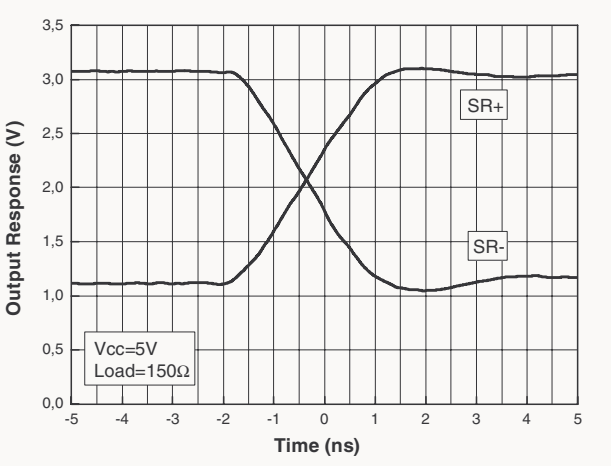


Figure 13. Reverse isolation vs. frequency

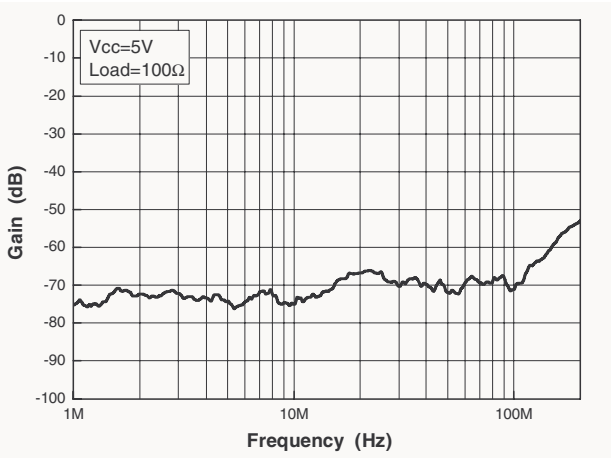


Figure 14. Bandwidth vs. temperature

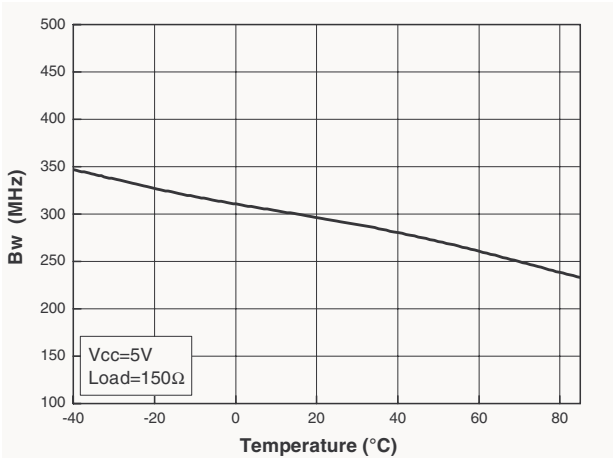


Figure 15. Quiescent current vs. Supply

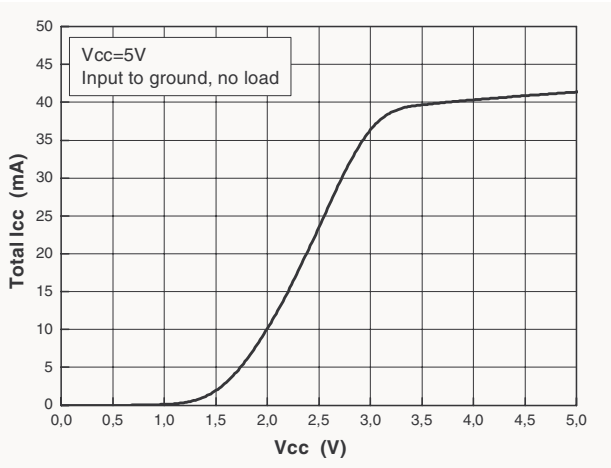


Figure 16. Input DC shift vs. temperature

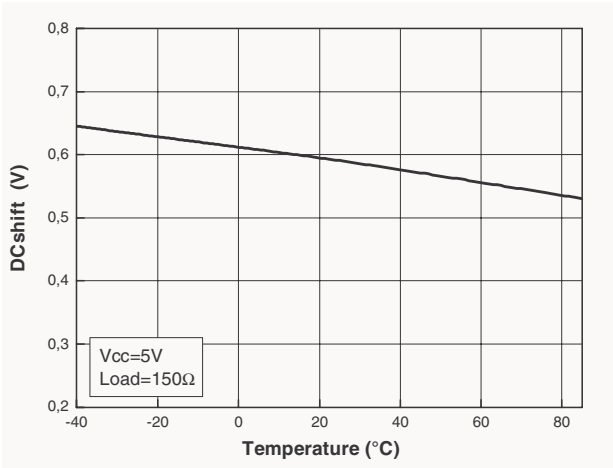


Figure 17. Isource vs. output voltage

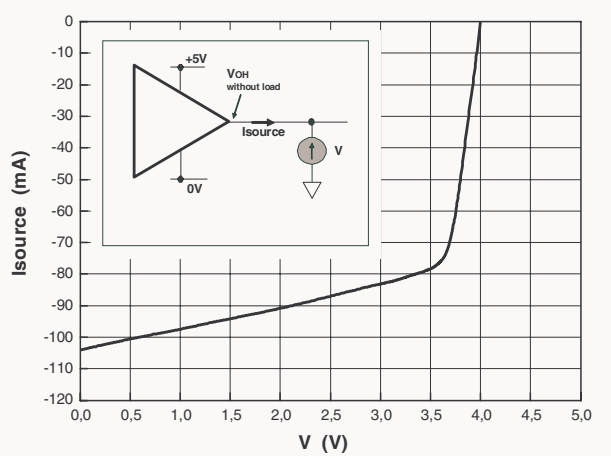


Figure 18. Voltage gain vs. temperature

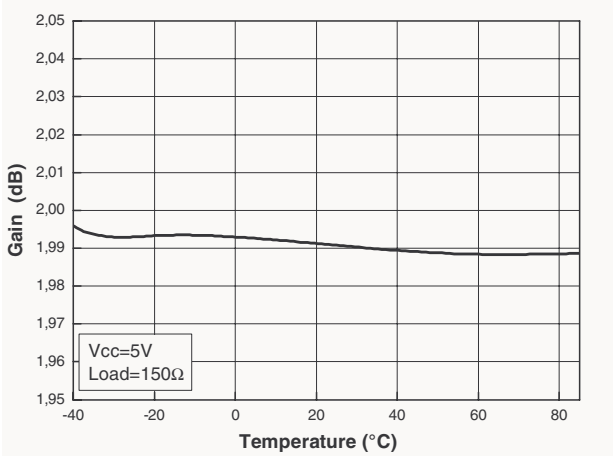


Figure 19. Ibias vs. temperature

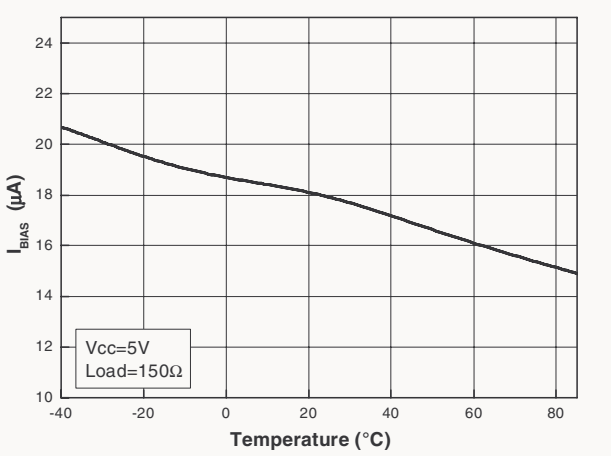


Figure 20. Gain deviation vs. temperature

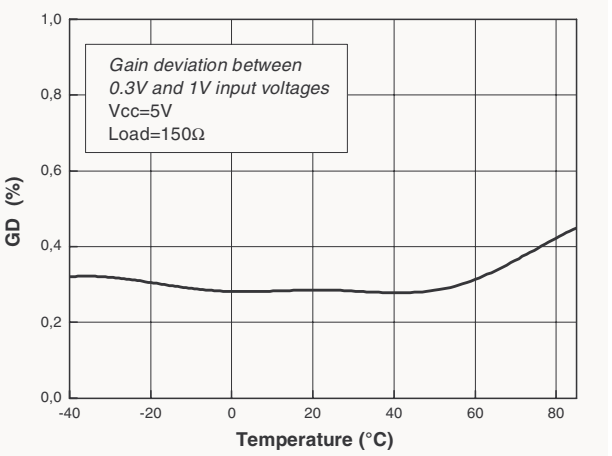


Figure 21. Supply current vs. temperature

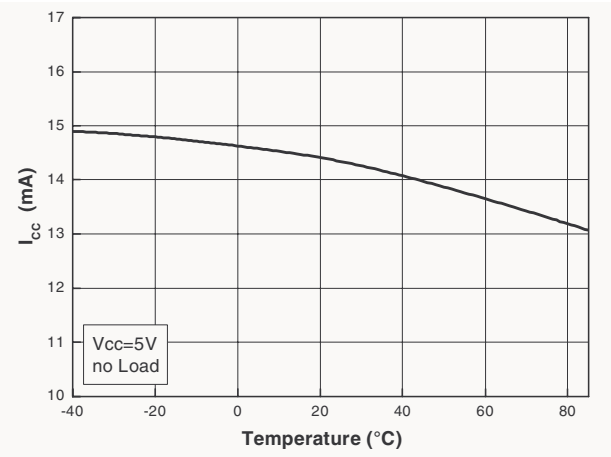


Figure 22. Output current vs. temperature

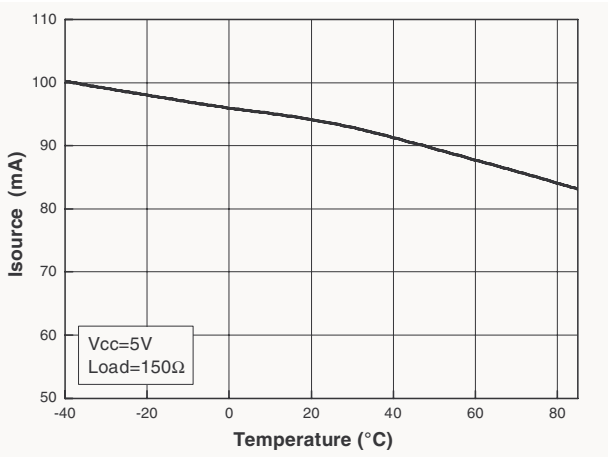


Figure 23. Output higher rail vs. temperature

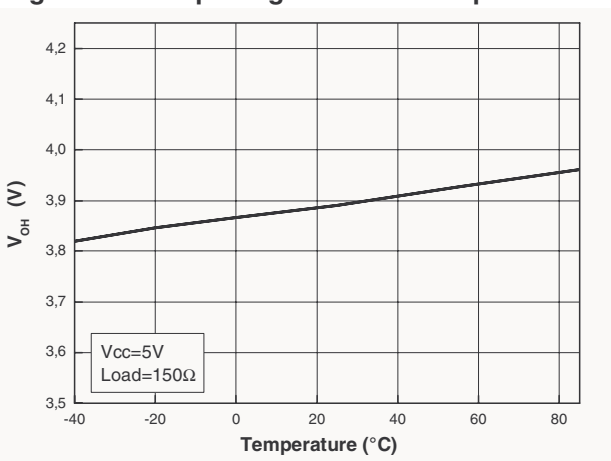
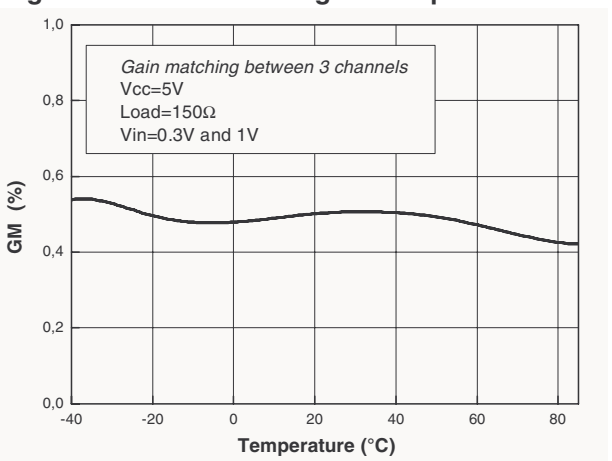


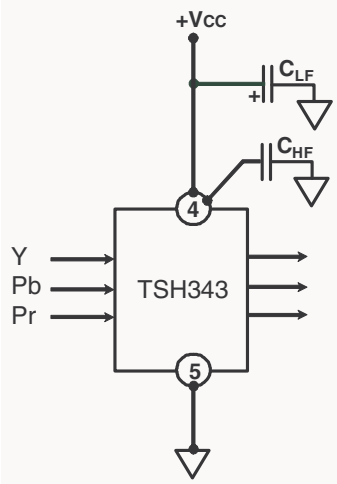
Figure 24. Gain matching vs. temperature



3 Power Supply Considerations and improvement of the PSRR

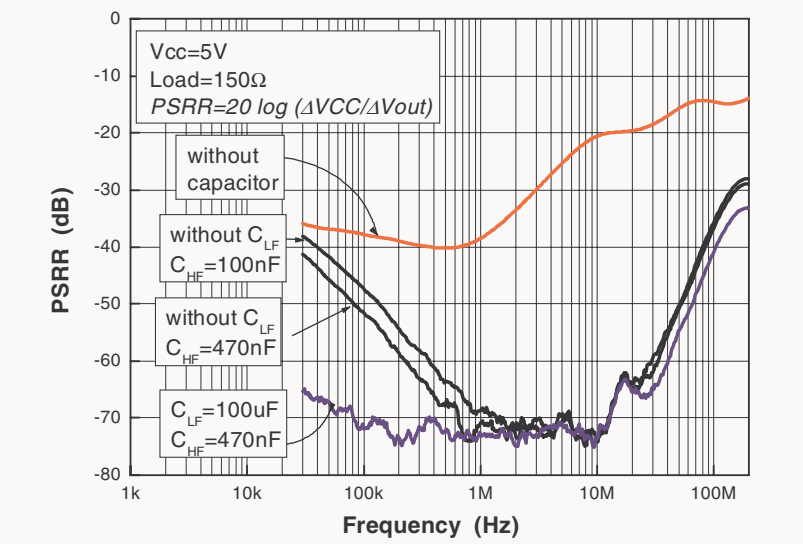
Correct power supply bypassing is very important for optimizing performance in low and high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pin (pin 4) to improve high-frequency bypassing. A capacitor (C_{LF}) greater than 100uF is necessary to improve the PSRR in low frequencies. For better quality bypassing, a capacitor of 470nF (C_{HF}) is added using the same implementation conditions to improve the PSRR in the higher frequencies.

Figure 25. Circuit for power supply bypassing



The following graph in *Figure 26* shows the evolution of the PSRR against the frequency when the power supply decoupling is achieved carefuly or not.

Figure 26. PSRR improvement



4 Using the TSH343 to Drive Y-Pb-Pr Video Components

Figure 27. Shapes of video signals coming from DACs

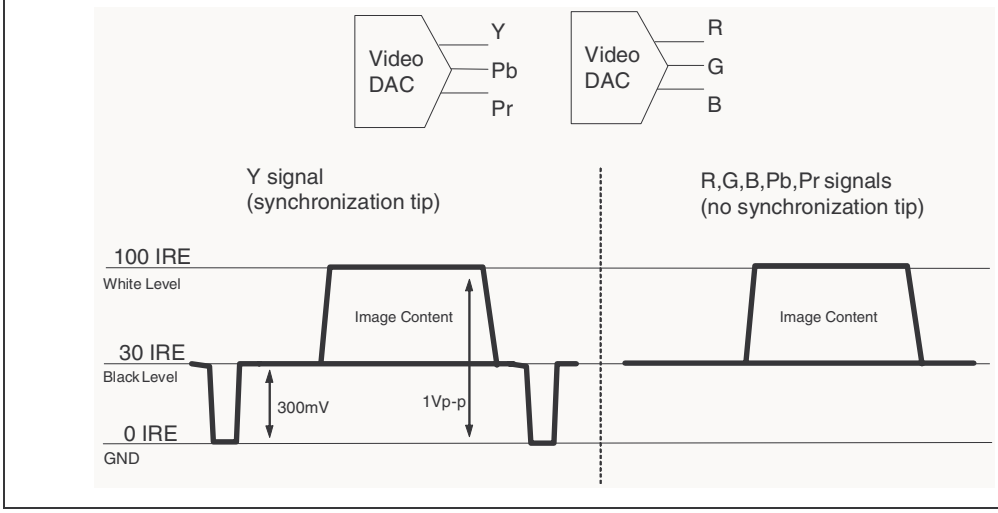


Figure 28. Implementation of the video driver on output video DACs

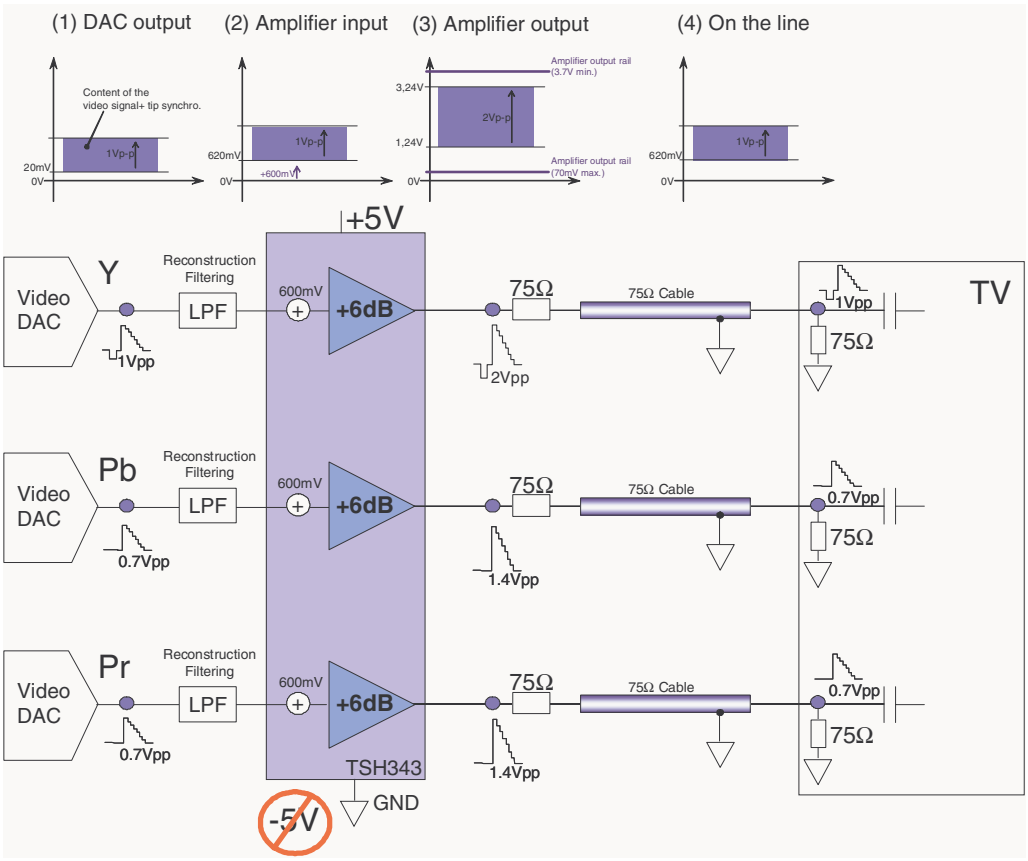


Figure 28 shows a schematic diagram of the use of the TSH343 to drive video output from DACs.

The TSH343 is used to drive high definition video signals up to 30MHz on 75-ohm video lines. It is dedicated to driving YPbPr signals where the synchronization tip—close to zero volts—is included in Y signal, as seen in (1). An internal input DC value of 600mV is added to the video signal in order to shift the bottom from 0V to 600mV as seen in (2).

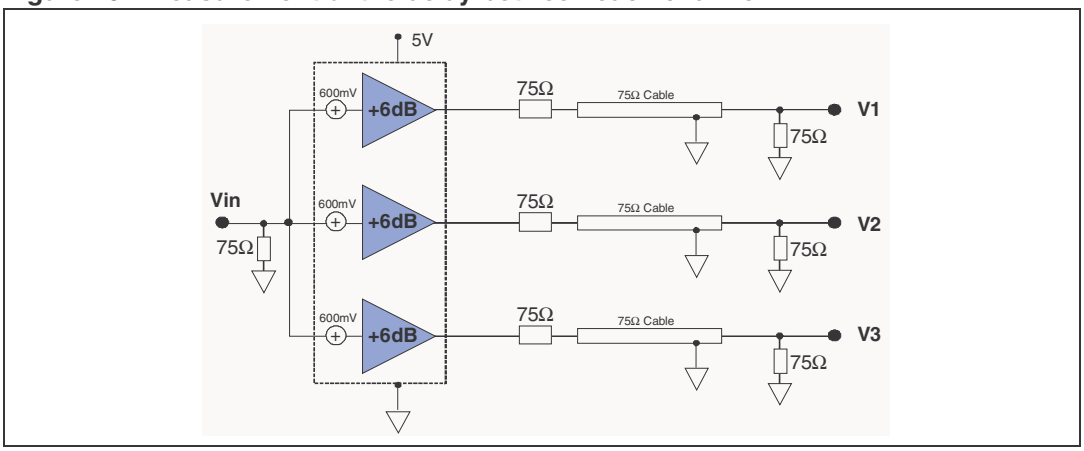
The shift is not based on the average of the signal, but is an analog summation of a DC component to the video signal. Therefore, no input capacitors are required which provides a real advantage in terms of cost and board space.

Under these conditions, it is possible to drive the signal in single supply without any saturation of the driver against the lower rail.

Assuming that we lose half of the signal by output impedance-matching in order to properly drive the video line, the shifted signal is multiplied by a gain of 2 or +6dB (3).

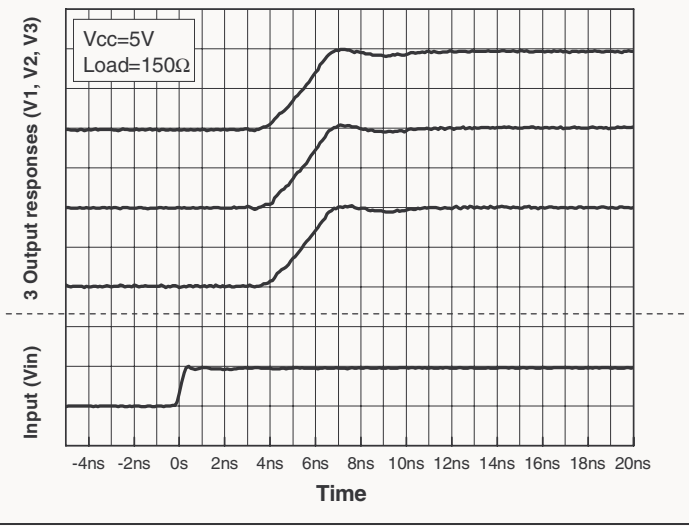
4.1 Delay between channels

Figure 29. Measurement of the delay between each channel



Delay between each video component is an important aspect in high definition video systems. To drive porperly the three video components without any relative delay, the dice of the TSH343 is layouted out with a very symetrical geometry. The effect is direct on the synchronization of each channel, as shown in *Figure 30*. No delay appears between each channel when the same Vin signal is applied on the three inputs. Note that the delay from the inputs the outputs equals 4ns.

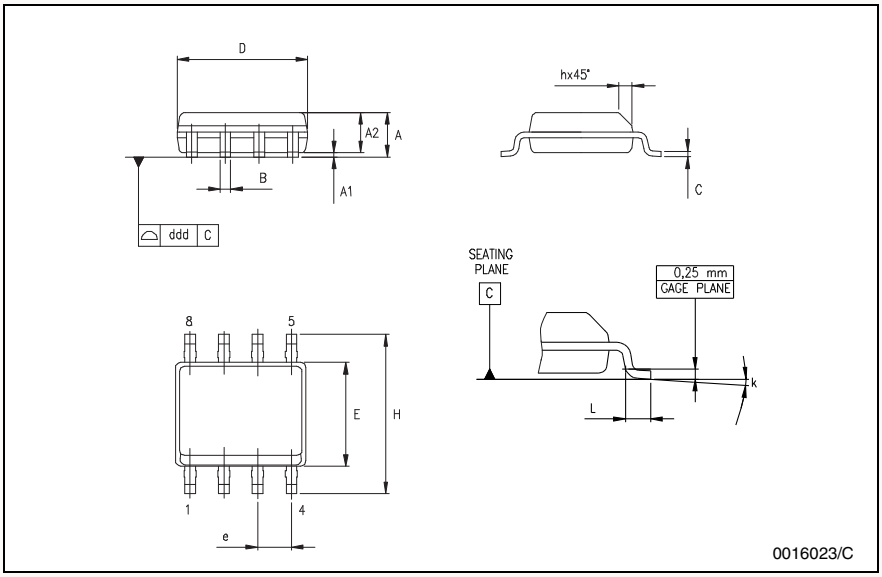
Figure 30. Relative delay between each channel



5 Package Mechanical Data

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



6 Revision History

Table 4. Document revision history

Date	Revision	Description of Changes
Dec. 2005	1	First release of datasheet.
Jan. 2006	2	Capa-load option paragraph deleted in page 11.