## Features

- **Two Identical Interface Channels**
- **Pre-regulated Smoothed Voltage and a Supply Current up to 50 mA for the Sensors**
- **Data from the Sensors by Current Modulation with a Transmission Rate of 60 kBaud (Transmission Bandwidth 500 kHz)**
- **TTL-compatible Input Activates the Sensor**
- **Data Output Can be Directly Connected to a Microcontroller Input**
- **Operation Supply Voltage Range 5.7V ≤ $V_S$ ≤ 40V**
- **ESD Protection According to MIL-STD-883C Test Method 3015.7**
- **High-level EMI Protection**

Pb Lead Free

## Benefits

- **Simple Wiring Thanks to One Common Line for Supply of the Sensor and Data Transmission from the Sensor to the U6268B**
- **Current Modulation Provides High Noise Immunity for Data Transfer**

# Side-airbag Sensor Dual Interface

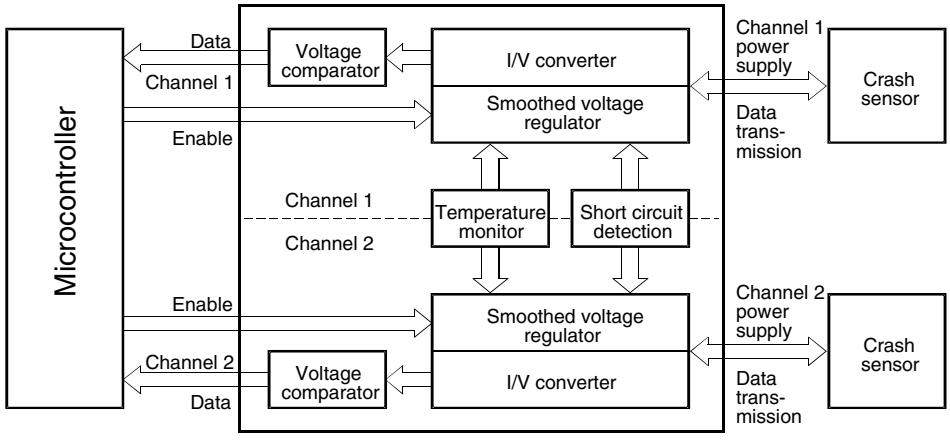
# U6268B

## 1. Description

The U6268B is an interface IC for remote automotive sensors. It links the crash sensors in the driver and passenger door with the main airbag unit in the dashboard. Two identical channels supply the external sensors and receive digital information from them via one active wire each. The interface supplies the external sensors with a pre-regulated smoothed voltage, the external units transmit the digital information back to the interface by current modulation.

As the device is designed for safety-critical applications, the highest data transmission security is mandatory. With high immunity against cross coupling between the two channels, the U6268B is tailored for the harsh automotive environment.

**Figure 1-1.** Block Diagram




Rev. 4808B–AUTO–09/05

## 2. Pin Configuration

**Figure 2-1.** Pinning SO16

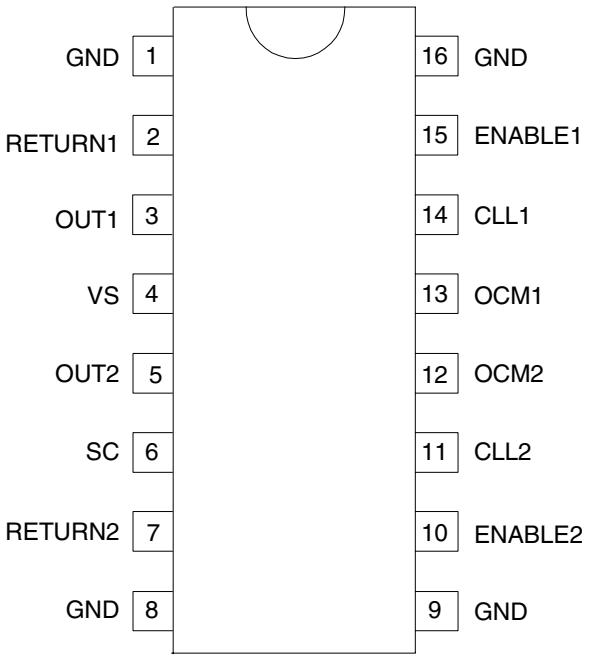
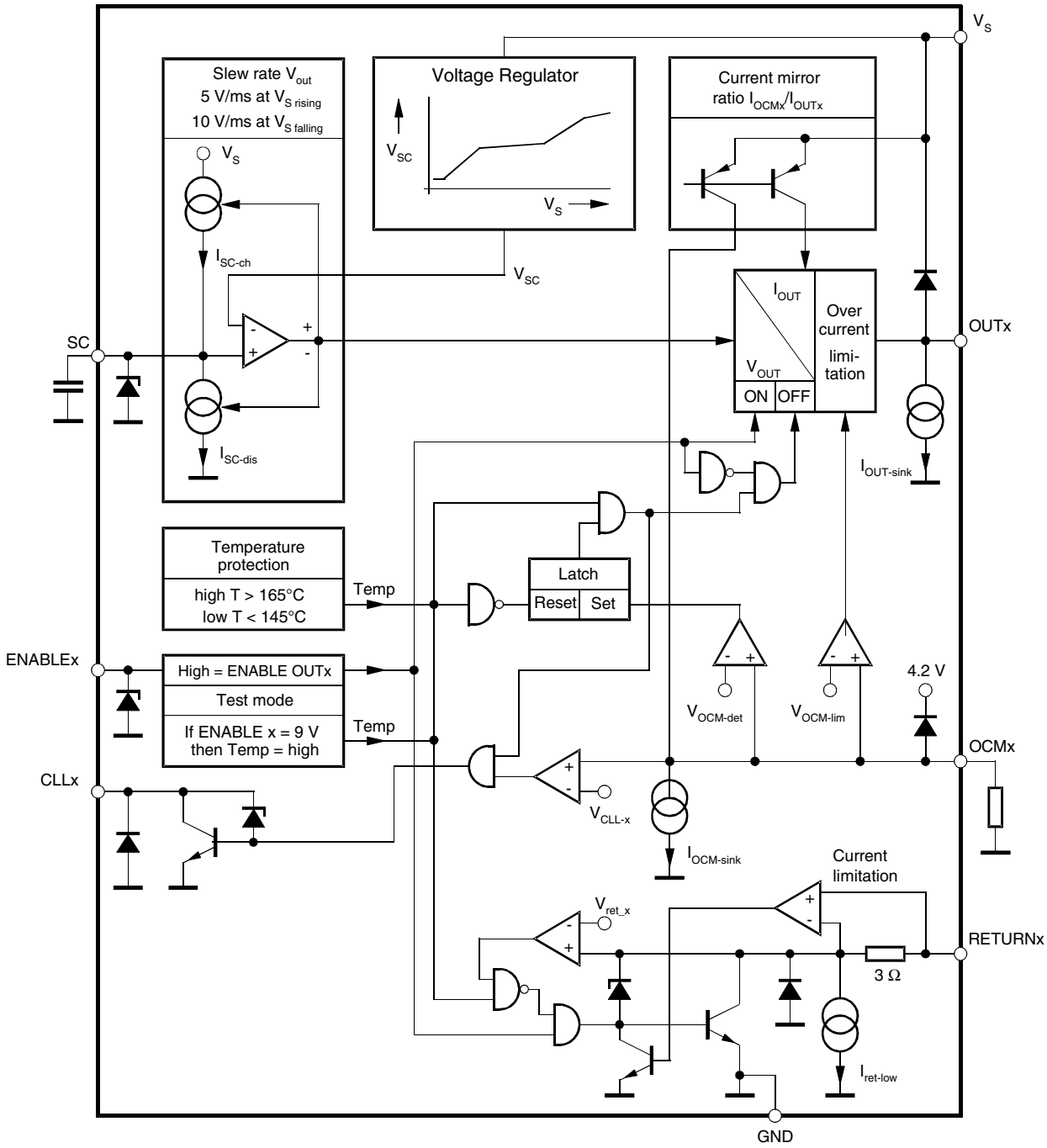



**Table 2-1.** Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | Ground and reference pin |
| 2 | RETURN1 | Return line of the external unit, internally connected to GND via a line-protection transistor |
| 3 | OUT1 | Voltage-stabilized supply output and current-modulation input |
| 4 | VS | Supply voltage of the IC |
| 5 | OUT2 | Voltage-stabilized supply output and current-modulation input |
| 6 | SC | Smooth time constant for slow voltage change at both OUT pins |
| 7 | RETURN2 | Return line of the external unit, internally connected to GND via a line-protection transistor |
| 8, 9 | GND | Ground and reference pin |
| 10 | ENABLE2 | Controls OUT1 voltage<br>ENABLE1 High = OUT1 active, ENABLE1 Low or open = OUT1 switched off |
| 11 | CLL2 | Current logic level output (low at high OUT2 current, monitoring via OCM2) |
| 12 | OCM2 | Analog current output, representing 1/10 current of OUT2 |
| 13 | OCM1 | Analog current output, representing 1/10 current of OUT1 |
| 14 | CLL1 | Current logic level output (low at high OUT1 current, monitoring via OCM1) |
| 15 | ENABLE1 | Controls OUT2 voltage<br>ENABLE2 High = OUT2 active, ENABLE1 Low or open = OUT2 switched off |
| 16 | GND | Ground and reference pin |

**Figure 2-2.** Functional Block Diagram



# 3. Functional Description

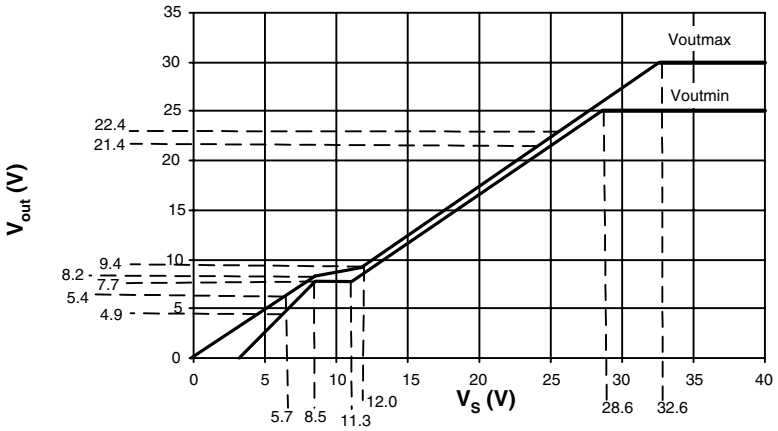
## 3.1 $V_S$

The IC and the external units are powered via the $V_S$ pin 4. This pin is connected to the battery via a reverse battery protection diode. An electrolythic capacitor of 22 µF smoothes the voltage and absorbs positive and negative transients.

## 3.2 OUT1, OUT2

OUTx provides a smoothed, very slowly changing supply voltage for the external units and monitors the output current. During normal operating conditions, the OUTx voltage is typically 3V below $V_S$, and changes very slowly with a varying battery voltage in order to suppress disturbances in the data transmission. At low $V_S$ (5.7V to 8.5V), the OUTx voltage is typically 0.5V below $V_S$. This voltage difference is reduced in to ensure sufficient supply voltage for the external unit between OUTx and RETURNx. The output current capability is 50 mA. The internal pull-down current at OUTx is typically 3 mA.

**Figure 3-1.** Output Voltage with Tolerances versus Supply Voltage




The data transmission from the external unit to the interface IC is carried out on the same line by varying the current level. The quiescent current consumption of the external unit is about 5 to 15 mA. This current level is interpreted as logic high level at the CLL pin. The external unit can switch on an additional current of 30 mA, interpreted by the interface as logic low. The slope time of the current pulse is approximately 1 µs which is suitable for a transmission rate up to 60 kBaud. The necessary transmission bandwidth of greater than 500 kHz between OUTx and OCMx is guaranteed (see “Application Circuit” on page 12). To achieve good current transmission behavior, the dynamic resistance of OUTx may not exceed 12Ω within the bandwidth range (total of 15Ω for OUTx and RETURN).

The OUTx voltage can be switched off by ENABLEx = LOW to reset the external unit and to reduce power dissipation during fault conditions.

The OUT pins are protected against overtemperature and short circuits. A reverse polarity diode at pin $V_S$ (pin 4) ensures that no current is fed back to the $V_{Batt}$ system in the case of a short between OUTx and $V_{Batt}$. A minimum capacity of 33 nF is required at the pins OUTx.

## 3.3 ENABLE1, ENABLE2

ENABLEx is a microcontroller-compatible input which switches the related output on or off.

- A low or open circuit applied to ENABLEx switches off the related OUTx and RETURNx (high impedance). A sink current at pin OUTx discharges the capacitive load.
- A high applied to ENABLEx switches on the related OUTx and RETURNx to supply the external unit.

## 3.4 OCM1, OCM2

The output current of OUTx is monitored with a transmission factor of 0.1 to the OCMx. With a resistor from OCM to GND, the current is converted to a voltage. The electrical characteristics are specified by $R_{OCM}$ = 750Ω. The CLL-current threshold, the OUT-current limitation and the OUT-current detection can be changed by varying $R_{OCM}$ in a range of 500Ω to 1 kΩ.

Current monitoring enables the device to detect overcurrent conditions at OUTx (short-circuit to GND or RETURNx) and low current conditions at OUTx (short-circuit to $V_{Batt}$ or open load).

The internal pull-down current at OUTx creates no OCMx-current. During ENABLE, the minimum voltage at OCMx is the saturation voltage of an internal NPN-transistor with typically 0.1V. The maximum voltage at OCM is limited by an internal clamping diode to 5.3V.

## 3.5 CLL1, CLL2

The current at pin OUTx is evaluated logically and ready to use for a microcontroller input. With this stage, the logic data transmission from the external unit to the interface is completed.

CLLx is the output stage of a comparator with an internal threshold and with the OCMx input. A OCMx voltage higher than 2.4V creates a logic low at CLLx, and a OCMx voltage lower than 1.43V creates a logic high at CLLx. The comparator has an internal hysteresis of typically 0.4V.

With the pull-down resistor $R_{OCMx}$ = 750Ω at OCMx, the correct OUTx-current threshold related to the logical output CLLx is ensured. The CLLx is low if the OUTx-current is higher than 27.3 mA, and the CLLx is “high”, if the OUTx-current is lower than 19.1 mA. The comparator has an internal hysteresis of typically 5 mA. The tolerance of the ROCM resistor is assumed to be 0%.

The CLL pin is an open-collector output and needs a pull-up resistor of typically 2 kΩ to the 5-V supply. For ESD protection, a 7-V Zener diode is implemented.

## 3.6 RETURN 1, RETURN 2

The RETURNx pin provides a low-ohmic connection to GND via a switched open-collector NPN-transistor. If ENABLEx is high, RETURNx is switched on with a saturation voltage of less than 0.5V at $I_{RETURNx} \leq 50$ mA. If ENABLEx is low or open, RETURNx is a current sink with ≤ 2 mA. RETURNx is current-limited at typically 150 mA.

## 3.7 SC

The smooth capacitor is designed to realize the long-time constant for the slow voltage change at OUTx for both interface channels. The capacity is typically 22 nF. At the rising edge of $V_{Batt}$, the maximum slew rate is $V_{OUTx}$ = 5 V/ms, and at the falling edge of $V_{Batt}$, the maximum slew rate is $V_{OUTx}$ = 10 V/ms.

## 3.8 GND Pins

A GND bond from the chip to pin 1 and pin 8 provides high ground breakage security and the lowest voltage drop and ground shift between the IC and circuit ground. The four GND pins and the die pad are directly connected to the copper leadframe, resulting in a very low thermal resistance, $R_{thJC}$. To also achieve a low ambient thermal resistance ($R_{thJA}$) it is recommended metal parts of the housing be connected in a proper way with the GND pins.

## 3.9 Power Dissipation

Worst case calculation of the supply current $I_S$:

$I_S = 1.278 \times (I_{OUT1} + I_{OUT2}) + 18\ mA$

Worst case calculation of the IC's power dissipation $P_V$:

$P_V = (V_S \times I_S) - [(V_S - V_{diff} - V_{ret\text{-}sat}) \times (I_{OUT1} + I_{OUT2}) + R_{OCM} \times ((I_{OUT1}^2 + I_{OUT2}^2)/81)]$

$V_S$ = Supply voltage (5.7 to 25V)

$V_{diff}$ = $V_S$ to $V_{OUTx}$ voltage difference

$V_{diff}$ = 3.6 V at 12 V $\leq V_S \leq$ 25V

$V_{diff}$ = 0.8 V at 5.7 V $\leq V_S \leq$ 8.5V

$V_{ret\text{-}sat}$ = 0.5 V saturation voltage return

$I_{OUTx}$ = output current at pin OUTx = 0 to 60 mA

$R_{OCM}$ = resistor at pin OCMx

An integrated overtemperature protection generates a switch-off signal at a chip temperature of typically $T_j$ = 160°C and a switch-on signal at typically $T_j$ = 150°C.

If overtemperature is detected, only the corresponding channel will be disabled. The other channel stays enabled.

The RETURNx is switched off if the voltage at RETURNx exceeds 2V (short-circuit comparator threshold) and overtemperature is detected.

The OUTx is switched off if the voltage at OCMx is higher than 4.6V (overcurrent detection level) and overtemperature is detected. The OCM voltage monitors the output current at OUTx via the current ratio of 0.1. The overcurrent-detection level of OUTx can be varied by changing the OCMx resistor. If OUTx is switched off by overtemperature and overcurrent detection, the CLLx output remains a logic low (overcurrent).

As the IC is only overtemperature-protected against short-circuit conditions at RETURNx or OUTx, it has to be checked in each application that the chip temperature does not exceed $T_{jmax}$ = 150°C in normal operation.

## 3.10 Test Hint

The overtemperature signal can be activated by connecting ENABLE1 or ENABLE2 to 9V/10 mA.

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | $V_S$ | –0.6 | 40 | V |
| Voltage at pins CLL1, CLL2, ENABLE1, ENABLE2 | | –0.3 | 6 | V |
| Voltage at SC | $V_{SC}$ | –0.3 | 30 | V |
| Voltage at OCM1, OCM2 | $V_{OCMx}$ | –0.3 | 6.8 | V |
| Voltage at RETURN1, RETURN2 | $V_{RETURNx}$ | –1 | 27 | V |
| Voltage at OUT1, OUT2 | $V_{OUTx}$ | –1 | 40 | V |
| Current at supply (both channels OUTx and RETURNx shorted) | $I_S$ | | 240 | mA |
| Current at logical pins: CLL1, CLL2<br>ENABLE1, ENABLE2 | $I_{CCLx}$<br>$I_{ENABLEx}$ | | 3<br>0.1 | mA<br>mA |
| Current at SC (SC related to GND or $V_{Batt}$) | $I_{SC}$ | –110 | 220 | µA |
| Current at pins to external unit OUT1, OUT2, RETURN1, RETURN2 | | Internally limited | | |
| ESD classification<br>Human body model (100 pF, 1.5 kΩ)<br>Machine model (200 pF, 0.0Ω) | All pins | <br>±2000<br>±200 | | <br>V<br>V |
| Ambient temperature range | $T_{amb}$ | –40 | 95 | °C |
| Junction temperature range | $T_j$ | –40 | 150 | °C |
| Storage temperature range | $T_{stg}$ | –55 | 125 | °C |

## 5. Thermal Resistance[1]

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction case | $R_{thJC}$ | 36 | K/W |

Note: 1. A good ambient thermal resistance junction ($R_{thJA}$ = 65 K/W) can be achieved by using a big pad size for ground connection near a metal component (see section “GND Pins” on page 6)

# 6. Electrical Characteristics

$T_{amb}$ = –40°C to +95°C and $T_j$ = –40°C to +150°C,
Operation supply-voltage range $V_S$ = 5.7V to 18V continuously, $V_S \leq 25V$ for maximum 25 min, $V_S \leq 40V$ for up to 500 ms.
The current values are based on R = 750Ω, 0%-resistor at OCM1/OCM2 pins.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Current<br>$T_j \geq 125°C$ | Outputs disabled, $V_S \leq 18V$ | $I_S$ | | | 8 | mA |
| | Outputs disabled, $V_S \leq 40V$ | $I_S$ | | | 14 | mA |
| | One output enabled, $V_S \leq 18V$ | $I_S$ | | | 13 | mA |
| | Both outputs enabled, $V_S \leq 18V$ | $I_S$ | | | 18 | mA |
| | Output load 2 × 15 mA, $V_S \leq 18V$ | $I_S$ | | | 56 | mA |
| | Output load 2 × 28 mA, $V_S \leq 18V$ | $I_S$ | | | 90 | mA |
| | Output load 2 × 50 mA, $V_S \leq 18V$ | $I_S$ | | | 146 | mA |
| | Output load 2 × 60 mA,<br>$V_S \leq 18V$ ($T_j > 125°C$) | $I_S$ | | | 171 | mA |
| | Both channels OUTx and RETURNx shorted, $V_S \leq 18V$ | $I_S$ | | | 200 | mA |
| **Function SC** | | | | | | |
| Voltage at SC | $V_S$ = 5.7V | $V_{SC}$ | 5.1 | | 5.3 | V |
| Voltage at SC | $V_S$ = 12.5V | $V_{SC}$ | 9 | | 9.4 | V |
| Maximal voltage at SC | $V_S$ = 40V | $V_{SCmax}$ | | | 30 | V |
| SC-discharge current | Voltage SC = $V_{SC}$ – 3V<br>$5.7V \leq V_S \leq 40V$ | $I_{SC\_dis}$ | 33 | | 82 | µA |
| SC-charge current | Voltage SC = $V_{SC}$ – 3V<br>$5.7V \leq V_S \leq 40V$ | $I_{SC\_ch}$ | –58 | | –20 | µA |
| **Function OUT1 and OUT2 (See Figure 3-1 on page 4)** | | | | | | |
| Voltage difference, $V_S$ to $V_{OUTx}$ | $I_{OUTx}$ = 5 to 50 mA<br>$5.7V \leq V_S \leq 8.5V$<br>$12V \leq V_S \leq 25V$ | <br>$V_{diff\_low}$<br>$V_{diff\_high}$ | <br>0.3<br>2.6 | | <br>0.8<br>3.6 | <br>V<br>V |
| Output voltage OUTx | $8.5V \leq V_S \leq 11.3V$ | $V_{OUT\_med}$ | 7.7 | | | V |
| Maximal voltage at OUTx | $V_S$ = 40V | $V_{OUT\_max}$ | 25 | | 30 | V |
| Current mirror ratio, $I_{OCMx}/I_{OUTx}$ | $V_S \leq 40V$, $I_{OUTx}$ = 5 to 15 mA<br>$V_S \leq 25V$, $I_{OUTx}$ = 15 to 50 mA<br>$V_S \leq 40V$, $I_{OUTx}$ = 15 to 50 mA | $I_{OUT\_ratio}$ | 0.09<br>0.10<br>0.097 | | 0.12<br>0.11<br>0.11 | |
| Linearity of mirror ratio $I_{OCMx}/I_{OUTx}$ | | Ratio_lin | –5 | | 5 | % |
| Dynamic resistance OUTx | $V_S \leq 40V$<br>$I_{OUT}$ = 15 to 50 mA | $R_{OUT}$ | 2 | | 12 | Ω |
| Dynamic resistance<br>OUTx + RETURNx | $V_S \leq 40V$<br>$I_{OUT}$ = 15 to 50 mA | $R_{Dyn}$ | 4 | | 15 | Ω |
| OUTx current limitation<br>(OUTx short to GND) | $V_S \leq 18V$<br>$V_S \leq 40V$ | $I_{OUT\_lim}$ | –80<br>–105 | | –60<br>–60 | mA<br>mA |
| Overcurrent detection level | $T_j < 125°C$ | $I_{OUT\_det}$ | –70 | | –51 | mA |
| | $T_j \geq 125°C$<br>Always valid: current limitation is higher than overcurrent detection | $I_{OUT\_det}$ | –60 | | –51 | mA |
| Maximum OUTx current<br>(OUTx short to GND) | $V_S$ = 14V, OCMx shorted to GND | $I_{OUT\_max}$ | –140 | | –85 | mA |

## 6. Electrical Characteristics (Continued)

$T_{amb}$ = –40°C to +95°C and $T_j$ = –40°C to +150°C,
Operation supply-voltage range $V_S$ = 5.7V to 18V continuously, $V_S \leq 25V$ for maximum 25 min, $V_S \leq 40V$ for up to 500 ms.
The current values are based on R = 750Ω, 0%-resistor at OCM1/OCM2 pins.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Leakage current at disabled OUTx | OUTx short to GND, $V_S \leq 25V$<br>OUTx short to GND, $V_S \leq 38.5V$ | $I_{OUT\_leak}$ | –0.02<br>–12 | | | mA<br>mA |
| Leakage voltage at disabled OUTx | OUTx open, $V_S \leq 38.5V$ | $V_{OUT\_leak}$ | | | 4.3 | V |
| Internal pull-down current | $V_S \leq 18V$<br>$V_S \leq 40V$ | $I_{OUT\_sink}$ | 1.8<br>2.5 | | 4<br>4.5 | mA<br>mA |
| Supply rejection ratio | $V_{SC}$ = 7.6V | $V_{rej\_mV}$ | | | 80 | mV |
| Supply rejection ratio | Variation of $V_S$ = 8.4V to 40V in 10 ms | $V_{rej\_dB}$ | 51.9 | | | dB |
| Minimum capacity at OUTx for phase margin | | $C_{OUT\_min}$ | 33 | | | nF |
| Delay time with $C_{out}$ = 47 nF | Switching on ENABLE = 1 to 90% $V_{OUT}$ reached<br>Switching off ENABLE = 0 to 10% $V_{OUT}$ reached | Enable_on<br>Enable_off | 3<br>30 | | 30<br>100 | µs<br>µs |
| **Function OCM1, OCM2** | | | | | | |
| Voltage threshold CLL-comparator | CLLx low-level voltage threshold<br>CLLx high-level voltage threshold<br>Voltage hysteresis | $V_{CLL\_L}$<br>$V_{CLL\_H}$<br>$V_{CLL\_hys}$ | 1.75<br>1.43<br>0.26 | | 2.4<br>1.9<br>0.6 | V<br>V<br>V |
| Minimum voltage at OCMx | $I_{OUT}$ = 0 to 5 mA | $V_{OCM\_min}$ | | | 0.5 | V |
| Current-limitation level | $V_S \leq 40V$, OUTx short to GND | $V_{OCM\_lim}$ | 4.3 | | 5.3 | V |
| Overcurrent-detection level | $V_S \leq 40V$ | $V_{OCM\_det}$ | 4.2 | | 4.9 | V |
| Current limitation minus overcurrent detection | $V_{OCM\_lim} - V_{OCM\_over}$ | $\Delta$_lim_OCM | 0.15 | | 0.5 | V |
| Internal pull-down current | | $I_{OCM\_sink}$ | 0.1 | | 0.45 | mA |
| **Function RETURN1, RETURN2** | | | | | | |
| Enable high saturation voltage | $I_{RETURN}$ = 50 mA | $V_{ret\_sat}$ | | | 0.5 | V |
| Dynamic resistance | dI ≥ 10 mA | $R_{ret}$ | 2 | | 8 | Ω |
| Current limitation<br>RETURNx is always higher than current limitation OUTx | Enable high, $V_{RETURNx}$ = 2V<br>Enable high, $V_{RETURNx} \leq 18V$<br>Enable low, $V_{RETURNx} \leq 18V$ | $I_{ret\_lim}$<br>$I_{ret\_lim}$<br>$I_{ret\_low}$ | 60<br>70<br>0.8 | | 150<br>200<br>2 | mA<br>mA<br>mA |
| Overcurrent-detection level | Threshold comparator, switch-off return<br>Threshold comparator, switch-on return<br>Hysteresis | $V_{ret\_low}$<br>$V_{ret\_high}$<br>$V_{ret\_hys}$ | 1.4<br>1.1<br>0.2 | | 2<br>1.5<br>0.7 | V<br>V<br>V |
| Delay time<br>$C_{RETURN}$ = 47 nF | Switching on $I_{RETURN}$ at 50 mA<br>Switching off $I_{RETURN}$ at 1 mA | $t_{dRet\_on}$<br>$t_{dRet\_off}$ | 3<br>30 | | 30<br>90 | µs<br>µs |
| **Function CLL1, CLL2 (CLLx with 2 kΩ to 5V)** | | | | | | |
| $I_{OUT}$ threshold CLL comparator | $R_{OCM}$ = 750Ω<br>CLL low-level threshold<br>CLL high-level threshold<br>Hysteresis | <br>$I_{CLL\_L}$<br>$I_{CLL\_H}$<br>$I_{CLL\_hys}$ | <br>23.3<br>19.1<br>3.5 | | <br>27.3<br>22.3<br>8.2 | <br>mA<br>mA<br>mA |
| CLL saturation voltage | $I_{CLL} \leq 2.5$ mA | $V_{CLL\_sat}$ | | | 0.4 | V |
| CLL leakage current | $V_{CLL} \leq 6.5V$ | $I_{CLL\_leak}$ | | | 1 | µA |

# 6. Electrical Characteristics (Continued)

$T_{amb}$ = –40°C to +95°C and $T_j$ = –40°C to +150°C,
Operation supply-voltage range $V_S$ = 5.7V to 18V continuously, $V_S \leq 25V$ for maximum 25 min, $V_S \leq 40V$ for up to 500 ms.
The current values are based on R = 750Ω, 0%-resistor at OCM1/OCM2 pins.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Response time to current change | $I_{OUT}$ to CLL rise<br>$I_{OUT}$ to CLL fall<br>Maximum difference between rise and fall time | $t_{Cll\_rise}$<br>$t_{Cll\_fall}$<br>$t_{\Delta\text{-rise-fall}}$ | 0.1<br>0.1 | | 2<br>2<br>1 | µs<br>µs<br>µs |
| CLL output switching speed | Rise<br>Fall | $t_{CLL\_rise}$<br>$t_{CLL\text{-}fall}$ | | | 1<br>1 | µs<br>µs |
| Current transmission rate | | | 60 | | | kHz |
| Current transmission 3 dB bandwidth | | | 500 | | | kHz |
| **Function ENABLE1, ENABLE2** | | | | | | |
| Enable high-level threshold | | $V_{Enable\_on}$ | 2 | | 6.5 | V |
| Enable low-level threshold | | $V_{Enable\_off}$ | –0.3 | | +0.8 | V |
| Enable input pull-down current (to ensure output disabled during power-off and reset of microcontroller) | | $I_{Enable}$ | 10 | | 100 | µA |
| **Power Dissipation** | | | | | | |
| Power dissipation 1<br>$T_j \geq 125°C$ | $V_S$ = 18V,<br>$I_{OUT1}$ = 28 mA,<br>$I_{OUT2}$ at overcurrent detection level<br>or<br>$I_{OUT2}$ = 28 mA,<br>$I_{OUT1}$ at overcurrent detection level | $P_{dis1}$ | | | 1 | W |
| Power dissipation 2<br>$T_j \geq 125°C$ | $V_S$ = 18V,<br>$I_{OUT1} = I_{OUT2}$ = 28 mA | $P_{dis2}$ | | | 0.75 | W |
| **Selective Overtemperature Protection** | | | | | | |
| Logic AND connected with overcurrent detection (RETURNx, OUTx) | Switch off<br>Switch on<br>Hysteresis | Temp_off<br>Temp_on<br>Temp_hys | 155<br>145<br>5 | | 165<br>155<br>20 | °C<br>°C<br>°C |
| Time delay until overtemperature shut-down | $V_S$ = 25V, $T_{amb}$ = 125°C<br>OUT1 = OUT2 = GND | $t_{del}$ | 100 | | | ms |

# 7. Timing Diagrams

**Figure 7-1.** Variation of Power Supply

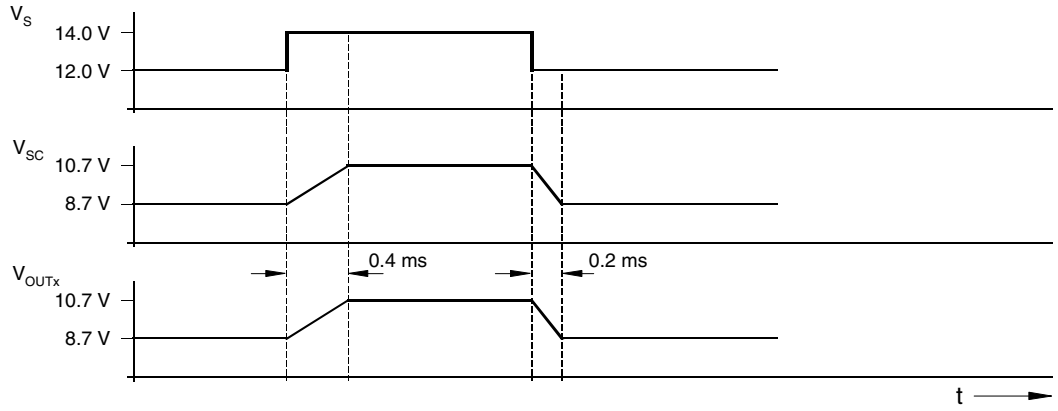



**Figure 7-2.** Overcurrent Protection

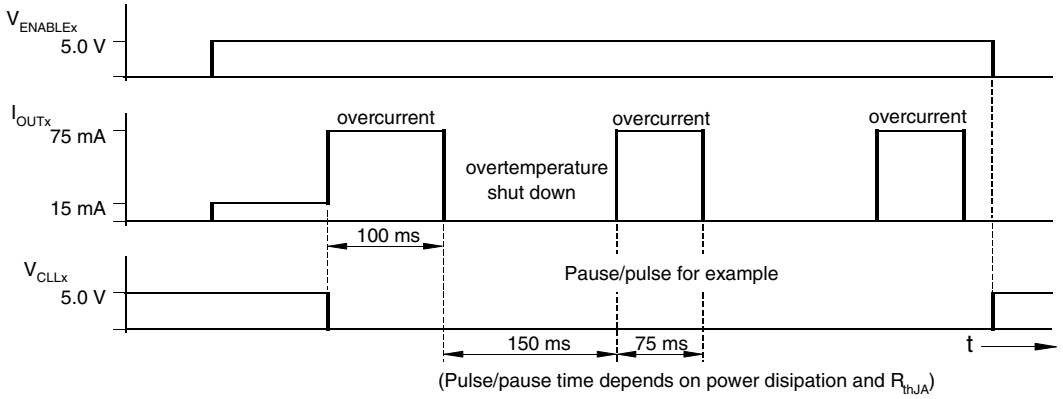


**Figure 7-3.** Data Transmission

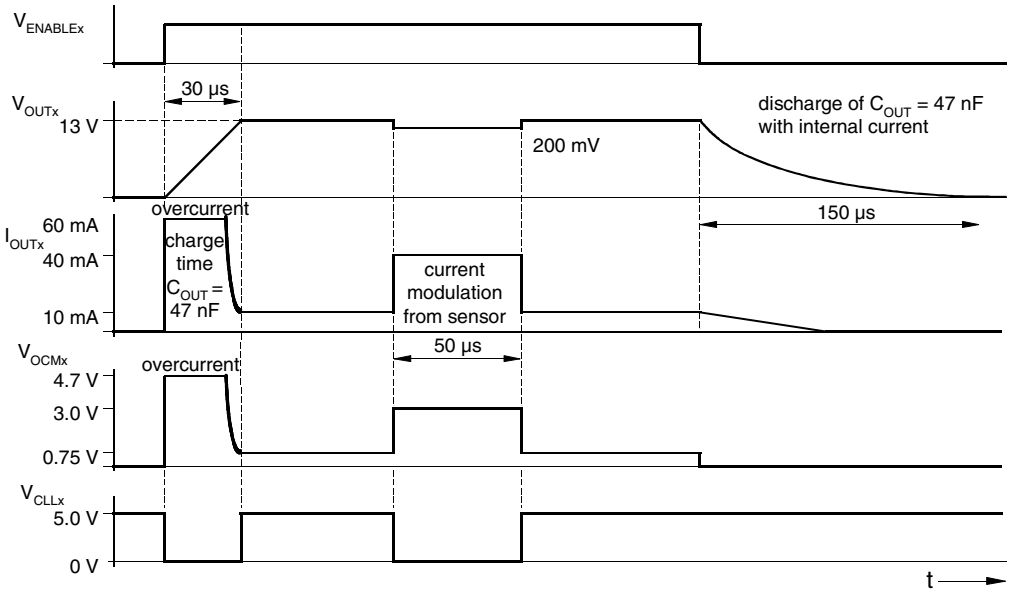
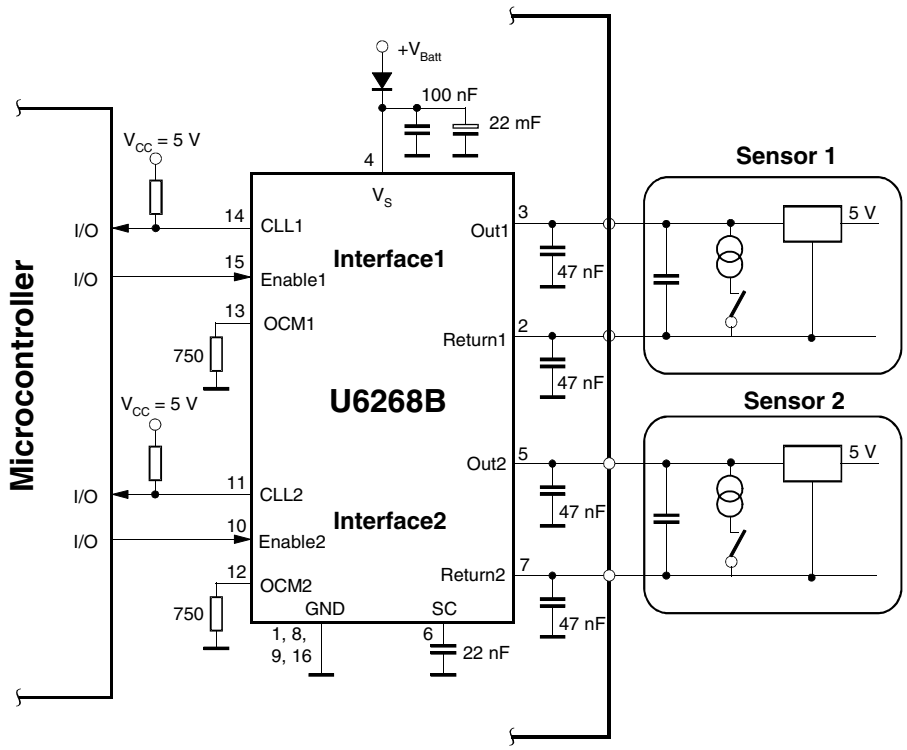



**Figure 7-4.** Application Circuit

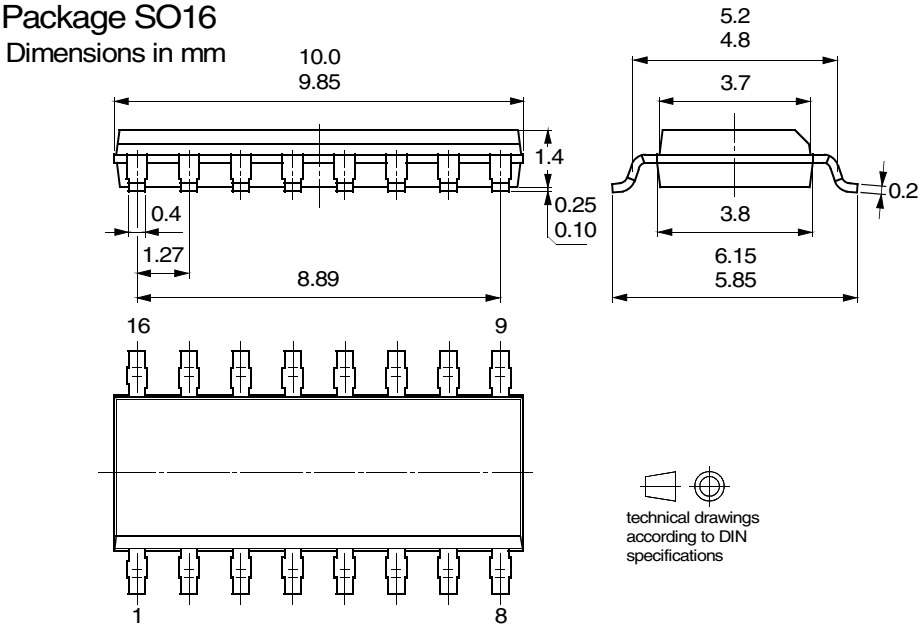


## 8. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U6268B-MFPG3Y | SO16 | Taped and reeled, Pb-free |

## 9. Package Information

Package SO16
Dimensions in mm




## 10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 4808B-AUTO-09/05 | • Put datasheet in a new template<br>• Pb-free logo on page 1 added<br>• Table “Ordering Information” on page 13 changed |

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