

# MOS FIELD EFFECT TRANSISTOR $\mu \mathbf{PA2708TP}$

# SWITCHING N-CHANNEL POWER MOS FET

# DESCRIPTION

The  $\mu$  PA2708TP which has a heat spreader is Nchannel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

# FEATURES

- Low on-state resistance
- R<sub>DS(on)1</sub> = 5.5 mΩ MAX. (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 9.0 A) R<sub>DS(on)2</sub> = 7.5 mΩ MAX. (V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 9.0 A)
- Low Ciss: Ciss = 4700 pF TYP. (VDs = 10 V, VGs = 0 V)
- Small and surface mount package (Power HSOP8)

# ORDERING INFORMATION

PART NUMBER	PACKAGE			
μ PA2708TP-E1	Power HSOP8			
μ ΡΑ2708ΤΡ-Ε1-ΑΖ <sup>Νote</sup>	Power HSOP8			
μ PA2708TP-E2	Power HSOP8			
μ PA2708TP-E2-AZ Note	Power HSOP8			

**Note** Pb-free (This product does not contain Pb in external electrode.)

# ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (VGs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDs = 0 V)	Vgss	±20	V
Drain Current (DC)	D(DC)	±40	А
Drain Current (pulse) Note1	D(pulse)	±68	А
Total Power Dissipation (Tc = 25°C)	<b>P</b> T1	34	W
Total Power Dissipation Note2	P <sub>T2</sub>	4.3	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note3	las	17	А
Single Avalanche Energy Note3	Eas	28.9	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- 2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm, PW =10 sec
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , L = 100  $\mu$ H, V<sub>GS</sub> = 20  $\rightarrow$  0 V

# THERMAL RESISTANCE

Channel to Ambient <sup>Note</sup>	Rth(ch-A)	96.2	°C/W
Channel to Case	Rth(ch-C)	3.68	°C/W

Note Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

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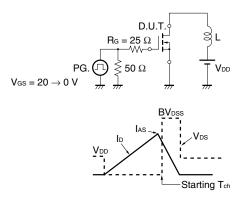
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V			±100	nA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 9.0 A	10			S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.0 A		4.5	5.5	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.0 A		5.6	7.5	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		4700		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		670		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		340		pF
Turn-on Delay Time	<b>t</b> d(on)	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9.0 A		19		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		26		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 10 Ω		100		ns
Fall Time	tr			27		ns
Total Gate Charge	QG	V <sub>DD</sub> = 15 V		38		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		13		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = 17 A		12		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 17 A, VGS = 0 V		0.8		V
Reverse Recovery Time	trr	IF = 17 A, VGS = 0 V		33		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		27		nC
Gate Resistance	Rg	f = 1 MHz		1.2		Ω

# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)

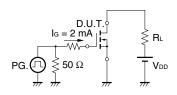
Note Pulsed

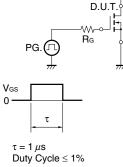
### TEST CIRCUIT 1 AVALANCHE CAPABILITY

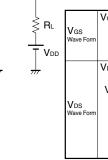
### **TEST CIRCUIT 2 SWITCHING TIME**



# **TEST CIRCUIT 3 GATE CHARGE**



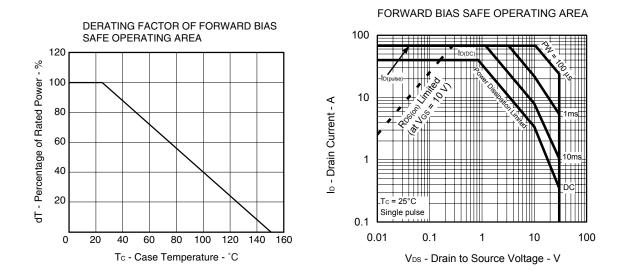




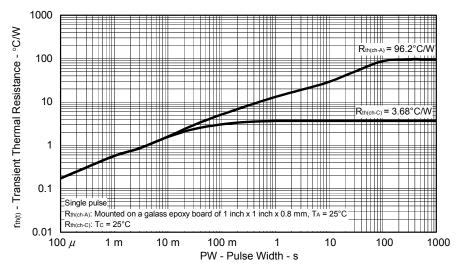
VGS Wave Form	V <sub>GS</sub> 0 <u>10%</u>	[	gs	90%
VDS Wave Form	VDS VDS 0 td(on)	10%	10% j	90%

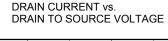
# TYPICAL CHARACTERISTICS (TA = 25°C)

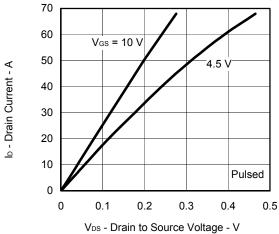
NEC



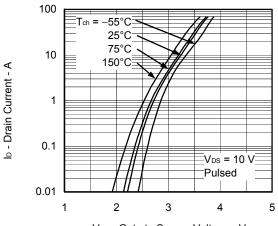
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



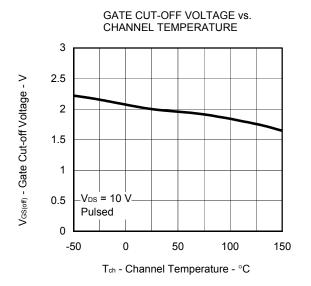


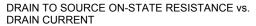


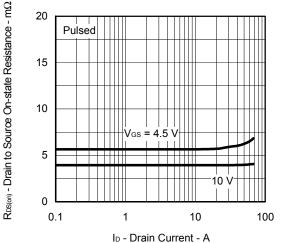
FORWARD TRANSFER CHARACTERISTICS



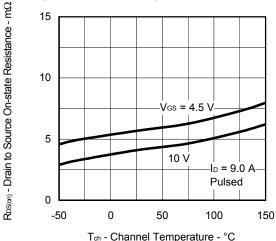
V<sub>GS</sub> - Gate to Source Voltage - V





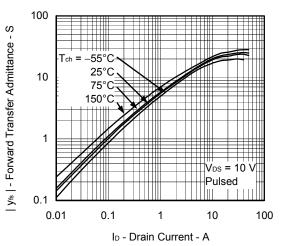




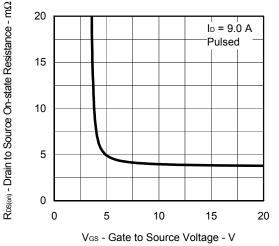


Tch - Channel Temperature - °C

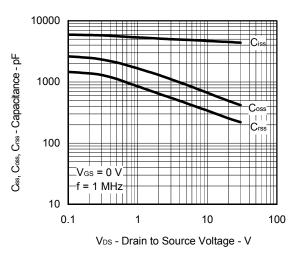
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

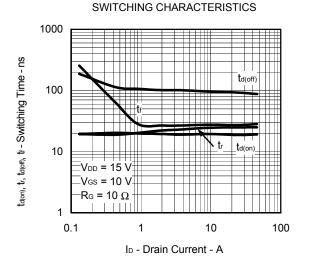


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

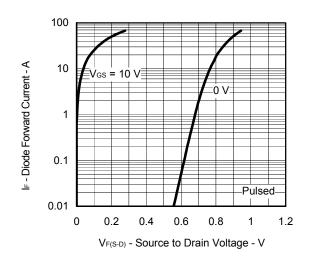


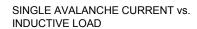
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

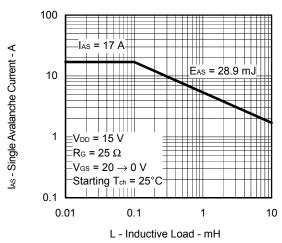


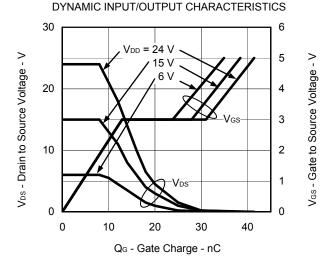


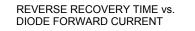
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

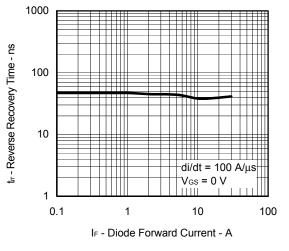


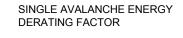


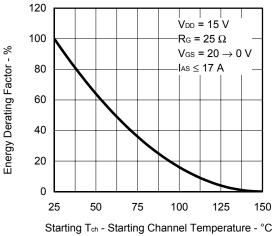






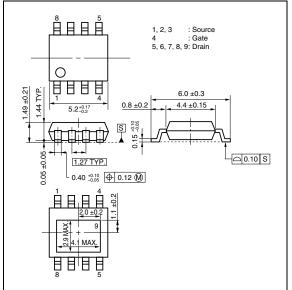




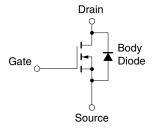


# PACKAGE DRAWING (Unit: mm)

### **Power HSOP8**



# EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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