NEC

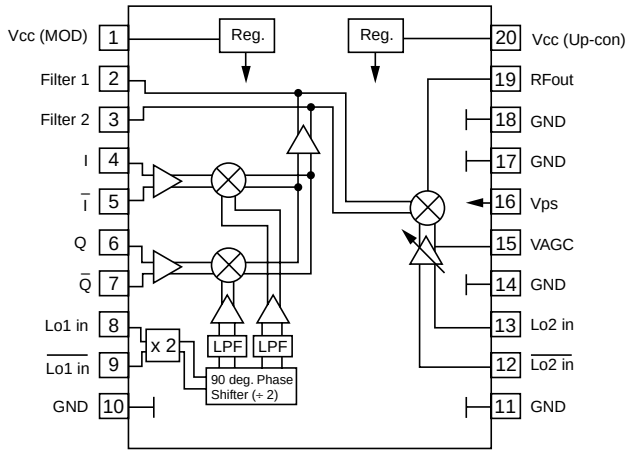
SILICON MMIC UPCONVERTER WITH AGC + IQ MODULATOR

UPC8125GR

FEATURES

- **WIDE SUPPLY VOLTAGE RANGE:** 2.7 to 5.5 V
- **OUTPUT FREQUENCY RANGE:** 1.8 to 2.0 GHz
- **INTERNAL LPF TO REJECT LO & SPURIOUS LEAKAGE**
- **PORTS FOR EXTERNAL IF FILTER**
- **AGC FUNCTION:** 40 dB RANGE
- **POWER SAVE FUNCTION**
- **SMALL 20 PIN SSOP PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

INTERNAL BLOCK DIAGRAM



DESCRIPTION

The UPC8125GR is a Silicon MMIC manufactured with the NESAT™ III silicon bipolar process. The IC consists of a 1.8 - 2.0 GHz upconverter with AGC function and a 220 - 270 MHz IQ modulator. The device operates over a wide 2.7 - 5.5 V supply voltage range and features a power save function. The device was specifically designed for digital mobile communication applications such as 1900 MHz PCS and PHS handsets.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = V_{PS} = 3.0 V, unless otherwise specified)

	PART NUMBER PACKAGE OUTLINE				UPC8125GR S20 (SSOP 20)		
	SYMBOLS	PARAMETERS AND CONDITIONS		UNITS	MIN	TYP	MAX
UP CONVERTER + QUADRATURE MODULATOR TOTAL	I_{CC}	Total Circuit Current (no input signal)		mA	30	36	48
	$I_{CC(PS)}$	Total Circuit Current at Sleep Mode	$V_{PS} \leq$ 0.5 V (Low)	μA		0.3	10
	$P_{RFout\ 1}$	Total Output Power 1	V_{AGC} = 3.0 V	dBm	-13	-9	-5
	$P_{RFout\ 2}$	Total Output Power 2	V_{AGC} = 0.5 V	dBm		-50	
	LoL	Lo Carrier Leak[1]	$f_{LO1} + f_{LO2}$	dBc		-37	-30
	ImR	Image Rejection (Side Band leak)[1]		dBc		-35	-30
	$IM_{3\ I/Q}$	I/Q 3rd Order Intermodulation Distortion[1]		dBc		-50	-30
	GCR	AGC Amp. Gain control range	V_{AGC} = 2.5 V to 0 V	dB	28	40	
	$T_{PS(RISE)}$	Power Save Rise Time	$V_{PS\ (OFF)} \rightarrow V_{PS\ (ON)}$	μS		2	5
	$T_{PS\ (FALL)}$	Power Save Fall Time	$V_{PS\ (ON)} \rightarrow V_{PS\ (OFF)}$	μS		5	10
	$Z_{I/Q}$	Input Impedance I and Q Ports	$f_{I/Q}$ = 24 kHz, $I \rightarrow \overline{I}$, $Q \rightarrow \overline{Q}$	kΩ		200	
	$I_{I/Q}$	I/Q Bias Current	$I \rightarrow \overline{I}$, $Q \rightarrow \overline{Q}$	μA		5	
	Z_{LO1}	Lo1 Input VSWR	f_{LO1}= 220 MHz to 270 MHz			1.2:1	
	EVM	Error Vector Magnitude	MOD Pattern : PN9	%rms		2.5	4.5
	Padj	Adjacent Channel Power	Δf = 600 KHz MOD Pattern : PN9	dBc		-68	-60

Notes:
1. $V_{I/Q}$ = 1.5 V (DC) +0.5 Vp-p (AC)

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	6.0
V_{PS}	Power Save Control Voltage	V	6.0
V_{AGC}	AGC Control Voltage	V	6.0
P_D	Power Dissipation[2]	mW	430
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

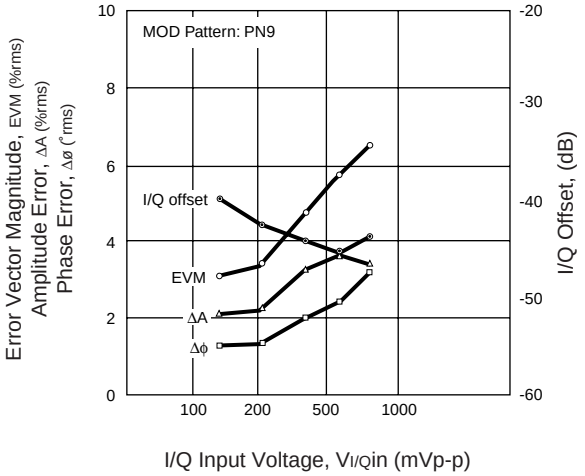
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. T_A = 85°C Mounted on a 50x50x1.6 mm double copper clad epoxy glass board.

RECOMMENDED OPERATING CONDITIONS

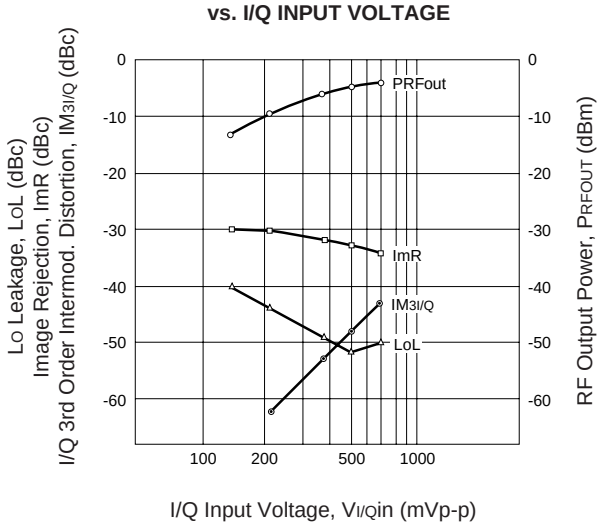
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	5.5
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{RFout}	Up Converter RF Frequency	GHz	1.8		2.0
$f_{UPCONin}$	Up Converter Input Freq.	MHz	220		270
f_{MODout}	Modulator Output Frequency				
f_{LO1in}	Lo1 Input Frequency, P_{LO1in} = -10 dBm				
f_{LO2in}	Lo2 Input Frequency, P_{LO2in} = -10 dBm	MHz	1500		1800
$f_{I/Qin}$	I/Q Input Frequency, $V_{I/Qin}$ = 500 mVp-p MAX (Single ended)	MHz	DC		10
P_{LO1in}	Lo1 Input Level	dBm	-11.5	-10	-5
P_{LO2in}	Lo2 Input Level	dBm	-15	-10	-5
$V_{I/Qin}$	I/Q Input Amplitude, Single ended Input	mVp-p			500
	Differential Input				250

TYPICAL PERFORMANCE CURVES (T_A = 25°C, V_{CC} = V_{PS} = V_{AGC} = 3.0 V, I/Q DC Offset = $\overline{I}/\overline{Q}$ DC Offset = 1.5 V, I/Q Input Signal = 500 mVp-p (Single-ended), LO1 = 250 MHz, P_{LO1} = -10 dBm, LO2 = 1650 MHz, P_{LO2} = -10 dBm, RF_{OUT} = 1900 MHz + $f_{I/Q}$ unless otherwise specified)

ERROR VECTOR MAGNITUDE, AMPLITUDE ERROR, PHASE ERROR AND I/Q OFFSET vs. I/Q INPUT VOLTAGE

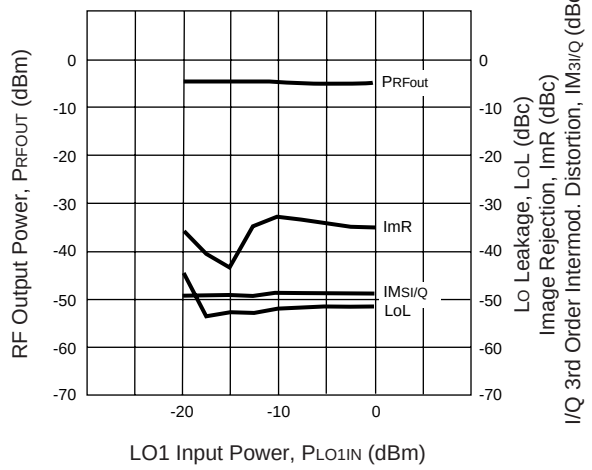


OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. I/Q INPUT VOLTAGE

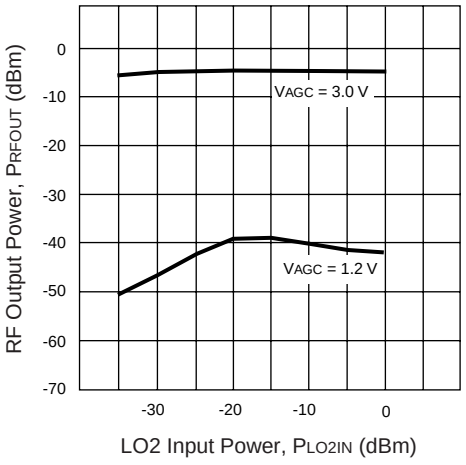


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

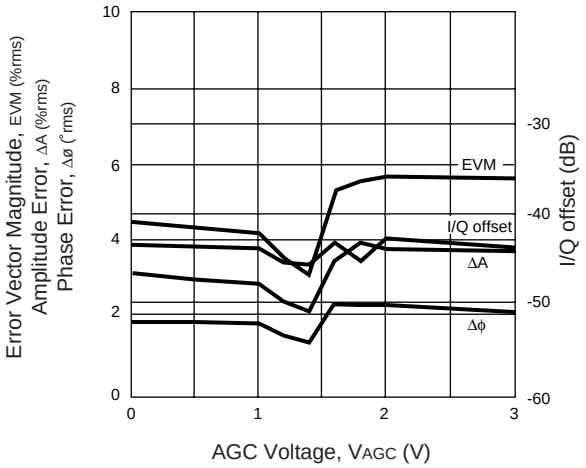
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. LO1 INPUT POWER



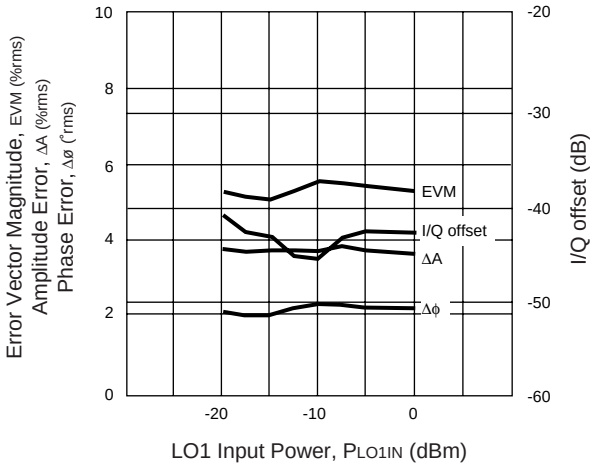
OUTPUT POWER vs. LO2 INPUT POWER AND VAGC



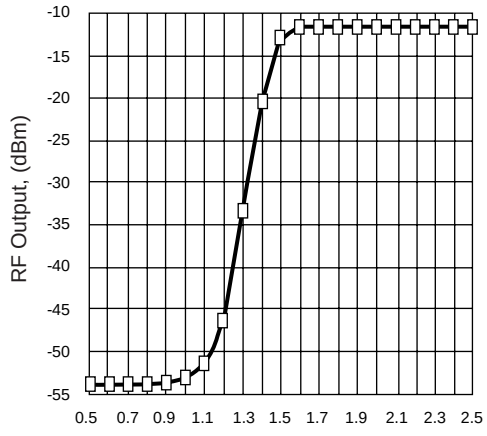
ERROR VECTOR MAGNITUDE, AMPLITUDE ERROR, PHASE ERROR, AND I/Q OFFSET vs. AGC VOLTAGE



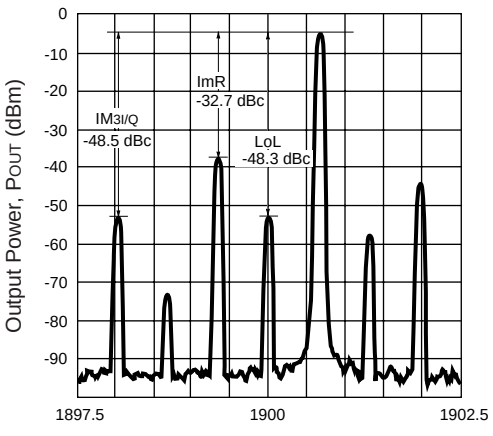
ERROR VECTOR MAGNITUDE, AMPLITUDE ERROR, PHASE ERROR, AND I/Q OFFSET vs. LO1 INPUT POWER



RF OUTPUT vs. AGC VOLTAGE

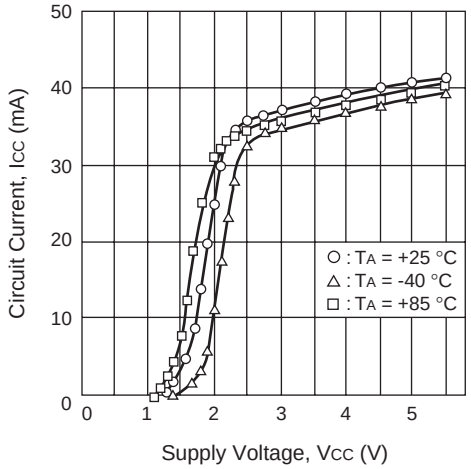


TYPICAL OUTPUT SPECTRUM

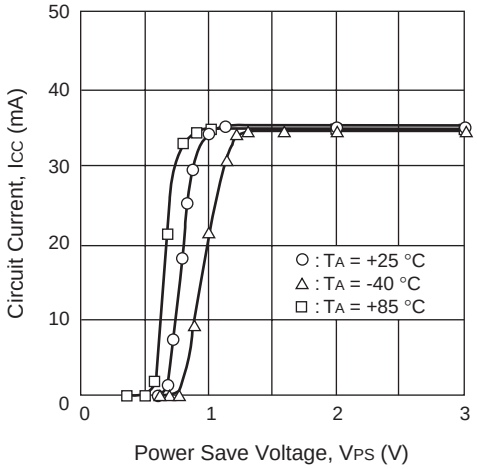


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

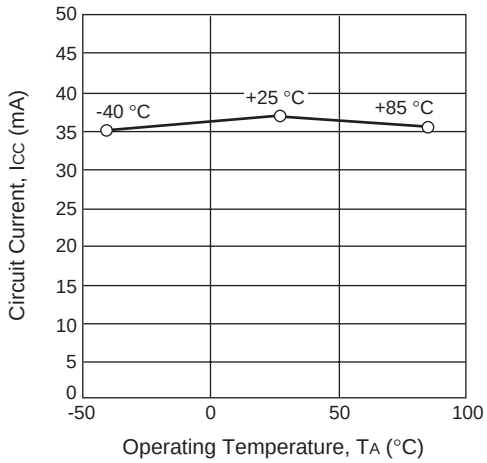
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



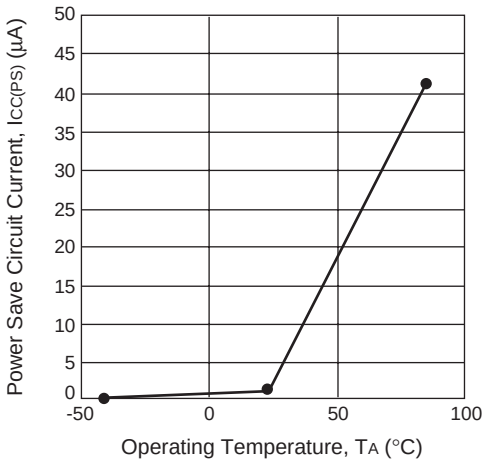
CIRCUIT CURRENT vs. POWER SAVE VOLTAGE



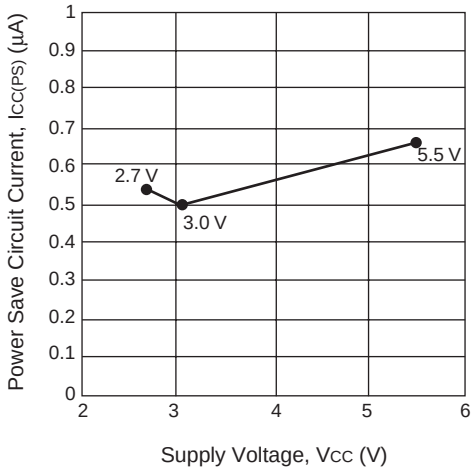
CIRCUIT CURRENT vs. OPERATING TEMPERATURE



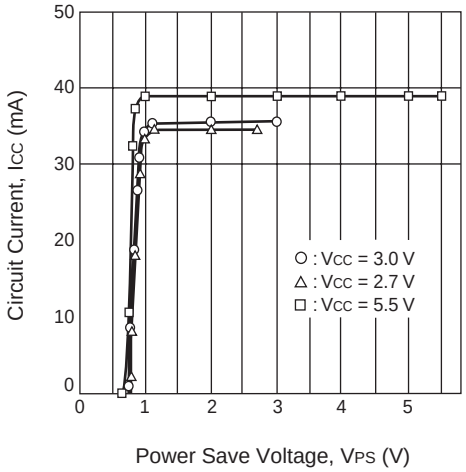
POWER SAVE CIRCUIT CURRENT vs. OPERATING TEMPERATURE



POWER SAVE CIRCUIT CURRENT vs. SUPPLY VOLTAGE

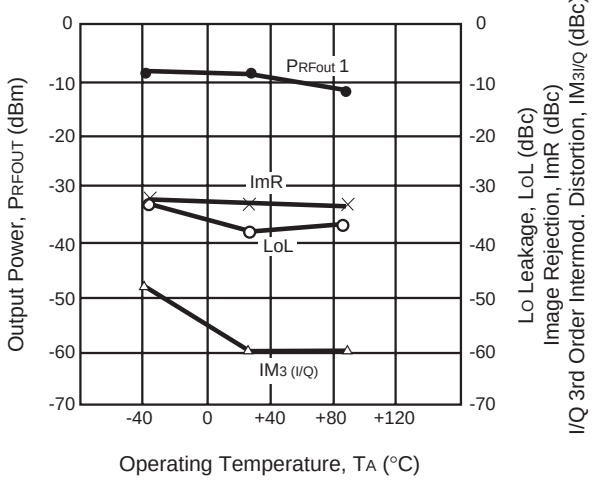


CIRCUIT CURRENT vs. POWER SAVE VOLTAGE

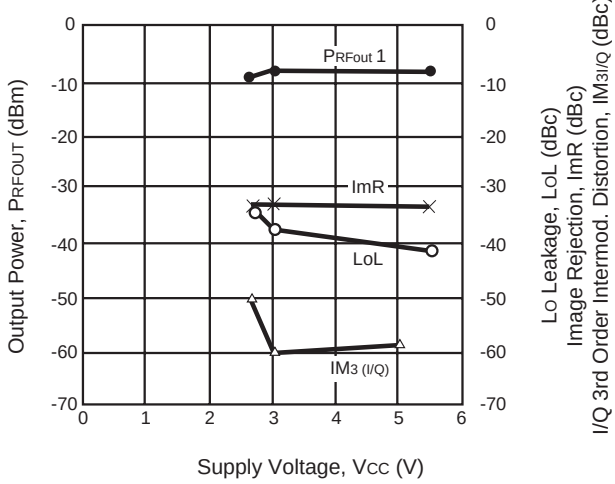


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

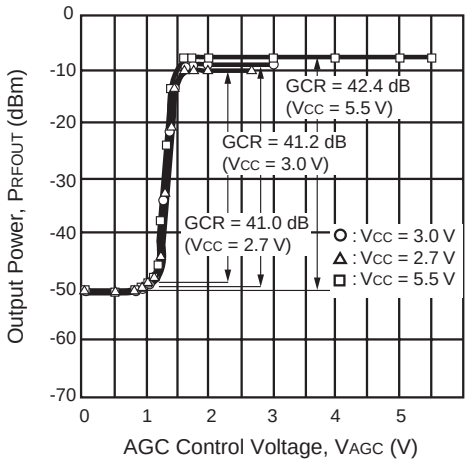
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. OPERATING TEMPERATURE



OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. SUPPLY VOLTAGE



OUTPUT POWER vs. AGC CONTROL VOLTAGE



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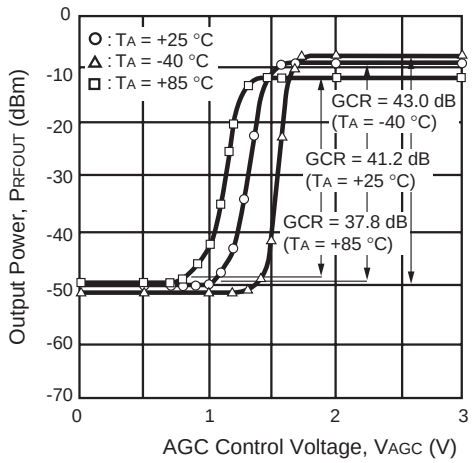
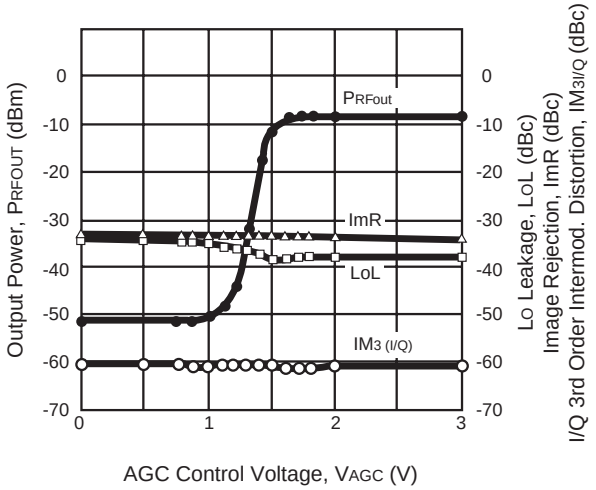
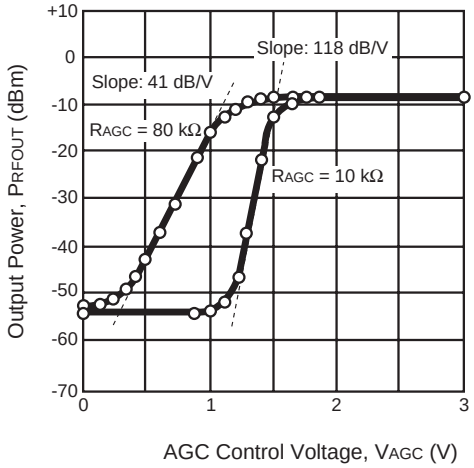


OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. AGC CONTROL VOLTAGE

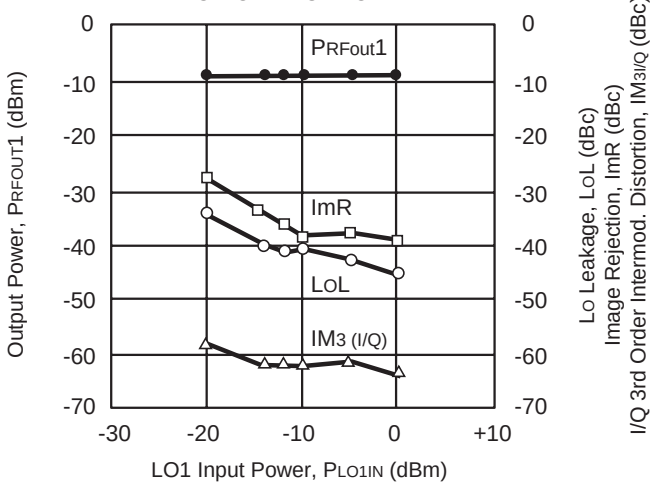


OUTPUT POWER vs. AGC CONTROL VOLTAGE

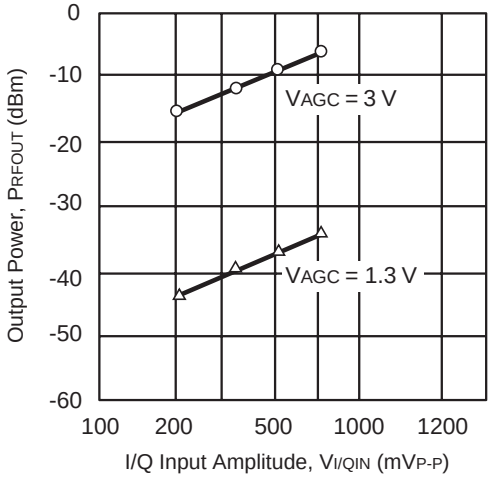


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

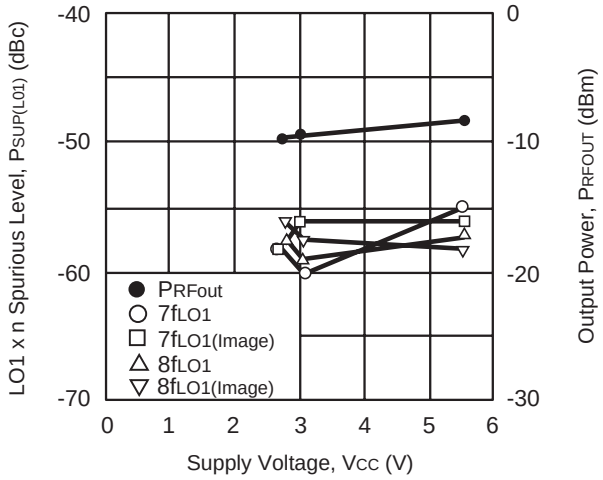
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. LO1 INPUT POWER



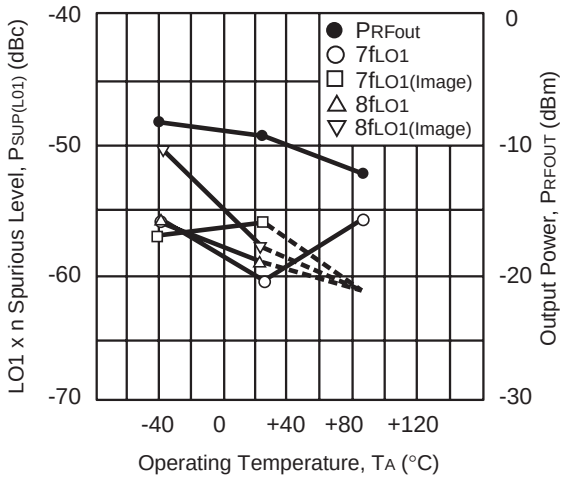
OUTPUT POWER vs. I/Q INPUT AMPLITUDE



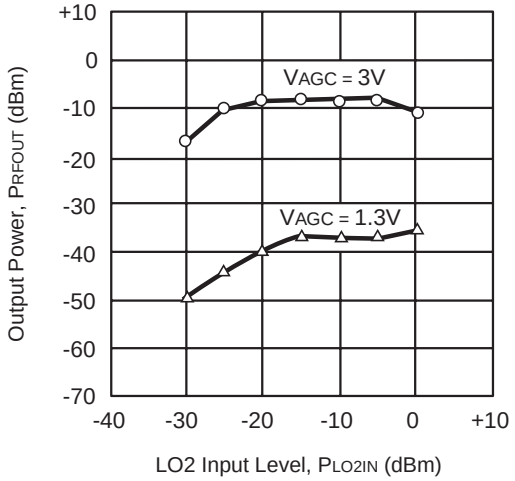
LO1 x n SPURIOUS LEVEL, OUTPUT POWER vs. SUPPLY VOLTAGE



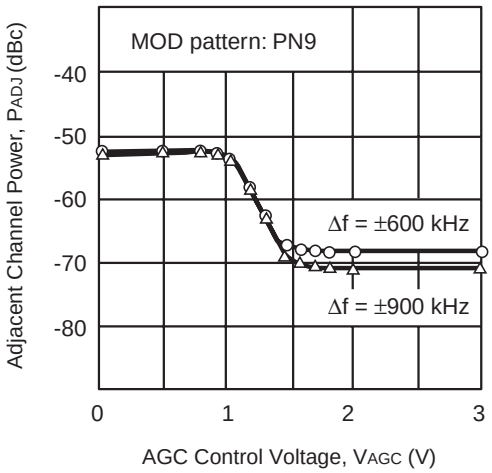
LO1 x n SPURIOUS LEVEL, OUTPUT POWER vs. OPERATING TEMPERATURE



OUTPUT POWER vs. LO2 INPUT LEVEL

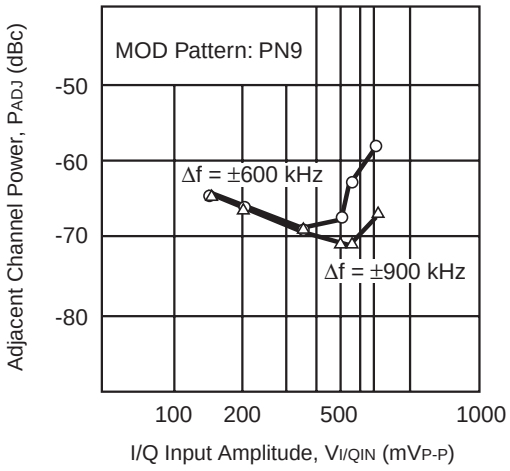


ADJACENT CHANNEL POWER vs. AGC CONTROL VOLTAGE

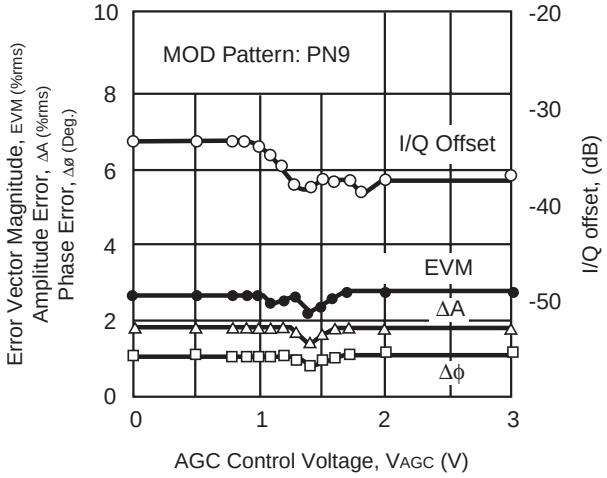


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

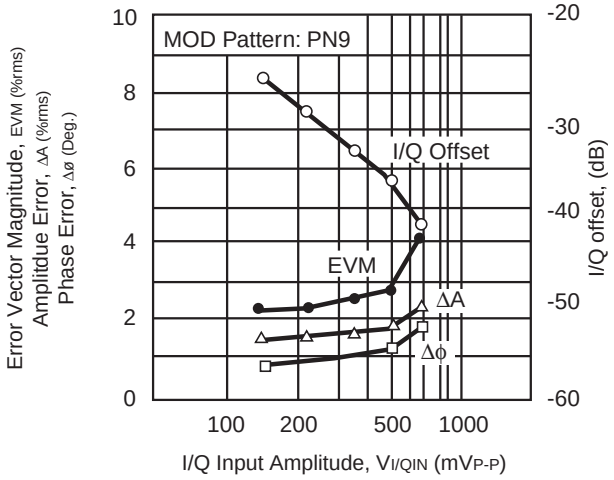
ADJACENT CHANNEL POWER vs. I/Q INPUT AMPLITUDE



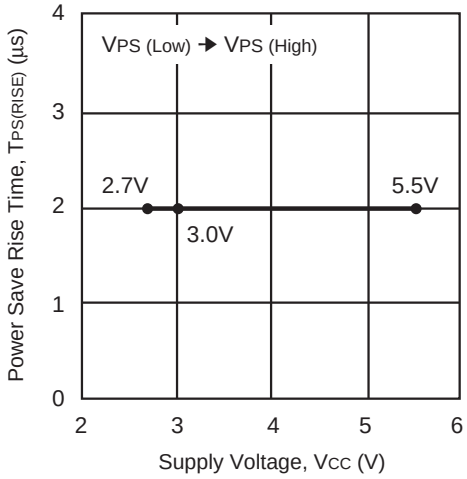
ERROR VECTOR MAGNITUDE, AMPLITUDE ERROR, PHASE ERROR, AND I/Q OFFSET vs. AGC CONTROL VOLTAGE



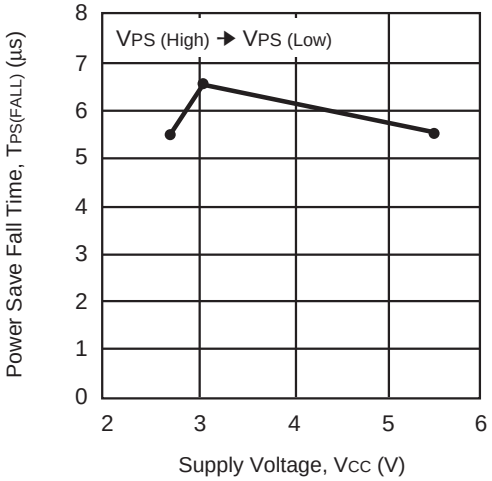
ERROR VECTOR MAGNITUDE, AMPLITUDE ERROR, PHASE ERROR, AND I/Q OFFSET vs. I/Q INPUT AMPLITUDE



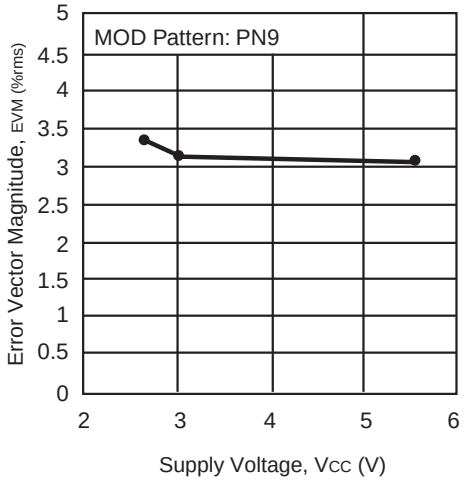
POWER SAVE RISE TIME vs. SUPPLY VOLTAGE



POWER SAVE FALL TIME vs. SUPPLY VOLTAGE

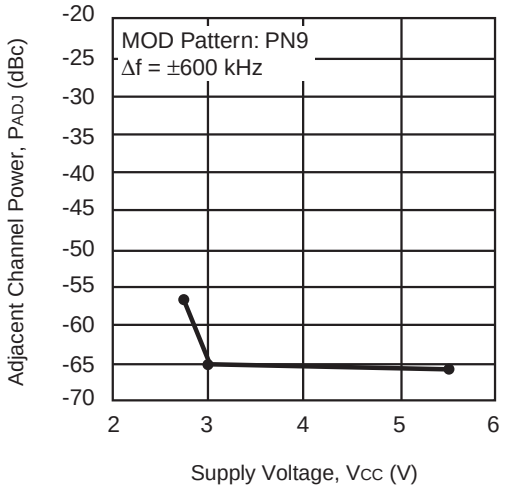


ERROR VECTOR MAGNITUDE vs. SUPPLY VOLTAGE

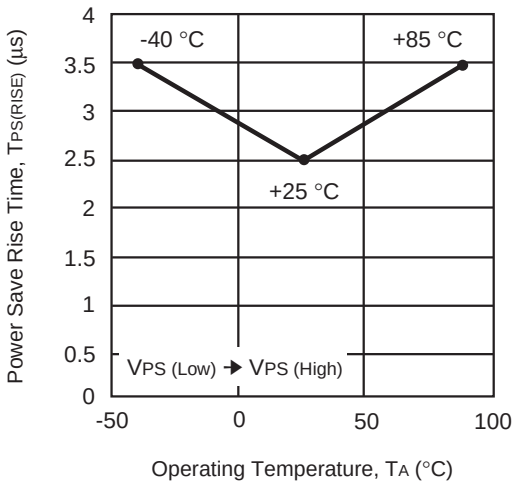


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

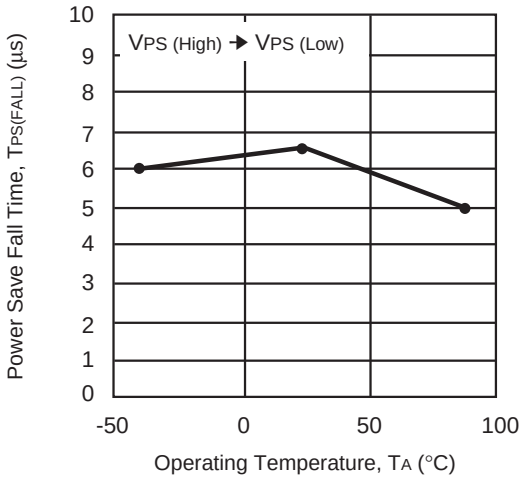
ADJACENT CHANNEL POWER vs. SUPPLY VOLTAGE



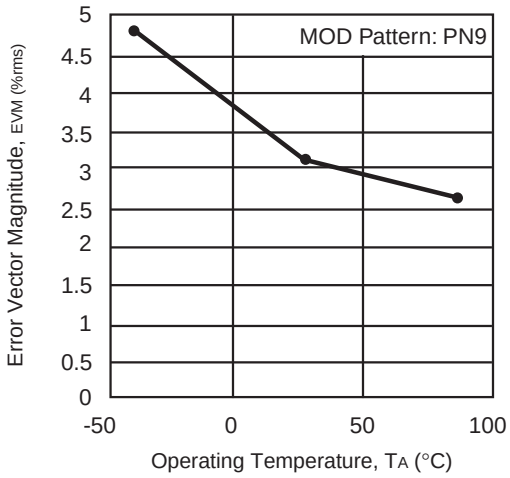
POWER SAVE RISE TIME vs. OPERATING TEMPERATURE



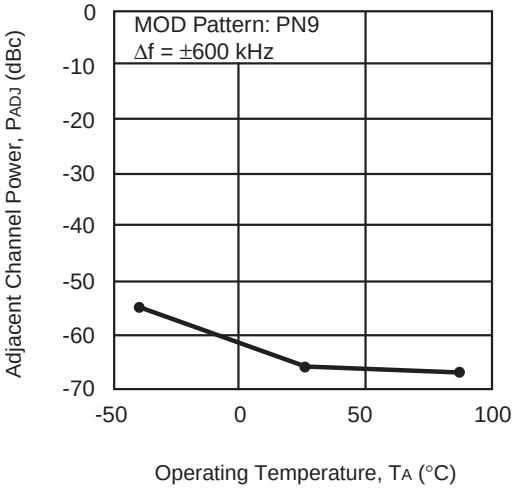
POWER SAVE FALL TIME vs. OPERATING TEMPERATURE



ERROR VECTOR MAGNITUDE vs. OPERATING TEMPERATURE

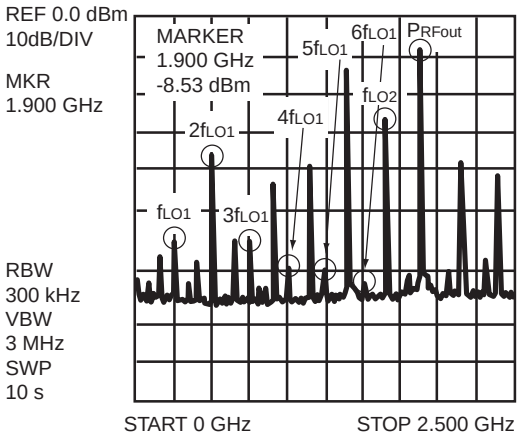


ADJACENT CHANNEL POWER vs. OPERATING TEMPERATURE

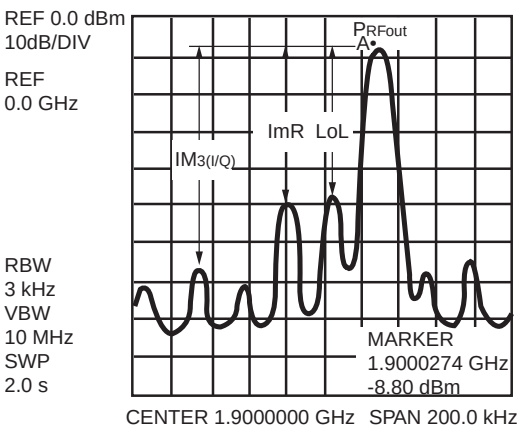


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

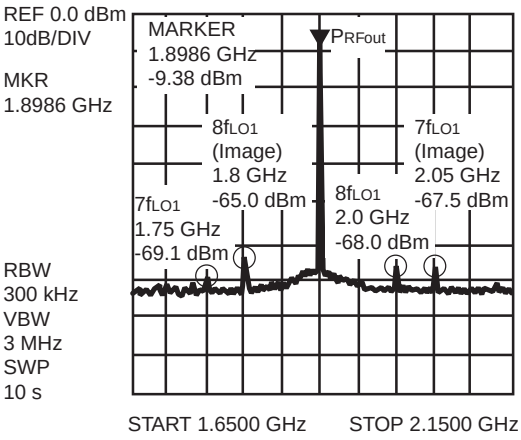
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



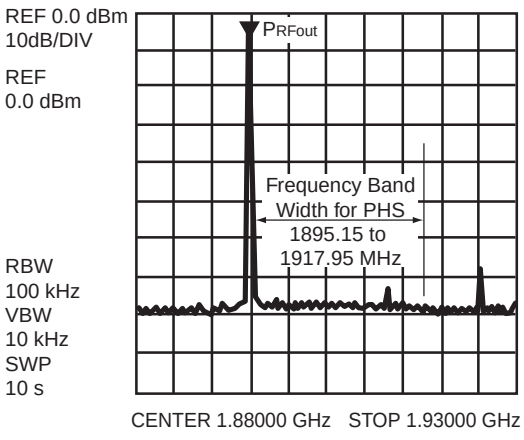
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



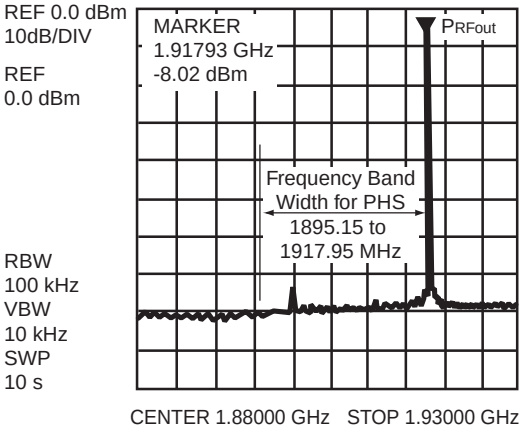
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (1)



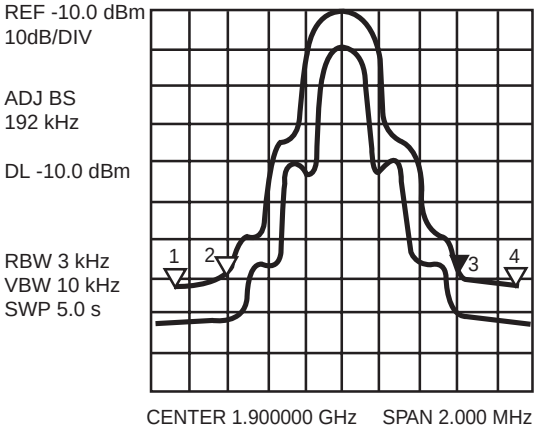
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (2) (f_{LO1} = 233.15 MHz, f_{LO2} = 1662 MHz)



TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (3) (f_{LO1} = 233.15 MHz, f_{LO2} = 1684.8 MHz)



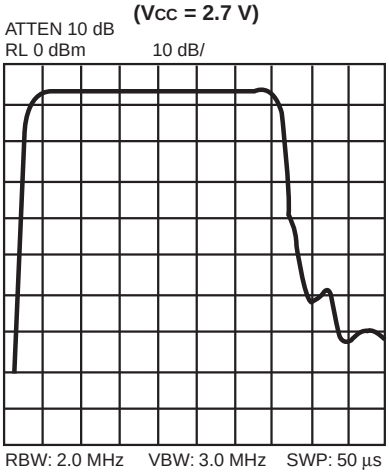
TYPICAL π/4 DQPSK MODULATION OUTPUT SPECTRUM



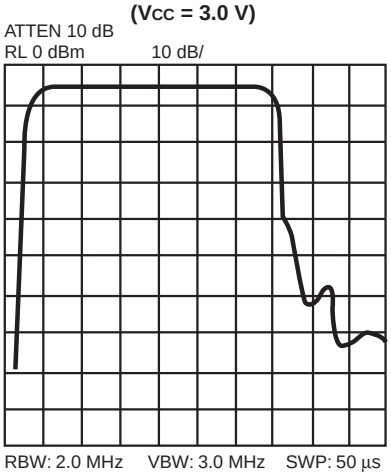
1: 1.899100 GHz -71.00 dB
2: 1.899400 GHz -68.00 dB
3: 1.900600 GHz -68.00 dB
4: 1.900900 GHz -71.25 dB

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

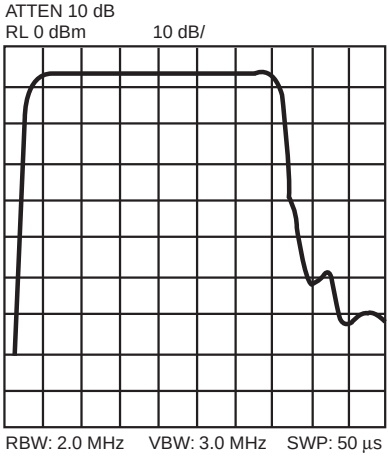
POWER SAVE RESPONSE (1)
(V_{CC} = 2.7 V)



POWER SAVE RESPONSE (2)
(V_{CC} = 3.0 V)



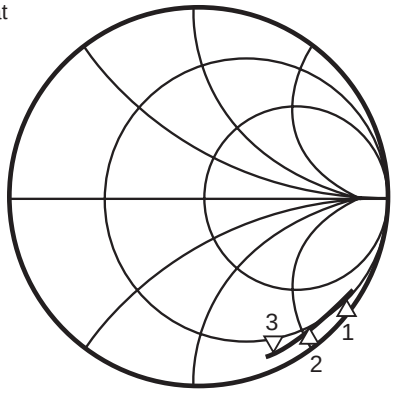
POWER SAVE RESPONSE (3)
(V_{CC} = 5.5 V)



TYPICAL PERFORMANCE CURVES (T_A = 25°C, V_{CC} = V_{PS} = 3.0 V)

RF OUTPUT IMPEDANCE (PIN 19)

Impedance at
Marker 3:
9.145-j84.36

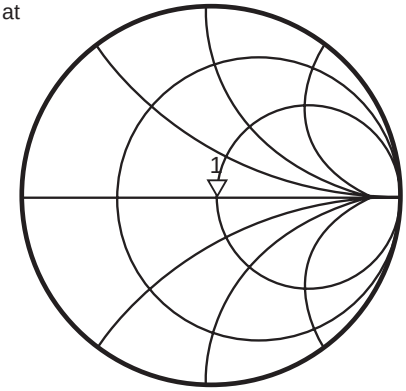


Marker:
1: 900 MHz
2: 1.5 GHz
3: 1.9 GHz

Start: 800 MHz
Stop: 2000 MHz

LO1 INPUT IMPEDANCE (PIN 8)

Impedance at
Marker 1:
50.00+j0.0

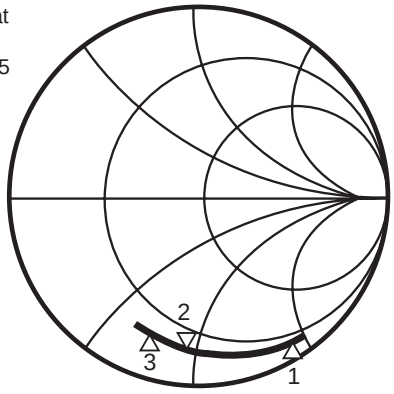


Marker:
1: 250 MHz

Start: 50 MHz
Stop: 500 MHz

LO2 INPUT IMPEDANCE (PIN 13)

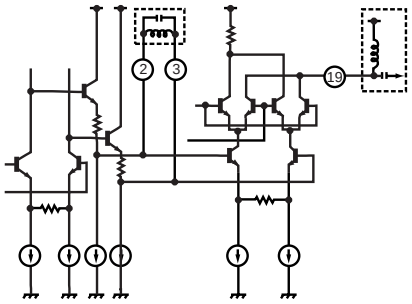
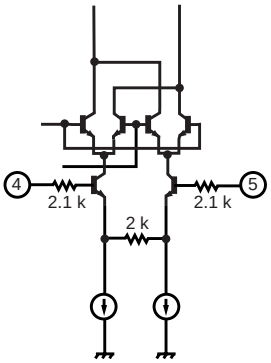
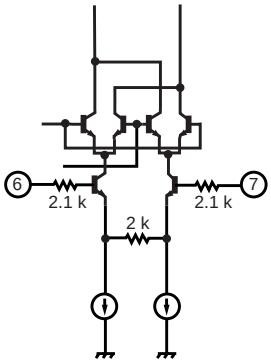
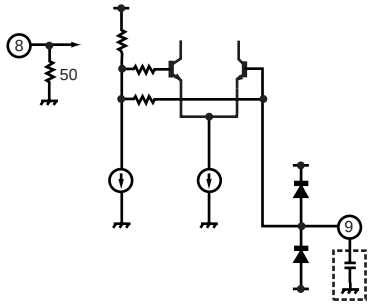
Impedance at
Marker 2:
10.053-j44.05



Marker:
1: 900 MHz
2: 1.65 GHz
3: 1.9 GHz

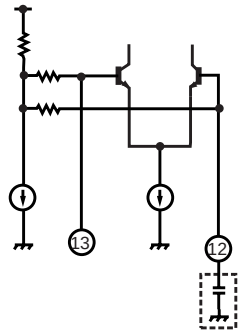
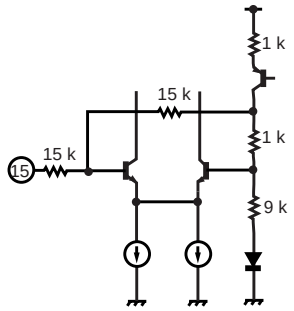
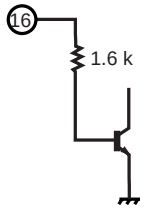
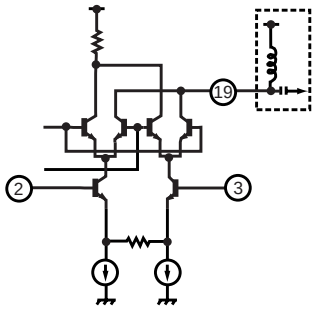
Start: 800 MHz
Stop: 2000 MHz

PIN FUNCTIONS

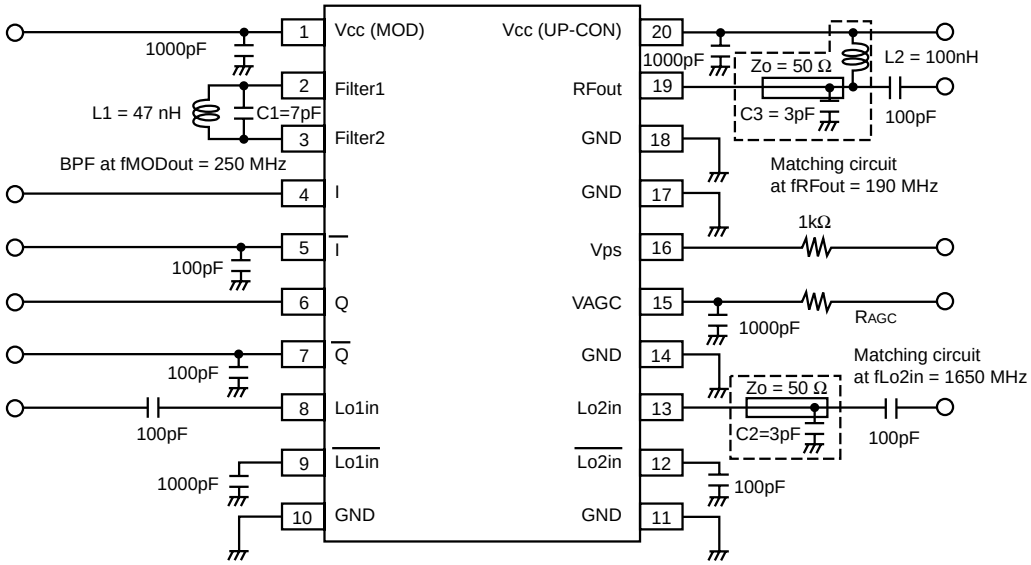
Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) @ 3 V	Description	Equivalent Circuit
1	V_{CC}(MOD.)	2.7 to 5.5	—	Supply Voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or V_{CC} variation. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
2	Filter 1	–	1.9	An external BPF installed between these pins can control the LO1 harmonics.	
3	Filter 2	–	1.9		
4	I	V_{CC}/2 NOTE	–	Input for I signal. This input impedance is 200 kΩ. When used as a single-ended input, the maximum amplitude should be 500 mV_{P-P}. When used as a differential input, the maximum amplitude should be 250 mV_{P-P}.	
5	$\overline{I}$	V_{CC}/2 NOTE	–	Input for I signal. This input impedance is 200 kΩ. When used as a single-ended input, a V_{CC}/2 biased DC signal should be input. When used as a differential input, the maximum amplitude is 250 mV_{P-P}.	
6	Q	V_{CC}/2 NOTE	–	Input for Q signal. This input impedance is 200 kΩ. When used as a single-ended input, the maximum amplitude should be 500 mV_{P-P}. When used as a differential input, the maximum amplitude should be 250 mV_{P-P}.	
7	$\overline{Q}$	V_{CC}/2 NOTE	–	Input for Q signal. This input impedance is 200 kΩ. When used as a single-ended input, a V_{CC}/2 biased DC signal should be input. When used as a differential input, the maximum amplitude is 250 mV_{P-P}.	
8	$LO1_{IN}$	–	0	LO input for the phase shifter. This input impedance is internally matched to 50 Ω.	
9	$\overline{LO_{IN}}$	–	2.4	Bypass of the LO1 input. This pin should be externally grounded through a capacitor.	
10 11	GND (MOD.)	–	0	Ground pins for modulator block. These pins should be connected to system ground with minimum inductance. Track length should be kept as short as possible.	

Note: V_{CC}/2 DC bias must be supplied to I, $\overline{I}$, Q, $\overline{Q}$.

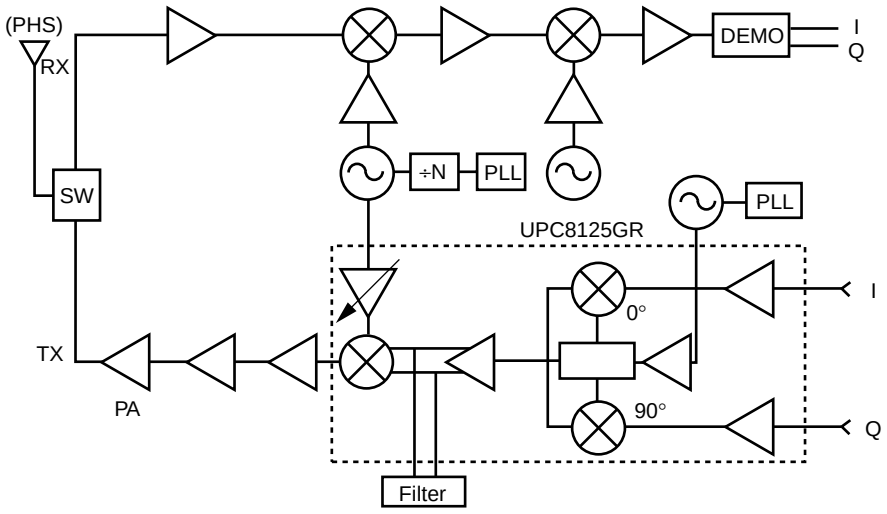
PIN FUNCTIONS

Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) @ 3 V	Description	Equivalent Circuit
12	$\overline{LO_{2IN}}$	–	1.9	Bypass of the LO2 input. This pin should be externally grounded through a capacitor.	
13	LO_{2IN}	–	1.9	LO input for the up-converter. This pin is high impedance input and should be used with an external matching circuit.	
14 17 18	GND (Up-conv.)	–	0	Ground pins for the upconverter block. These pins should be connected to sytem ground with minimum inductance. Track length should be kept as short as possible.	
15	V_{AGC}	0 to V_{CC}	–	Gain Control pin. V_{AGC} Up = Gain Up. Adjust value of R_{AGC} to set gain slope.	
16	V_{PS}	0 to V_{CC}	–	Power save control pin can control the On/ Sleep state with bias as follows: V_{PS} (V) / STATE ≥2.0 / ON 0 to 0.5 / SLEEP	
19	RF_{OUT}	V_{CC}	–	RF output from up-converter. This pin is an open collector and requires an external LC matching circuit.	
20	V_{CC} (Up-con.)	2.7 to 5.5	–	Supply voltage pin for the up-converter. An internal regulator helps keep the device stable against temperature or V_{CC} variation. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	

APPLICATION CIRCUIT

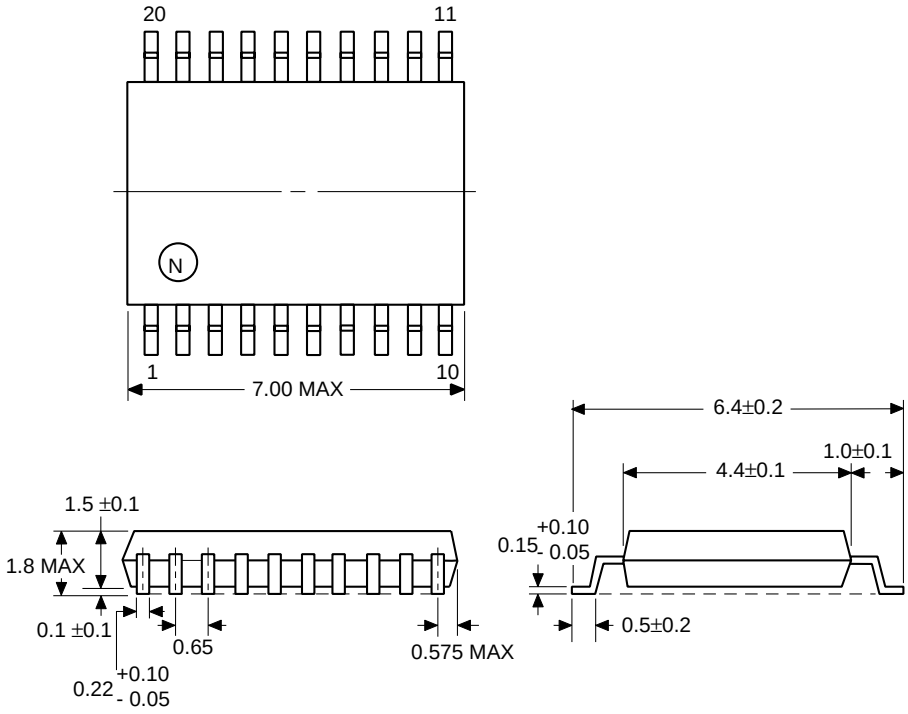


APPLICATION CIRCUIT



PACKAGE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 20



ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC8125GR-E1	2500/Reel

Notes:
1. Embossed tape, 12 mm wide.