NEC

MOS INTEGRATED CIRCUIT

μPD784915A, 784916A

16-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD784915A, 784916A are members of the NEC 78K/IV Series of microcontrollers equipped with a high-speed 16-bit CPU and are the successors of the 78K/I Series 8-bit single-chip microcontrollers for VCR software servo control.

This series contains many peripheral hardware units ideal for VCR control, such as a multi-function timer unit (super timer unit) suitable for software servo control and VCR analog circuits.

A one-time PROM version of the μPD784916A, the μPD78P4916, is also available.

The functions of the μPD784916A are described in detail in the following user's manuals. Be sure to read them before designing.

μPD784915 Subseries User's Manual - Hardware: U10444E
78K/IV Series User's Manual - Instruction: U10905E

FEATURES

- High instruction execution speed realized by 16-bit CPU core
  - Minimum instruction execution time: 250 ns (with 8-MHz internal clock)
- ★ High internal memory capacity

Part Number	ROM	RAM
μPD784915A	48 Kbytes	1280 bytes
μPD784916A	62 Kbytes	

- VCR analog circuits conforming to VHS Standard
  - CTL amplifier
  - RECCTL driver (rewritable)
  - CFG amplifier
  - DFG amplifier
  - DPG comparator
  - DPFG separation circuit (ternary separation circuit)
  - Reel FG comparator (2 channels)
  - CSYNC comparator
- Timer unit (super timer unit) for servo control
- Serial interface: 2 channels (3-wire serial I/O)
- A/D converter: 12 channels (conversion time: 10 μs)
- Low-frequency oscillation mode: main system clock frequency = internal clock frequency
- Low-power dissipation mode: CPU can operate with a subsystem clock.
- Supply voltage range: V_{DD} = 2.7 to 5.5 V
- Hardware watch function: watch operation at low voltage (V_{DD} = 2.7 V (MIN.)) and low current

APPLICATIONS

Control system/servo/timer of VCR

Unless mentioned otherwise, the μPD784916A is described as the representative product.

The information in this document is subject to change without notice

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The mark ★ shows major revised points.

ORDERING INFORMATION

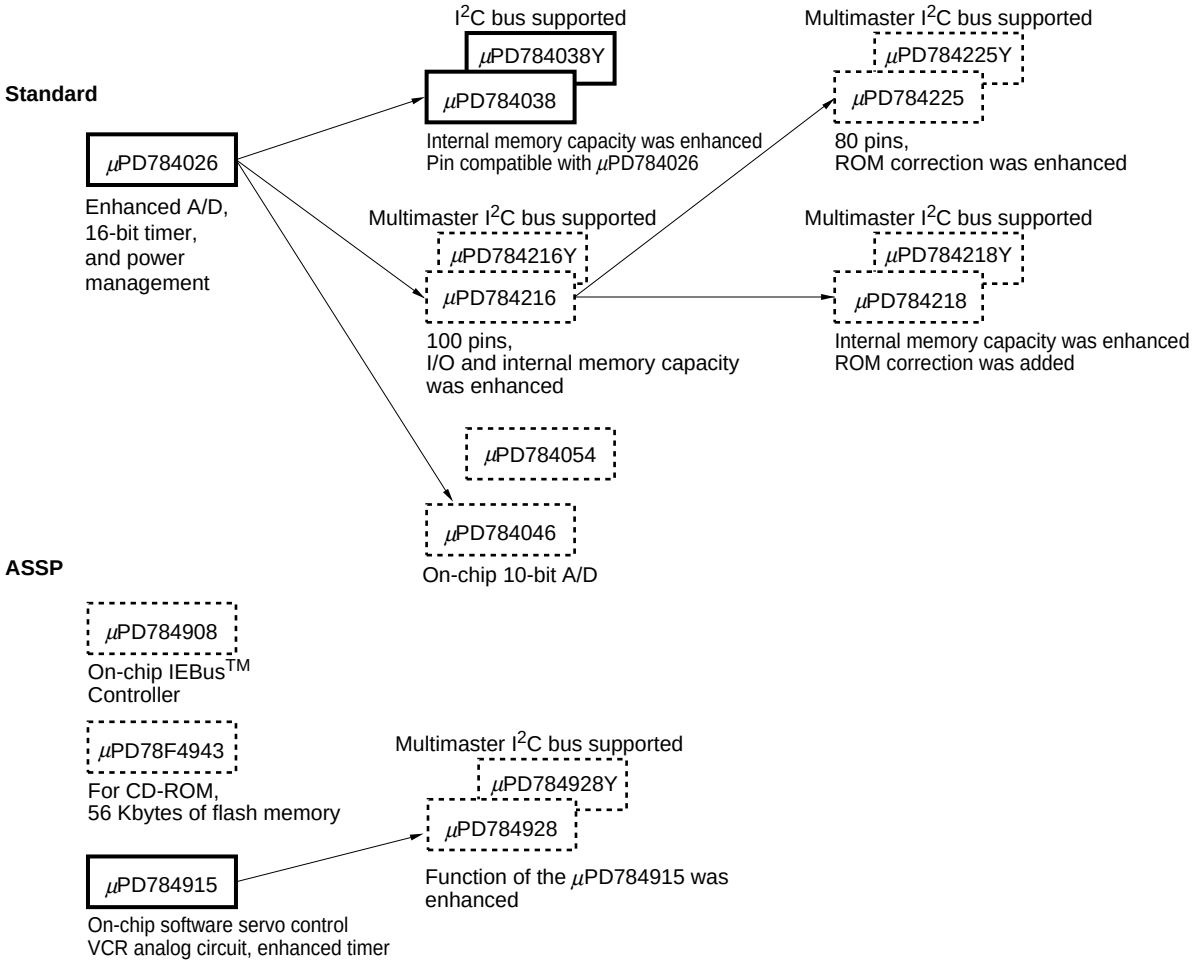
	Part Number	Package
★	μPD784915AGF-xxx-3BA	100-pin plastic QFP (14 x 20 mm)
	μPD784916AGF-xxx-3BA	100-pin plastic QFP (14 x 20 mm)

Remark xxx indicates a ROM code number.

★ Product Development of 78K/IV Series

: Under mass production

: Under development



Function List (1/2)

<table>
<tr><th colspan="2">Item</th><th>μPD784915A</th><th>μPD784916A</th></tr>
<tr><td colspan="2">Internal ROM capacity</td><td>48 Kbytes</td><td>64 Kbytes</td></tr>
<tr><td colspan="2">Internal RAM capacity</td><td colspan="2">1280 bytes</td></tr>
<tr><td colspan="2">Operating clock</td><td colspan="2">16 MHz (internal clock: 8 MHz)
Low frequency oscillation mode: 8 MHz (internal clock: 8 MHz)
Low power dissipation mode: 32.768 kHz (subsystem clock)</td></tr>
<tr><td colspan="2">Minimum instruction execution time</td><td colspan="2">250 ns (with 8-MHz internal system clock)</td></tr>
<tr><td colspan="2">I/O ports</td><td colspan="2">54 { input : 8
I/O : 46</td></tr>
<tr><td colspan="2">Real-time output port</td><td colspan="2">11 (including one each for pseudo VSYNC, head amplifier switch, and chrominance rotation)</td></tr>
<tr><td rowspan="5">Super timer unit</td><td>Timer/counter</td><td colspan="2"><table><tr><th>Timer/counter</th><th>Compare register</th><th>Capture register</th><th>Remark</th></tr><tr><td>TM0 (16 bits)</td><td>3</td><td>–</td><td></td></tr><tr><td>TM1 (16 bits)</td><td>3</td><td>1</td><td></td></tr><tr><td>FRC (22 bits)</td><td>–</td><td>6</td><td></td></tr><tr><td>TM3 (16 bits)</td><td>2</td><td>1</td><td></td></tr><tr><td>UDC (5 bits)</td><td>1</td><td>–</td><td></td></tr><tr><td>EC (8 bits)</td><td>4</td><td>–</td><td>For HSW signal generation</td></tr><tr><td>EDV (8 bits)</td><td>1</td><td>–</td><td>For CFG signal division</td></tr></table></td></tr>
<tr><td>Capture register</td><td colspan="2"><table><tr><th>Input signal</th><th>Number of bits</th><th>Measurable cycle</th><th>Operating edge</th></tr><tr><td>CFG</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr><tr><td>DFG</td><td>22</td><td>125 ns to 524 ms</td><td>↑</td></tr><tr><td>HSW</td><td>16</td><td>1 μs to 65.5 ms</td><td>↑ ↓</td></tr><tr><td>VSYNC</td><td>22</td><td>125 ns to 524 ms</td><td>↑</td></tr><tr><td>CTL</td><td>16</td><td>1 μs to 65.5 ms</td><td>↑ ↓</td></tr><tr><td>TREEL</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr><tr><td>SREEL</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr></table></td></tr>
<tr><td>VCR special circuit</td><td colspan="2">• VSYNC separation circuit, HSYNC separation circuit
• VISS detection, wide aspect detection circuits
• Field identification circuit
• Head amplifier switch/chroma rotation output circuit</td></tr>
<tr><td>General-purpose timer</td><td colspan="2"><table><tr><th>Timer</th><th>Compare register</th><th>Capture register</th></tr><tr><td>TM2 (16 bits)</td><td>1</td><td>–</td></tr><tr><td>TM4 (16 bits)</td><td>1 (capture/compare)</td><td>1</td></tr><tr><td>TM5 (16 bits)</td><td>1</td><td>–</td></tr></table></td></tr>
<tr><td>PWM output</td><td colspan="2">• 16-bit accuracy : 3 channels (carrier frequency: 62.5 kHz)
• 8-bit accuracy : 3 channels (carrier frequency: 62.5 kHz)</td></tr>
<tr><td colspan="2">Serial interface</td><td colspan="2">3-wire serial I/O: 2 channels
• BUSY/STRB control (1 channel only)</td></tr>
<tr><td colspan="2">A/D converter</td><td colspan="2">8-bit resolution x 12 channels, conversion time: 10 μs</td></tr>
</table>

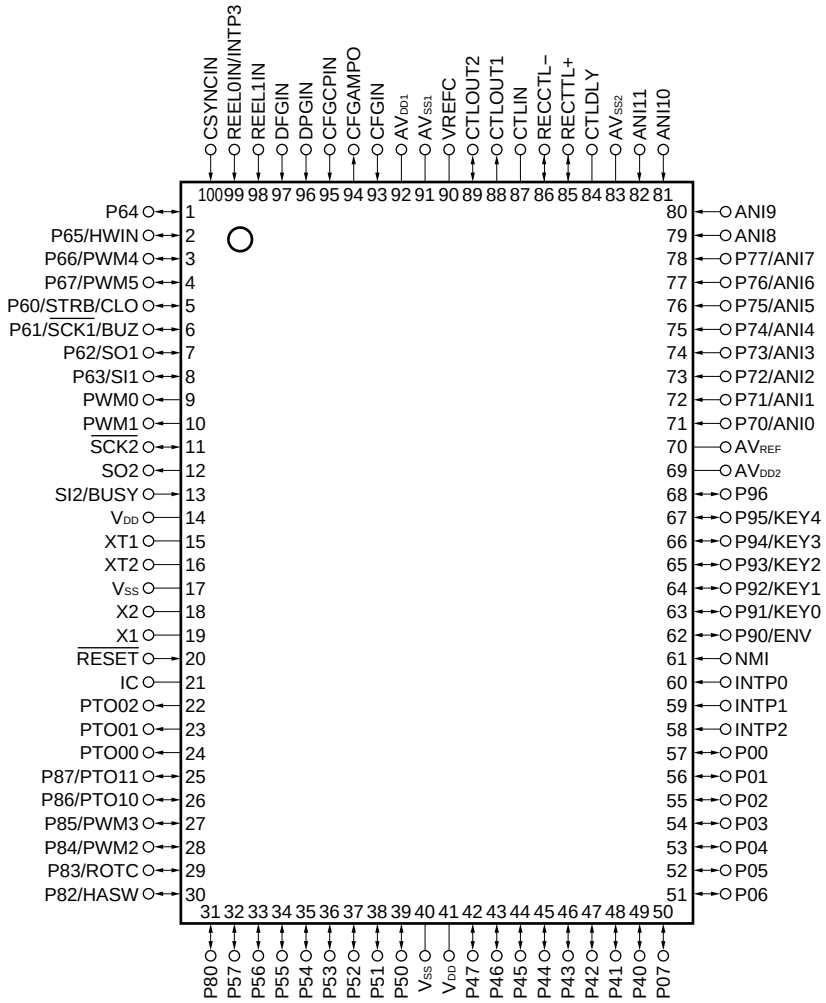
Function List (2/2)

Item	μPD784915A	μPD784916A
Analog circuit	• CTL amplifier • RECCTL driver (rewritable) • DFG amplifier, DPG comparator, CFG amplifier • DPFG separation circuit (ternary separation circuit) • Reel FG comparator (2 channels) • CSYNC comparator	
Interrupt	4 levels (programmable), vector interrupt, macro service, context switching	
External	9 (including NMI)	
Internal	19 (including software interrupt)	
Standby function	HALT/STOP mode/low power dissipation mode/low power dissipation HALT mode	
	STOP mode can be released by input of valid edge of NMI pin, watch interrupt (INTW), or INTP1/INTP2/KEY0-KEY4 pins	
Watch function	0.5-second measurement, low-voltage operation (V_{DD} = 2.7 V)	
Supply voltage	V_{DD} = 2.7 to 5.5 V	
Package	100-pin plastic QFP (14 x 20 mm)	

PIN CONFIGURATION (Top View)

- **100-pin plastic QFP (14 x 20 mm)**

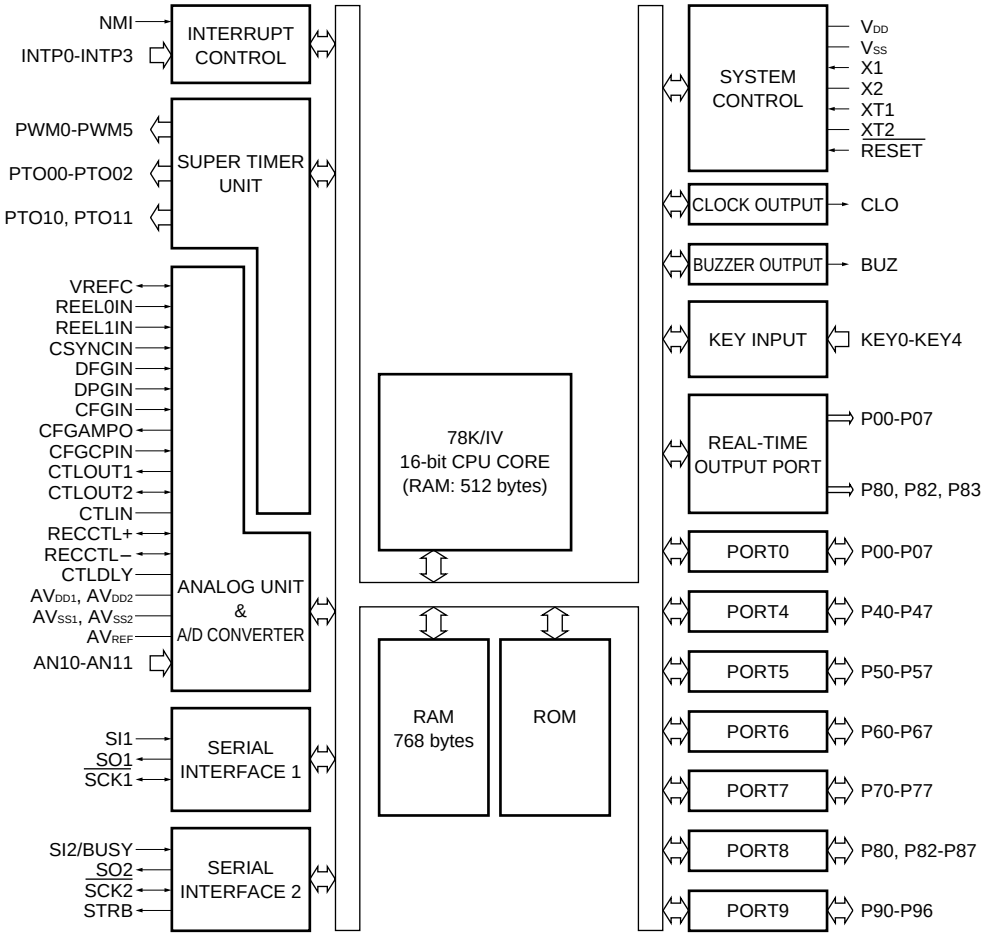
★ **μPD784915AGF-xxx-3BA**
μPD784916AGF-xxx-3BA



Caution Directly connect the IC (Internally Connected) pins to V_{SS}.

ANI0-ANI11	: Analog Input
AV_{DD1}, AV_{DD2}	: Analog Power Supply
AV_{SS1}, AV_{SS2}	: Analog Ground
AV_{REF}	: Analog Reference Voltage
BUSY	: Serial Busy
BUZ	: Buzzer Output
CFGAMPO	: Capstan FG Amplifier Output
CFGCPIN	: Capstan FG Capacitor Input
CFGIN	: Analog Unit Input
CLO	: Clock Output
CSYNCIN	: Analog Unit Input
CTLDLY	: Control Delay Input
CTLIN	: CTL Amplifier Input Capacitor
CTLOUT1, CTLOUT2	: CTL Amplifier Output
DFGIN	: Analog Unit Input
DPGIN	: Analog Unit Input
ENV	: Envelope Input
HASW	: Head Amplifier Switch Output
HWIN	: Hardware Timer External Input
IC	: Internally Connected
INTP0-INTP3	: Interrupt From Peripherals
KEY0-KEY4	: Key Return
NMI	: Nonmaskable Interrupt
P00-P07	: Port0
P40-P47	: Port4
P50-P57	: Port5
P60-P67	: Port6
P70-P77	: Port7
P80, P82-P87	: Port8
P90-P96	: Port9
PTO00-PTO02	: Programmable Timer Output
PTO10, PTO11	
PWM0-PWM5	: Pulse Width Modulation Output
RECCTL+, RECCTL–	: RECCTL Output/PBCLT Input
REEL0IN, REEL1IN	: Analog Unit Input
$\overline{\text{RESET}}$	: Reset
ROTC	: Chrominance Rotate Output
$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$	: Serial Clock
SI1, SI2	: Serial Input
SO1, SO2	: Serial Output
STRB	: Serial Strobe
V_{DD}	: Power Supply
VREFC	: Reference Amplifier Capacitor
V_{SS}	: Ground
X1, X2	: Crystal (Main System Clock)
XT1, XT2	: Crystal (Subsystem Clock)

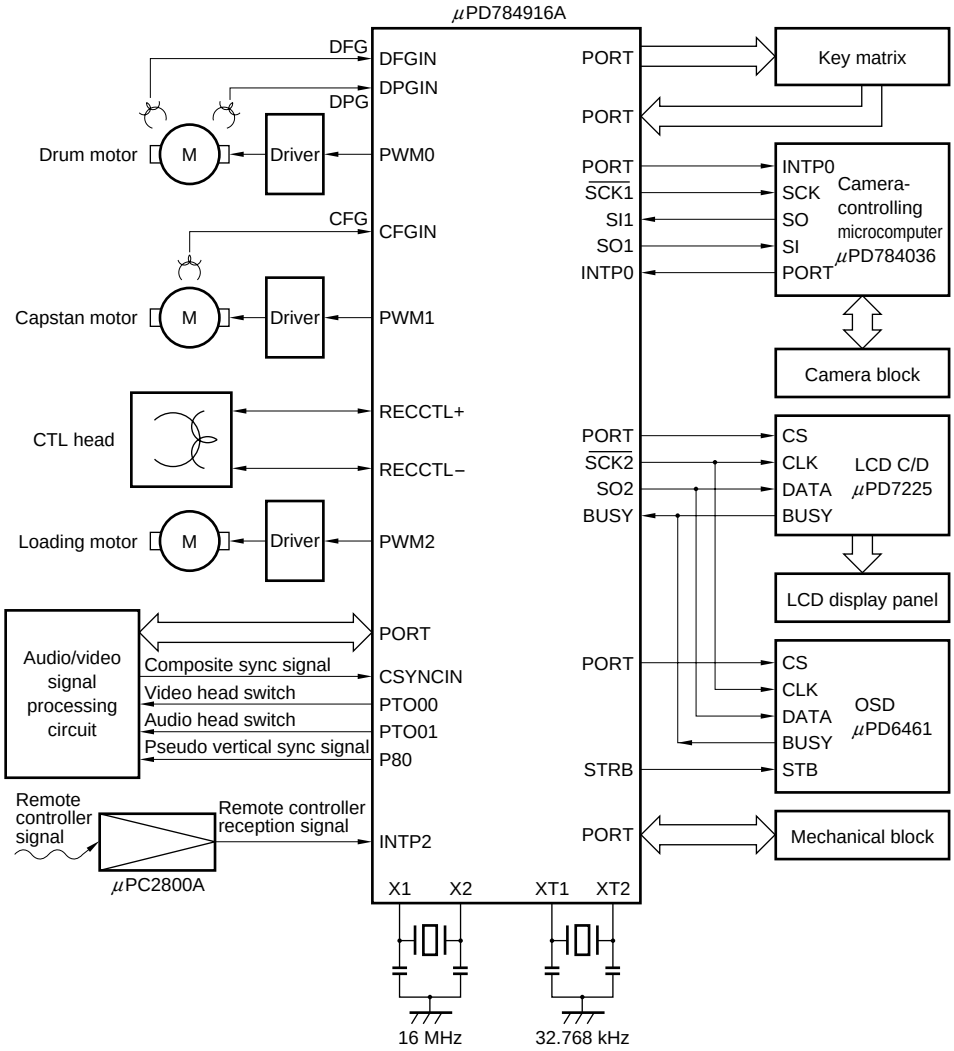
INTERNAL BLOCK DIAGRAM



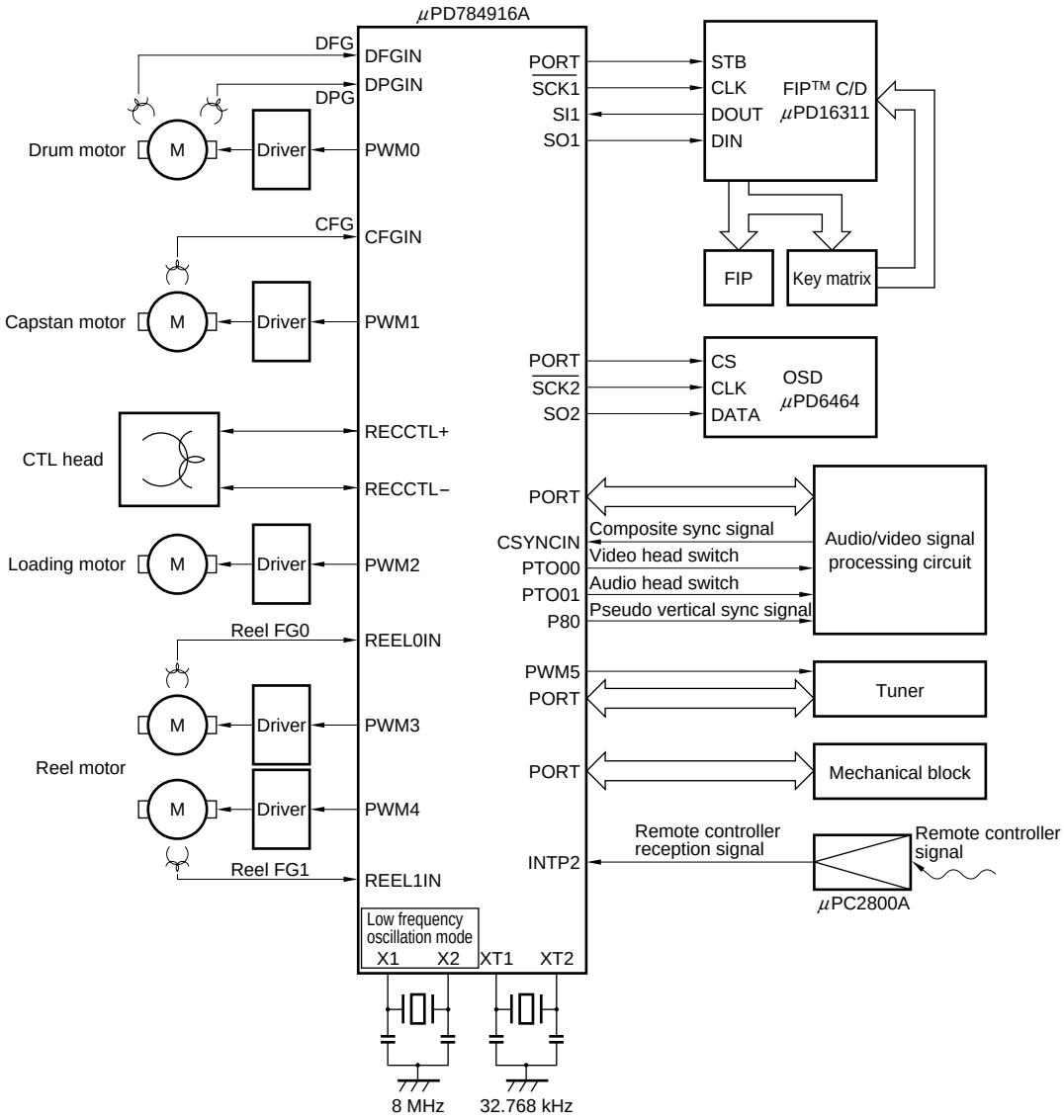
Remark Internal ROM capacity varies depending on the part number.

SYSTEM CONFIGURATION EXAMPLE

- **Camera-contained VCR**



- **Stationary VCR**



CONTENTS

★ 1. DIFFERENCES AMONG μPD784915 SUBSERIES PRODUCTS

The μPD784915 subseries comprises the four products shown in Table 1-1. The μPD784915A, which is a process-shrinked version of the μPD784915 is a low-cost product. The μPD784916A is a version of the μPD784915 with internal ROM extended to 62K bytes. The μPD78P4916 is a product with the mask ROM of the μPD784915, 784915A, and 784916A replaced by a writable one-time PROM. Therefore, it has the same functions as those of the μPD784915, 784915A and 784916A, with only exception that it has PROM for internal ROM and a different capacity.

Before using the PROM to perform debugging or preproduction of an application system and then using the mask ROM to proceed with volume production, etc., thoroughly check the differences between these products.

For more information about the CPU functions and on-chip hardware, see **μPD784915 Subseries User's Manual - Hardware (U10444E)**.

Table 1-1. Differences among μPD784915 Subseries Products

Item	μPD784915, 784915A	μPD784916A	μPD78P4916
Internal ROM	Mask ROM	Mask ROM	One-time PROM
	48K bytes	62K bytes	62K bytes[Note]
Internal RAM	1280 bytes	1280 bytes	2048 bytes[Note]
Internal memory capacity select register (IMS)	Not available	Not available	Available
Pin connections	The μPD78P4916 has additional PROM write/read related pin functions.		
Other	Since these products are different in circuit scale and mask layout, they partly differ in noise resistance, noise radiation and electrical specifications.		

Note The internal PROM and internal RAM capacities can be changed by the internal memory capacity select register (IMS).

Caution The PROM version and mask ROM version differ in noise immunity and noise radiation, etc. When considering replacing a PROM product with a mask ROM product when switching from preproduction to volume production, perform sufficient evaluation using a CS version (not ES version) of the mask ROM product.

2. PIN FUNCTIONS

2.1 Port Pins

Pin Name	I/O	Alternate Function	Function	
P00-P07	I/O	Real-time output port	8-bit I/O port (port 0). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P00-P07).	
P40-P47	I/O	–	8-bit I/O port (port 4). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P40-P47).	
P50-P57	I/O	–	8-bit I/O port (port 5). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P50-P57).	
P60	I/O	STRB/CLO	8-bit I/O port (port 6). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P60-P67).	
P61		$\overline{\text{SCK1}}$/BUZ		
P62		SO1		
P63		SI1		
P64		–		
P65		HWIN		
P66		PWM4		
P67		PWM5		
P70-P77	Input	ANI0-ANI7	8-bit input port (port 7)	
P80	I/O	Real-time output port	Pseudo V_{SYNC} output	7-bit I/O port (port 8). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P80, P82-P87).
P82			HASW output	
P83			ROTC output	
P84		PWM2		
P85		PWM3		
P86		PTO10		
P87		PTO11		
P90	I/O	ENV	7-bit I/O port (port 9). • Can be set in input or output mode in 1-bit units. • Can be connected with software pull-up resistors (P90-P96).	
P91-P95		KEY0-KEY4		
P96		–		

2.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
REEL0IN	Input	INTP3	Reel FG input
REEL1IN		–	
DFGIN		–	Drum FG, PFG input (ternary)
DPGIN		–	Drum PG input
CFGIN		–	Capstan FG input
CSYNCIN		–	Composite SYNC input
CFGCPIN		–	CFG comparator input
CFGAMPO	Output	–	CFG amplifier output
PTO00	Output	–	Programmable timer output of super timer unit
PTO01		–	
PTO02		–	
PTO10		P86	
PTO11		P87	
PWM0	Output	–	PWM output of super timer unit
PWM1		–	
PWM2		P84	
PWM3		P85	
PWM4		P66	
PWM5		P67	
HASW	Output	P82	Head amplifier switch signal output
ROTC	Output	P83	Chroma rotation signal output
ENV	Input	P90	Envelope signal input
SI1	Input	P63	Serial data input (serial interface channel 1)
SO1	Output	P62	Serial data output (serial interface channel 1)
$\overline{\text{SCK1}}$	I/O	P61/BUZ	Serial clock I/O (serial interface channel 1)
SI2	Input	BUSY	Serial data input (serial interface channel 2)
SO2	Output	–	Serial data output (serial interface channel 2)
$\overline{\text{SCK2}}$	I/O	–	Serial clock I/O (serial interface channel 2)
BUSY	Input	SI2	Serial busy signal input (serial interface channel 2)
STRB	Output	P60/CLO	Serial strobe signal output (serial interface channel 2)
ANI0-ANI7	Analog input	P70-P77	Analog signal input of A/D converter
ANI8-ANI11		–	
CTLIN	–	–	CTL amplifier input capacitor connection
CTLOUT1	Output	–	CTL amplifier output
CTLOUT2	I/O	–	Logic signal input/CTL amplifier output
RECCTL+, RECCTL–	I/O	–	RECCTL signal output/PBCTL signal input
CTLDLY	–	–	External time constant connection (for RECCTL rewriting)
VREFC	–	–	VREF amplifier AC connection
NMI	Input	–	Non-maskable interrupt request input
INTP0-INTP2	Input	–	External interrupt request input
INTP3	Input	REEL0IN	
KEY0-KEY4	Input	P91-P95	Key input signal input
CLO	Output	P60/STRB	Clock output
BUZ	Output	P61/$\overline{\text{SCK1}}$	Buzzer output

2.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
HWIN	Input	P65	External input of hardware watch counter
$\overline{\text{RESET}}$	Input	–	Reset input
X1	Input	–	Crystal connection for main system clock oscillation
X2	–		
XT1	Input	–	Crystal connection for subsystem clock oscillation.
XT2	–		Crystal connection for watch clock oscillation
AV_{DD1}, AV_{DD2}	–	–	Positive power supply to analog circuits
AV_{SS1}, AV_{SS2}	–	–	GND of analog circuits
AV_{REF}	–	–	Reference voltage input to A/D converter
V_{DD}	–	–	Positive power supply to digital circuits
V_{SS}	–	–	GND of digital circuits
IC	–	–	Internally connected. Directly connect this pin to V_{SS}.

2.3 I/O Circuits and Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and the recommended connection of unused pins. For the configuration of each type of I/O circuit, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of each Pin and Recommended Connection of Unused Pins (1/2)

Pin	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00-P07	5-A	I/O	Input: Connect to V_{DD} Output: Open
P40-P47			
P50-P57			
P60/STRB/CLO			
P61/$\overline{SCK1}$/BUZ	8-A		
P62/SO1	5-A		
P63/SI1	8-A		
P64	5-A		
P65/HWIN	8-A		
P66/PWM4	5-A		
P67/PWM5			
P70/ANI0-P77/ANI7	9	Input	Connect to V_{SS}
P80	5-A	I/O	Input: Connect to V_{DD} Output: Open
P82/HASW			
P83/ROTC			
P84/PWM2			
P85/PWM3			
P86/PTO10			
P87/PTO11			
P90/ENV			
P91/KEY0-P95/KEY4	8-A		
P96	5-A		
SI2/BUSY	2-A	Input	Connect to V_{DD}
SO2	4	Output	Hi-Z: Connect to V_{SS} via pull-down resistor Others: Open
$\overline{SCK2}$	8-A	I/O	Input: Connect to V_{DD} Output: Open
ANI8-ANI11	7	Input	Connect to V_{SS}
RECCTL+, RECCTL–	–	I/O	When ENCTL = 0 and ENREC = 0: Connect to V_{SS}

Remark ENCTL : bit 1 of amplifier control register (AMPC)
ENREC: bit 7 of amplifier mode register 0 (AMPM0)

Table 2-1. I/O Circuit Type of each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
DFGIN	–	Input	When ENDRUM = 0: Connect to V_{SS}
DPGIN			When ENDRUM = 0 or ENDRUM = 1 and SELPGSEPA = 0: Connect to V_{SS}
CFGIN, CFGCPIN			When ENCAP = 0: Connect to V_{SS}
CSYNCIN			When ENCSYN = 0: Connect to V_{SS}
REEL0IN/INTP3, REEL1IN			When ENREEL = 0: Connect to V_{SS}
CTLOUT1	–	Output	Open
CTLOUT2	–	I/O	When ENCTL = 0 and ENCOMP = 0: Connect to V_{SS} When ENCTL = 1: Open
CFGAMPO	–	Output	Open
CTLIN	–	–	When ENCTL = 0: Open
VREFC			When ENCTL = 0 and ENCAP = 0 and ENCOMP = 0: Open
CTLDLY			Open
PWM0, PWM1	3	Output	Open
PTO00-PTO02			
NMI	2	Input	Connect to V_{DD}
INTP0			Connect to V_{DD} or V_{SS}
INTP1, INTP2	2-A	Input	Connect to V_{DD}
AV_{DD1}, AV_{DD2}	–	–	Connect to V_{DD}
AV_{REF}, AV_{SS1}, AV_{SS2}			Connect to V_{SS}
$\overline{RESET}$	2	–	–
XT1	–	–	Connect to V_{SS}
XT2			Open
IC			Directly connect to V_{SS}

Remark ENDRUM : bit 2 of amplifier control register (AMPC)
SELPGSEPA: bit 2 of amplifier mode register 0 (AMPM0)
ENCAP : bit 3 of amplifier control register (AMPC)
ENCSYN : bit 5 of amplifier control register (AMPC)
ENREEL : bit 6 of amplifier control register (AMPC)
ENCTL : bit 1 of amplifier control register (AMPC)
ENCOMP : bit 4 of amplifier control register (AMPC)

Figure 2-1. I/O Circuits of Pins (1/2)

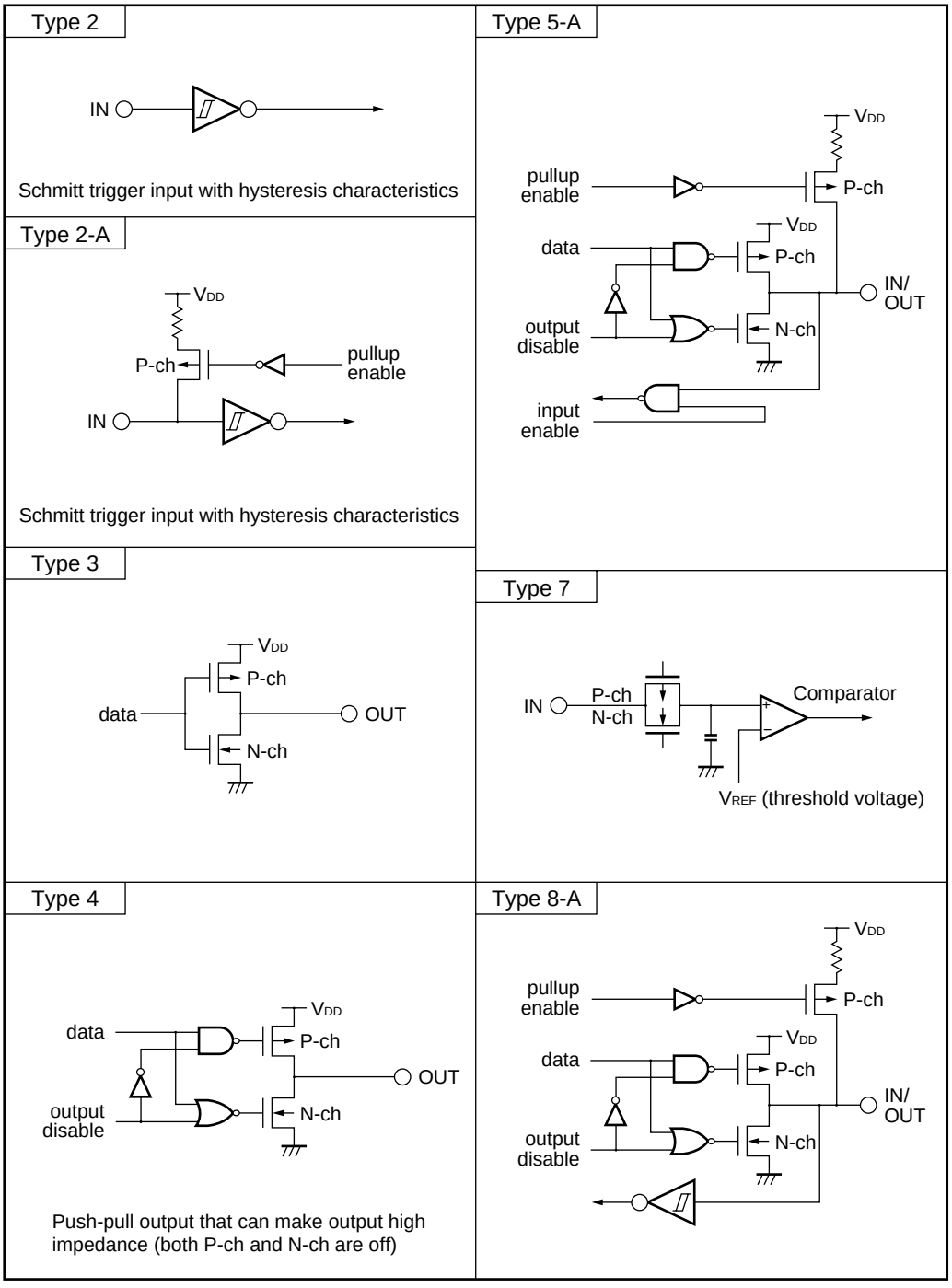
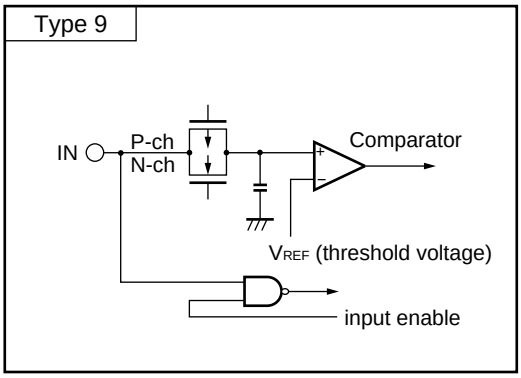


Figure 2-1. I/O Circuits of Pins (2/2)



3. INTERNAL BLOCK FUNCTIONS

3.1 CPU Registers

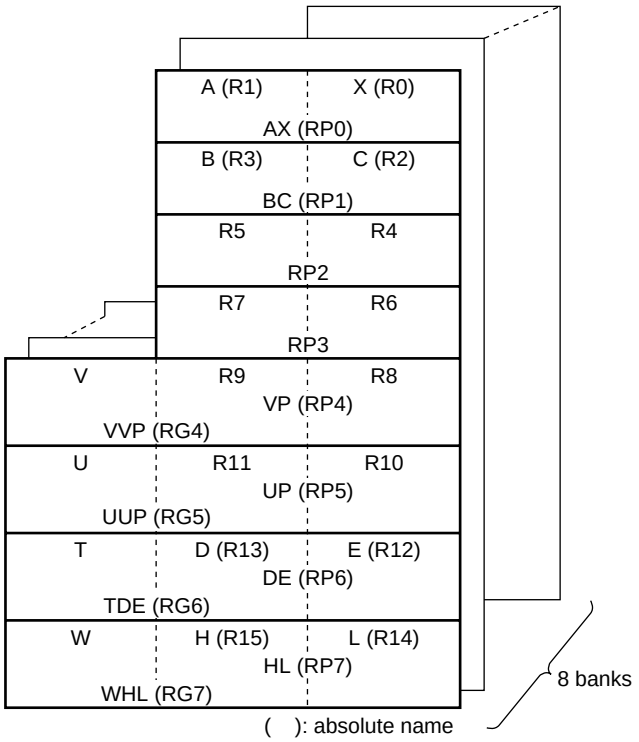
3.1.1 General-purpose registers

The μPD784916A has eight banks of general-purpose registers. One bank consists of sixteen 8-bit general-purpose registers. Two of these 8-bit registers can be used in pairs as a 16-bit register. Four of the 16-bit general-purpose registers can be used to specify a 24-bit address in combination with an 8-bit address expansion register.

These eight banks of general-purpose registers can be selected by software or context switching function.

The general-purpose registers, except for the address expansion registers V, U, T, and W, are mapped to the internal RAM.

Figure 3-1. Configuration of General-Purpose Registers

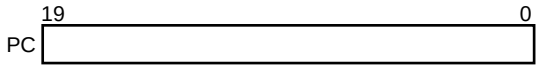


Caution Although R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of PSW to 1, do not use this function. The function of the RSS bit is planned to be deleted from the future models in the 78K/IV Series.

3.1.2 Other CPU registers

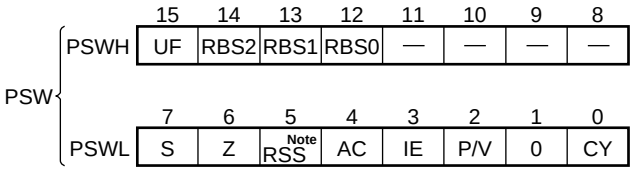
(1) Program counter

The program counter of the μPD784916A is 20 bits wide. The value of the program counter is automatically updated as the program is executed.



(2) Program status word

This is a register that holds the various statuses of the CPU. Its contents are automatically updated as the program is executed.

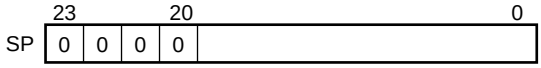


Note The RSS flag is provided to maintain compatibility with the microcomputers in the 78K/III Series. Always clear this flag to 0 except when the software of the 78K/III Series is used.

(3) Stack pointer

This is a 24-bit pointer that holds the first address of the stack.

Be sure to write 0 to the higher 4 bits.



3.2 Memory Space

The μPD784916A can access a 64K-byte memory space.

The addresses of the internal ROM and internal data areas are as follows:

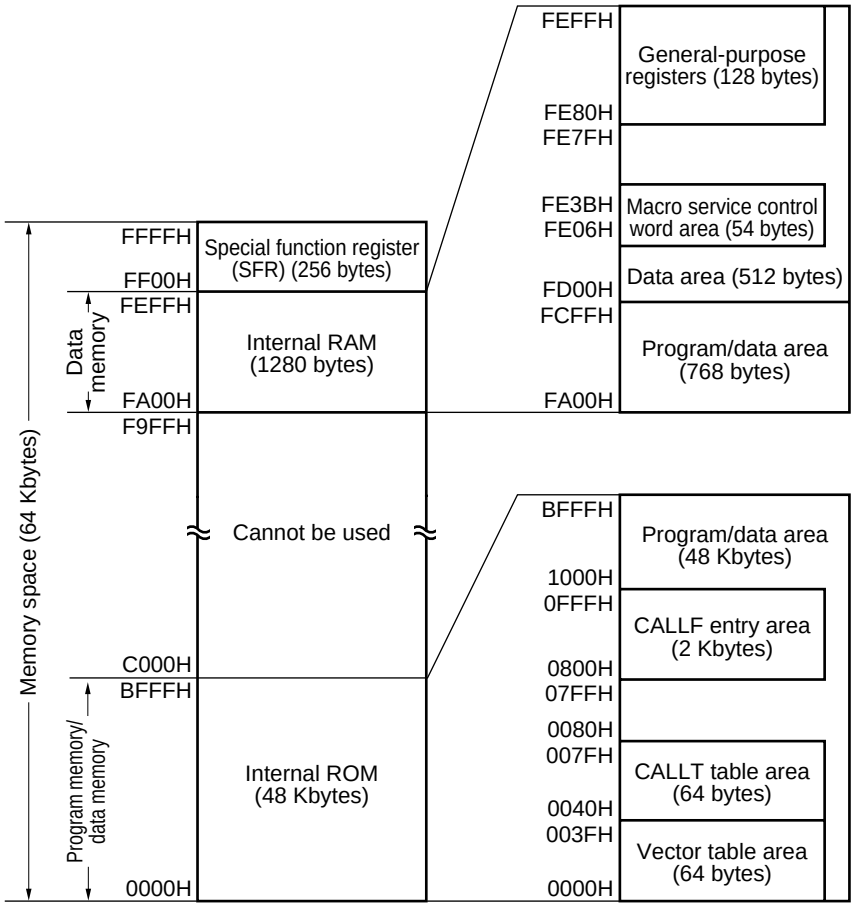
Table 3-1. Memory Space

★

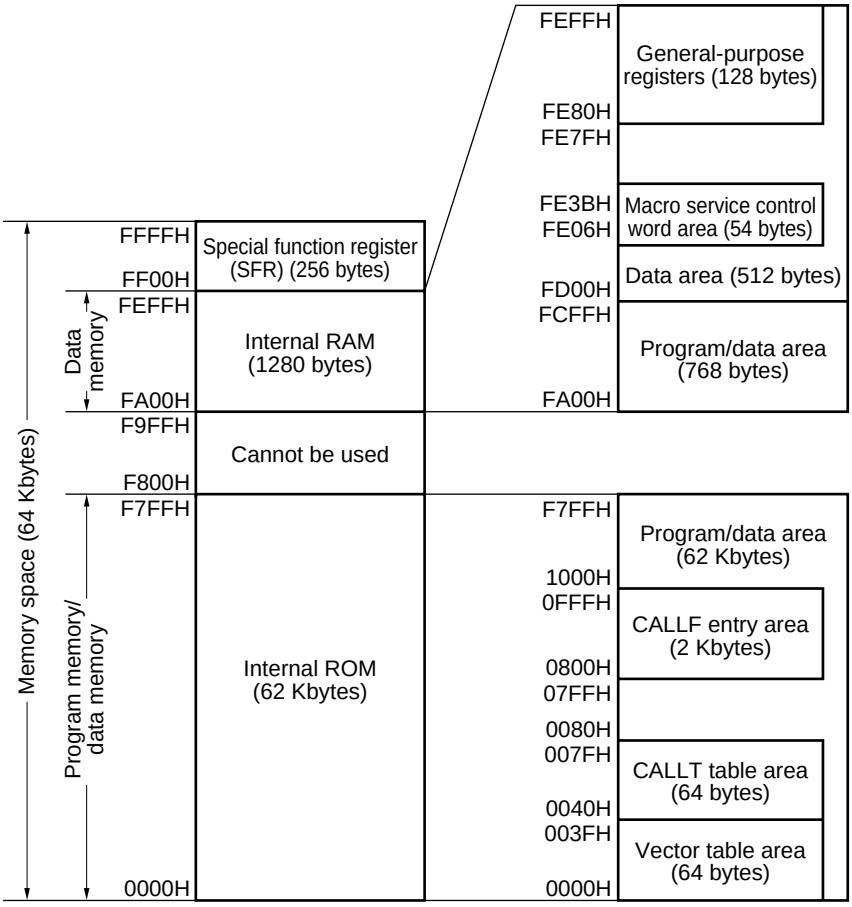
Part Number	Internal ROM Area	Internal Data Area
μPD784915A	0000H-BFFFH	FA00H-FFFFH
μPD784916A	0000H-F7FFH	

Caution Some products in the 78K/IV Series can access up to 1 Mbyte of memory space in an address expansion mode which is set by the LOCATION instruction. However, the memory space of the μPD784916A is 64K bytes (0000H through FFFFH). Therefore, be sure to execute the LOCATION 0 instruction immediately after reset to set the memory space to 64 Kbytes (the LOCATION instruction cannot be used more than once).

★ **Figure 3-2. Memory Map of μPD784915A**



★ **Figure 3-3. Memory Map of μPD784916A**



3.3 Special Function Registers (SFRs)

Special function registers are assigned special functions and mapped to a 256-byte space from addresses FF00H through FFFFH. These registers include mode registers and control registers that control the internal peripheral hardware units.

Caution Do not access an address to which no SFR is assigned. If such an address is accessed by mistake, the μPD784916A may be deadlocked. This deadlock can be cleared only by reset input.

Table 3-2 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Abbreviation ..... Abbreviation of an SFR. This abbreviation is reserved for NEC's assembler (RA78K4). With a C compiler (CC78K4), the abbreviation can be used as an sfr variable by the #pragma sfr instruction.

- R/W ..... Indicates whether the SFR in question can be read or written.
  R/W : Read/write
  R : Read only
  W : Write only

- Bit length ..... Indicates the bit length (word length) of the SFR.

- Bit units for manipulation ..... Indicates bit units in which the SFR in question can be manipulated. An SFR that can be manipulated in 16-bit units can be described as the operand sfrp of an instruction. Specify an even address to manipulate this SFR.
  An SFR that can be manipulated in 1-bit units can be described for a bit manipulation instruction.

- After reset ..... Indicates the status of each register after the $\overline{\text{RESET}}$ signal has been input.

Table 3-2. Special Function Registers (1/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Length	Bit Units for Manipulation			After Releasing Reset
					1 bit	8 bits	16 bits	
FF00H	Port 0	P0	R/W	8	○	○	–	Undefined
FF04H	Port 4	P4		8	○	○	–	
FF05H	Port 5	P5		8	○	○	–	
FF06H	Port 6	P6		8	○	○	–	
FF07H	Port 7	P7	R	8	○	○	–	
FF08H	Port 8	P8	R/W	8	○	○	–	
FF09H	Port 9	P9		8	○	○	–	
FF0EH	Port 0 buffer register L	P0L		8	○	○	–	
FF0FH	Port 0 buffer register H	P0H		8	○	○	–	
FF10H	Timer 0 compare register 0	CR00		16	–	–	○	Cleared to 0
FF11H	Event counter compare register 0	ECC0	W	8	–	○	–	
FF12H	Timer 0 compare register 1	CR01	R/W	16	–	–	○	
FF13H	Event counter compare register 1	ECC1	W	8	–	○	–	
FF14H	Timer 0 compare register 2	CR02	R/W	16	–	–	○	
FF15H	Event counter compare register 2	ECC2	W	8	–	○	–	
FF16H	Timer 1 compare register 0	CR10	R/W	16	–	–	○	
FF17H	Event counter compare register 3	ECC3	W	8	–	○	–	
FF18H	Timer 1 compare register 1	CR11	R/W	16	–	–	○	
FF1AH	Timer 1 compare register 2	CR12	R	16	–	–	○	
FF1CH	Timer 1 compare register 3	CR13	R/W	16	–	–	○	
FF1EH	Timer 2 compare register 0	CR20		16	–	–	○	
FF20H	Port 0 mode register	PM0	W	8	–	○	–	FFH
FF24H	Port 4 mode register	PM4		8	–	○	–	
FF25H	Port 5 mode register	PM5		8	–	○	–	
FF26H	Port 6 mode register	PM6		8	–	○	–	
FF28H	Port 8 mode register	PM8		8	–	○	–	FDH
FF29H	Port 9 mode register	PM9		8	–	○	–	7FH
FF2EH	Real-time output port 0 control register	RTPC	R/W	8	○	○	–	00H
FF30H	Timer register 0	TM0	R	16	–	–	○	Cleared to 0
FF31H	Event counter	EC	R/W	8	–	○	–	
FF32H	Timer register 1	TM1	R	16	–	–	○	
FF34H	Free running counter (bits 0 to 15)	FRCL		16	–	–	○	0000H
FF35H	Free running counter (bits 16 to 21)	FRCH		8	–	○	–	00H
FF36H	Timer register 2	TM2		16	–	–	○	Cleared to 0
FF38H	Timer control register 0	TMC0	R/W	8	○	○	–	00H
FF39H	Timer control register 1	TMC1		8	○	○	–	
FF3AH	Timer control register 2	TMC2		8	○	○	–	
FF3BH	Timer control register 3	TMC3		8	○	○	–	00×00000

Remark Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been deasserted (the contents before initialization are undefined).

Table 3-2. Special Function Registers (2/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Length	Bit Units for Manipulation			After Releasing Reset
					1 bit	8 bits	16 bits	
FF3CH	Timer register 3	TM3	R	16	–	–	○	Cleared to 0
FF3DH	Timer control register 4	TMC4	R/W	8	○	○	–	××000000
FF3EH	Timer register 4	TM4	R	16	–	–	○	Cleared to 0
FF48H	Port 8 mode control register	PMC8	R/W	8	○	○	–	00H
FF4DH	Trigger source select register	TRGS0		8	○	○	–	
FF4EH	Pull-up resistor option register L	PUOL		8	○	○	–	
FF4FH	Pull-up resistor option register H	PUOH		8	○	○	–	
FF50H	Input control register	ICR		8	○	○	–	10H
FF51H	Up/down counter count register	UDC		8	–	○	–	Undefined
FF52H	Event divider counter	EDV	R	8	–	○	–	Cleared to 0
FF53H	Capture mode register	CPTM	R/W	8	○	○	–	00H
FF54H	Timer register 5	TM5	R	16	–	–	○	Cleared to 0
FF56H	Timer 3 capture register 0	CPT30		16	–	–	○	
FF58H	Timer 0 output mode register	TOM0	W	8	–	○	–	××000000
FF59H	Timer 0 output control register	TOC0		8	–	○	–	00H
FF5AH	Timer 1 output mode register	TOM1[Note 1]	R/W	8	–	○	–	80H
FF5BH	Timer 1 output control register	TOC1	W	8	–	○	–	00H
FF5CH	Timer 3 compare register 0	CR30	R/W	16	–	–	○	Cleared to 0
FF5EH	Timer 3 compare register 1	CR31		16	–	–	○	
FF60H	Port 8 buffer register L	P8L		8	○	○	–	000×0×0×
FF63H	Up/down counter compare register	UDCC	W	8	–	○	–	Undefined
FF65H	Trigger source select register 1	TRGS1	R/W	8	○	○	–	00H
FF66H	Port 6 mode control register	PMC6		8	○	○	–	
FF68H	A/D converter mode register	ADM		16	–	–	○	0000H
		ADML[Note 2]		8	○	○	–	
FF6AH	A/D conversion result register	ADCR	R	8	–	○	–	Undefined
FF6CH	Hardware watch counter 0	HW0	R/W	16	–	–	○	Not affected
FF6EH	Hardware watch counter 1	HW1	R	16	–	–	○	by reset
FF6FH	Watch mode register	WM	R/W	8	○	○	–	00××0×00
FF70H	PWM control register 0	PWMC0	R/W	8	○	○	–	05H
FF71H	PWM control register 1	PWMC1		8	○	○	–	15H
FF72H	PWM0 modulo register	PWM0		16	–	–	○	0000H
FF73H	PWM2 modulo register	PWM2		8	–	○	–	00H
FF74H	PWM1 modulo register	PWM1		16	–	–	○	0000H
FF75H	PWM3 modulo register	PWM3		8	–	○	–	00H

Notes 1. When the timer 1 output mode register (TOM1) is read, the write sequence of the REC driver is read (bits 0 and 1).

2. ADML is the lower 8 bits of the A/D converter mode register (ADM) and can be manipulated in 1- or 8-bit units.

Remark Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been deasserted (the contents before initialization are undefined).

Table 3-2. Special Function Registers (3/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Bit Length	Bit Units for Manipulation			After Releasing Reset
						1 bit	8 bits	16 bits	
FF76H	PWM5 modulo register	PWM5		R/W	16	–	–	○	0000H
FF77H	PWM4 modulo register	PWM4			8	–	○	–	00H
FF78H	Event divider control register	EDVC		W	8	–	○	–	00H
FF79H	Clock output mode register	CLOM		R/W	8	○	○	–	00H
FF7AH	Timer 4 capture/compare register 0	CR40			16	–	–	○	Cleared to 0
FF7BH	Clock control register	CC			8	○	○	–	00H
FF7CH	Timer 4 capture register 1	CR41		R	16	–	–	○	Cleared to 0
FF7DH	Capture/compare control register	CRC		W	8	–	○	–	00H
FF7EH	Timer 5 compare register	CR50		R/W	16	–	–	○	Cleared to 0
FF84H	Serial mode register 1	CSIM1			8	○	○	–	00H
FF85H	Serial shift register 1	SIO1			8	–	○	–	Undefined
FF88H	Serial mode register 2	CSIM2			8	○	○	–	00H
FF89H	Serial shift register 2	SIO2			8	–	○	–	Undefined
FF8AH	Serial control register 2	CSIC2			8	–	○	–	00H
FF91H	Head amplifier switch output control register	HAPC			8	○	○	–	
FF94H	Amplifier control register	AMPC			8	○	○	–	
FF95H	Amplifier mode register 0	AMPM0			8	○	○	–	
FF96H	Amplifier mode register 1	AMPM1			8	○	○	–	
FF97H	Gain control register	CTLM			8	○	○	–	
FFA0H	External interrupt mode register	INTM0			8	○	○	–	000000×0
FFA1H	External capture mode register 1	INTM1			8	○	○	–	00H
FFA2H	External capture mode register 2	INTM2			8	○	○	–	
FFA6H	Key interrupt control register	KEYC			8	○	○	–	70H
FFA8H	In-service priority register	ISPR		R	8	○	○	–	00H
FFAAH	Interrupt mode control register	IMC		R/W	8	○	○	–	80H
FFACH	Interrupt mask flag register	MK0L	MK0		8	○	○	○	FFH
FFADH		MK0H			8	○	○		
FFAEH		MK1L	MK1		8	○	○	○	
FFAFH		MK1H			8	○	○		
FFB0H	FRC capture register 0L	CPT0L		R	16	–	–	○	Cleared to 0
FFB1H	FRC capture register 0H	CPT0H			8	–	○	–	
FFB2H	FRC capture register 1L	CPT1L			16	–	–	○	
FFB3H	FRC capture register 1H	CPT1H			8	–	○	–	
FFB4H	FRC capture register 2L	CPT2L			16	–	–	○	
FFB5H	FRC capture register 2H	CPT2H			8	–	○	–	
FFB6H	FRC capture register 3L	CPT3L			16	–	–	○	
FFB7H	FRC capture register 3H	CPT3H			8	–	○	–	
FFB8H	FRC capture register 4L	CPT4L			16	–	–	○	

Remark Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been deasserted (the contents before initialization are undefined).

Table 3-2. Special Function Registers (4/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Length	Bit Units for Manipulation			After Releasing Reset
					1 bit	8 bits	16 bits	
FFB9H	FRC capture register 4H	CPT4H	R	8	–	○	–	Cleared to 0
FFBAH	FRC capture register 5L	CPT5L		16	–	–	○	
FFBBH	FRC capture register 5H	CPT5H		8	–	○	–	
FFC0H	Standby control register	STBC	R/W	8	–	○	–	0000×000
FFC4H	Execution speed select register	MM	W	8	–	○	–	20H
FFCEH	CPU clock status register	PCS	R	8	○	○	–	00H
FFCFH	Oscillation stabilization time specification register	OSTS	W	8	–	○	–	
FFE0H	Interrupt control register (INTP0)	PIC0	R/W	8	○	○	–	43H
FFE1H	Interrupt control register (INTCPT3)	CPTIC3		8	○	○	–	
FFE2H	Interrupt control register (INTCPT2)	CPTIC2		8	○	○	–	
FFE3H	Interrupt control register (INTCR00)	CRIC12		8	○	○	–	
FFE4H	Interrupt control register (INTCR00)	CRIC00		8	○	○	–	
FFE5H	Interrupt control register (INTCLR1)	CLRIC1		8	○	○	–	
FFE6H	Interrupt control register (INTCR10)	CRIC10		8	○	○	–	
FFE7H	Interrupt control register (INTCR01)	CRIC01		8	○	○	–	
FFE8H	Interrupt control register (INTCR02)	CRIC02		8	○	○	–	
FFE9H	Interrupt control register (INTCR11)	CRIC11		8	○	○	–	
FFEAH	Interrupt control register (INTCPT1)	CPTIC1		8	○	○	–	
FFEBH	Interrupt control register (INTCR20)	CRIC20		8	○	○	–	
FFEDH	Interrupt control register (INTTB)	TBIC		8	○	○	–	
FFEEH	Interrupt control register (INTAD)	ADIC		8	○	○	–	
FFEFH	Interrupt control register (INTP2)[Note]	PIC2		8	○	○	–	
	Interrupt control register (INTCR40)[Note]	CRIC40						
FFF0H	Interrupt control register (INTUDC)	UDCIC		8	○	○	–	
FFF1H	Interrupt control register (INTCR30)	CRIC30		8	○	○	–	
FFF2H	Interrupt control register (INTCR50)	CRIC50		8	○	○	–	
FFF3H	Interrupt control register (INTCR13)	CRIC13		8	○	○	–	
FFF4H	Interrupt control register (INTCSI1)	CSIIC1		8	○	○	–	
FFF5H	Interrupt control register (INTW)	WIC		8	○	○	–	
FFF7H	Interrupt control register (INTP1)	PIC1		8	○	○	–	
FFF8H	Interrupt control register (INTP3)	PIC3		8	○	○	–	
FFFAH	Interrupt control register (INTCSI2)	CSIIC2		8	○	○	–	

Note PIC2 and CRIC40 are at the same address (register).

Remark Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been deasserted (the contents before initialization are undefined).

3.4 PORTS

The μPD784916A is provided with the ports shown in Figure 3-4. Table 3-3 shows the function of each port.

Figure 3-4. Port Configuration

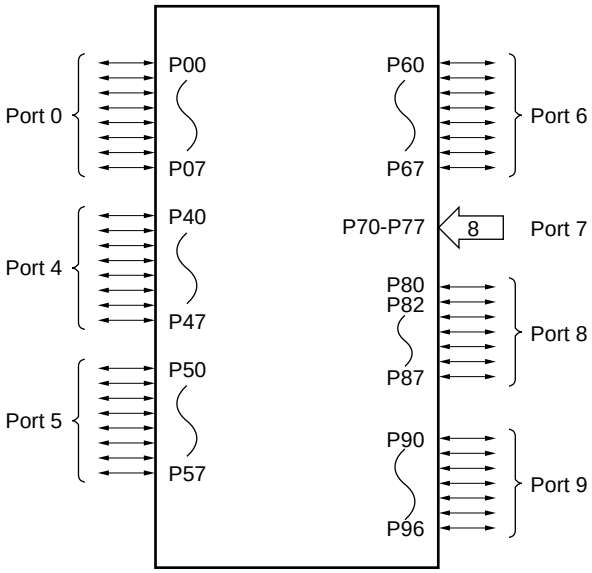


Table 3-3. Port Function

Name	Pin Name	Function	Specification of Pull-up Resistor
Port 0	P00-P07	Can be set in input or output mode in 1-bit units.	Pull-up resistors are connected to all pins in input mode.
Port 4	P40-P47		
Port 5	P50-P57		
Port 6	P60-P67		
Port 7	P70-P77	Input port	Pull-up resistor is not provided.
Port 8	P80, P82-P87	Can be set in input or output mode in 1-bit units.	Pull-up resistors are connected to all pins in input mode.
Port 9	P90-P96		

3.5 Real-time Output Port

A real-time output port consists of a port output latch and a buffer register (refer to **Figure 3-5**).

The function to transfer the data prepared in advance in the buffer register to the output latch when a trigger such as a timer interrupt occurs, and output the data to an external device is called a real-time output function. A port used in this way is called a real-time output port (RTP).

Table 3-4 shows the real-time output ports of the μPD784916A.

Table 3-5 shows the trigger sources of RTPs.

Figure 3-5. Configuration of RTP

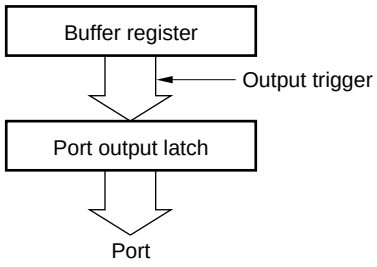


Table 3-4. Bit Configuration of RTP

RTP	Alternate Function	Number of Bits of Real-Time Output Data	Number of Bits That Can Be Specified as RTP	Remark
RTP0	Port 0	4 bits x 2 channels or 8 bits x 1 channel	4-bit units	–
RTP8	Port 8	1 bit x 1 channel and 2 bits x 1 channel	1-bit units	Pseudo V_{SYNC} output: 1 channel (RTP80) Head amplifier switch: 1 channel (RTP82) Chrominance rotation signal output: 1 channel (RTP83)

Table 3-5. Trigger Sources of RTP

RTP \ Trigger Source		INTCR00	INTCR01	INTCR02	INTCR13	INTCR50	INTCR0	Remark
RTP0	Higher 4 bits		○					
	Lower 4 bits			○			○	
	All 8 bits			○			○	
RTP8	Bit 0		○	○	○	○		**Note 1**
	Bits 2 and 3	○						**Note 2**

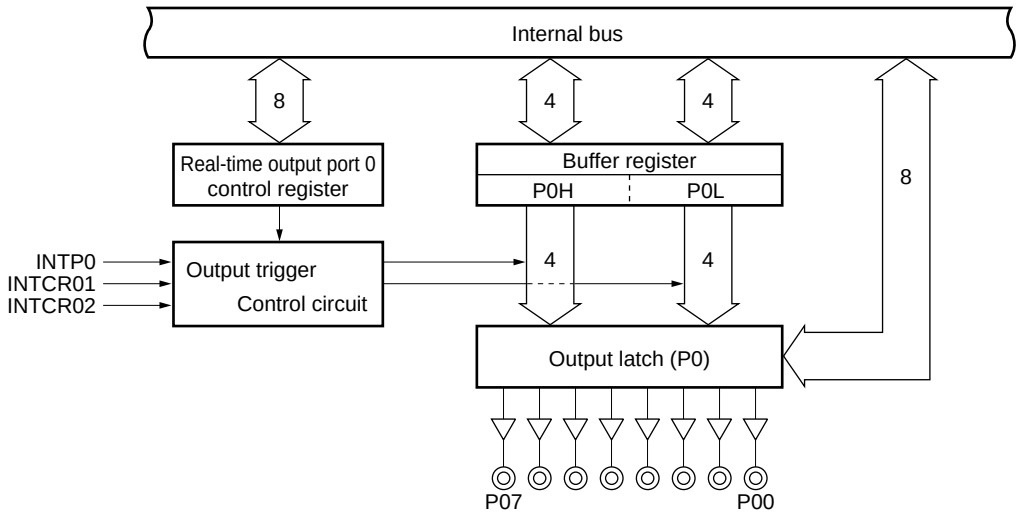
Notes 1. Select one of the four trigger sources.

2. When the real-time output port mode is set by the port mode control register 8 (PMC8), the HASW and ROT-C signals that are set by the head amplifier switch output control register (HAPC) are directly output. The HASW and ROT-C signals are synchronized with HSW output (TM0-CR00 coincidence signal). However, the set signal is output immediately when the HAPC register is rewritten.

Figures 3-6 and 3-7 show the block diagrams of RTP0 and RTP8.

Figure 3-8 shows the types of RTP output trigger sources.

Figure 3-6. Block Diagram of RTP0



Remark INTCR01: TM0-CR01 coincidence signal
INTCR02: TM0-CR02 coincidence signal

Figure 3-7. Block Diagram of RPT8

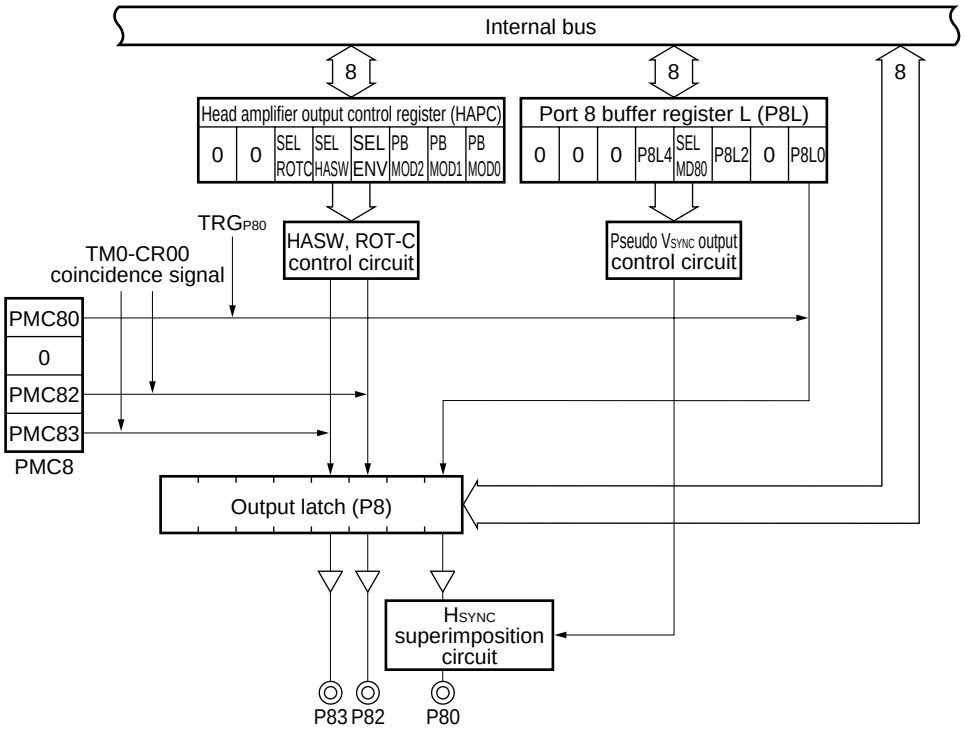
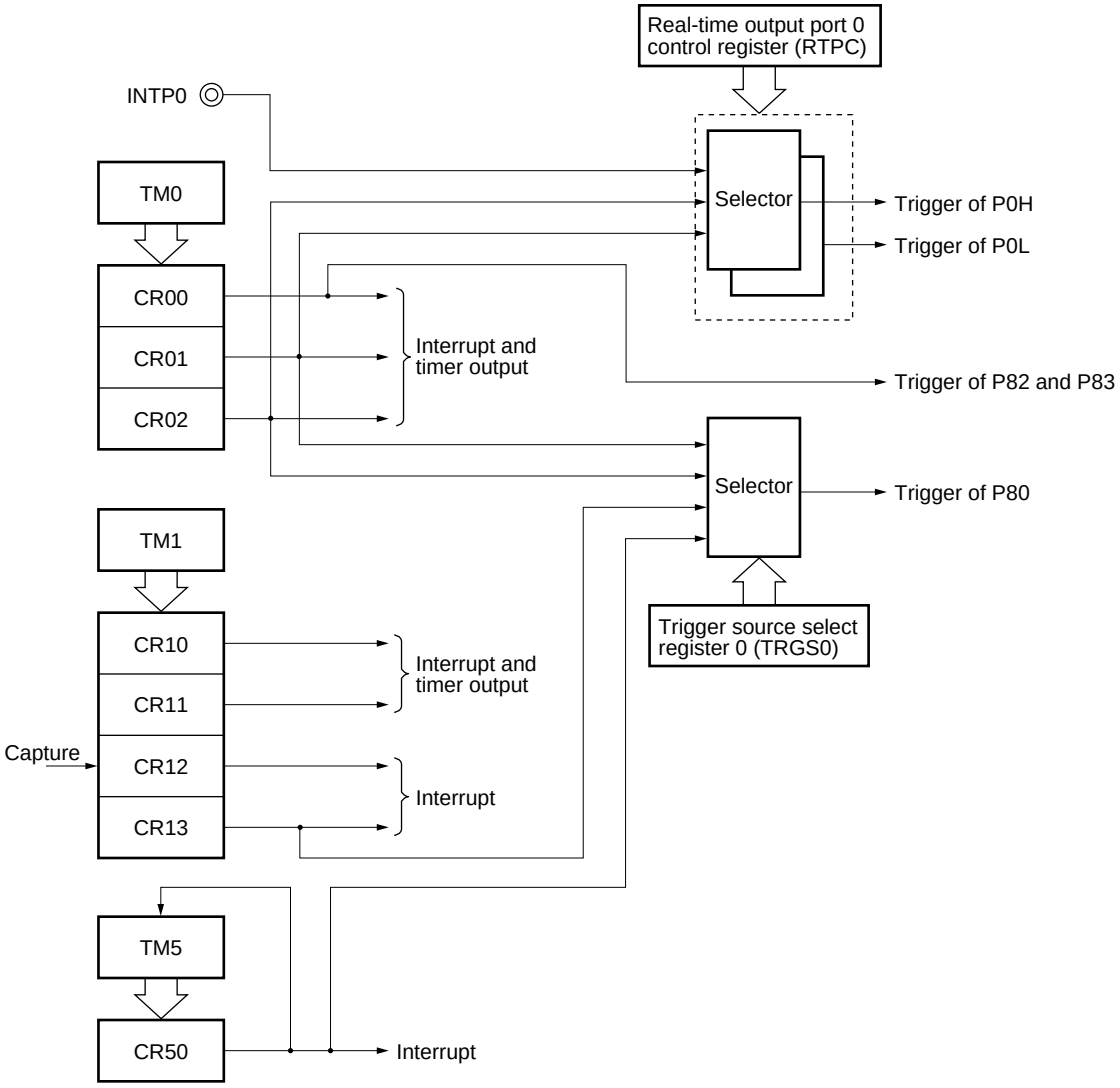


Figure 3-8. Types of RTP Output Trigger Sources



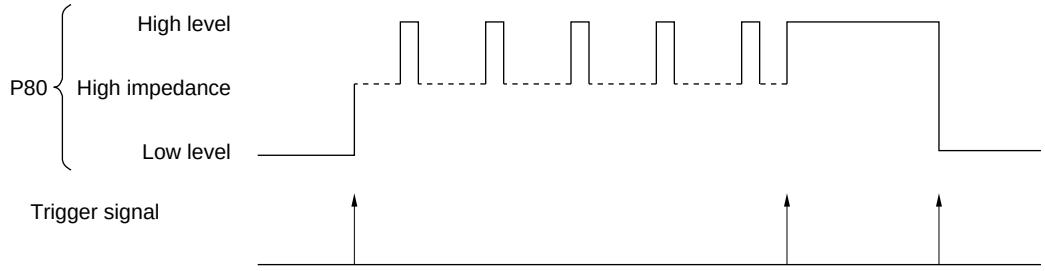
RTP80 can output low-level, high-level, and high-impedance values real-time.

Because RTP80 can superimpose a horizontal sync signal, it can be used to create a pseudo vertical sync signal. When RTP80 is set in the pseudo V_{SYNC} output mode, it repeatedly outputs a specific pattern when an output trigger occurs.

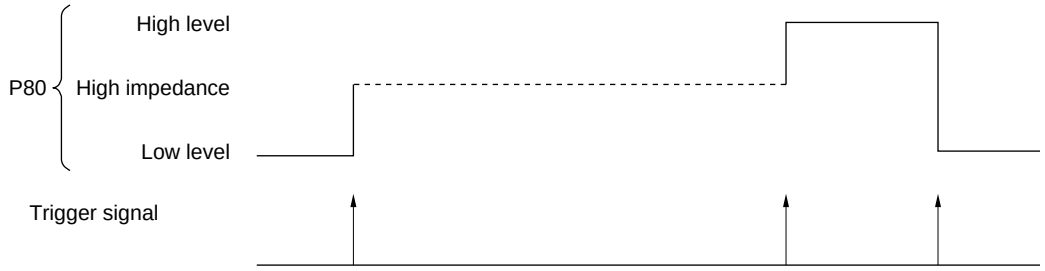
Figure 3-9 shows the operation timing of RTP80.

Figure 3-9. Example of Operation Timing of RTP80

(a) When H_{SYNC} signal is superimposed



(b) Pseudo V_{SYNC} output mode



3.6 Super Timer Unit

The μPD784916A is provided with a super timer unit that consists of the timers shown in Table 3-6.

Table 3-6. Configuration of Super Timer Unit

Unit Name	Timer/Counter	Resolution	Maximum Count Time	Register	Remark
Timer 0	TM0 (16-bit timer)	1 μs	65.5 ms	CR00	Controls delay of video head switching signal
				CR01	Controls delay of audio head switching signal
				CR02	Controls pseudo V_{SYNC} output timing
	EC (8-bit counter)	–	–	ECC0, ECC1, ECC2, ECC3	Creates internal head switching signal
Free running counter	FRC (22-bit counter)	125 ns	524 ms	CPT0	Detects reference phase (to control drum phase)
				CPT1	Detects phase of drum motor (to control drum phase)
				CPT2	Detects speed of drum motor (to control drum speed)
				CPT3	Detects speed of capstan motor (to control speed of capstan motor)
				CPT4, CPT5	Detects remaining tape for reel FG
Timer 1	TM1 (16-bit timer)	1 μs	65.5 ms	CR10	Playback: Creates internal reference signal Recording: Buffer oscillator in case V_{SYNC} is missing
				CR11	Controls RECCTL output timing
				CR12	Detects phase of capstan motor (to control capstan phase)
				CR13	Controls V_{SYNC} mask as noise prevention measures
	TM3 (16-bit timer)	1 μs or 1.1 μs	65.5 ms or 71.5 ms	CR30, CR31	Controls duty detection timing of PBCTL signal
				CPT30	Measures cycle of PBCTL signal
	EDV (8-bit counter)	–	–	EDVC	Divides CFG signal frequency
Timer 2	TM2 (16-bit timer)	1 μs	65.5 ms	CR20	Can be used as interval timer (to control system)
Timer 4	TM4 (16-bit timer)	2 μs	131 ms	CR40	Detects duty of remote controller signal (to decode remote controller signal)
				CR41	Measures cycle of remote controller signal (to decode remote controller signal)
Timer 5	TM5 (16-bit timer)	2 μs	131 ms	CR50	Can be used as interval timer (to control system)
Up/down counter	UDC (5-bit counter)	–	–	UDCC	Creates linear tape counter
PWM output unit	–	–	–	PWM0, PWM1, PWM5	16-bit resolution (carrier frequency: 62.5 kHz)
				PWM2, PWM3, PWM4	8-bit resolution (carrier frequency: 62.5 kHz)

(1) Timer 0 unit

Timer 0 unit creates head switching signal and pseudo V_{SYNC} output timing from the PG and FG signals of the drum motor.

This unit consists of an event counter (EC: 8 bits), four compare registers (ECC0 through ECC3), a timer (TM0: 16 bits), and three compare registers (CR00 through CR02).

A signal indicating coincidence between the value of timer 0 and the value of a compare register can be used as the output trigger of the real-time output port.

(2) Free running counter unit

The free running counter unit detects the speed and phase of the drum motor, and the speed and reel speed of the capstan motor.

This unit consists of a free running counter (FRC), six capture registers (CPT0 through CPT5), a V_{SYNC} separation circuit, and a H_{SYNC} separation circuit.

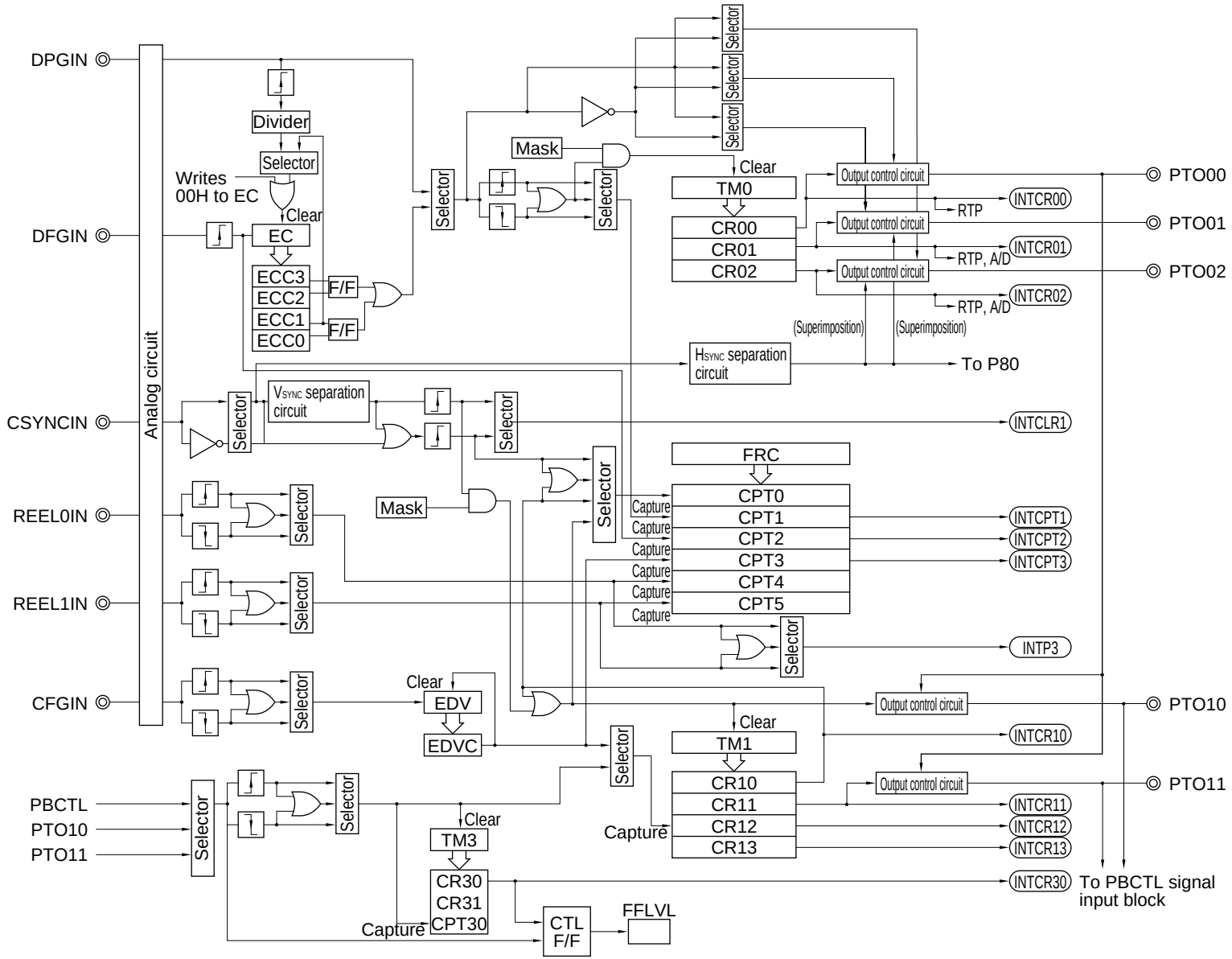
(3) Timer 1 unit

Timer 1 unit is a reference timer unit synchronized with the frame cycle and creates the RECCTL signal, detects the phase of the capstan motor, and detects the duty factor of the PBCTL signal. This unit consists of the following three groups:

- Timer 1 (TM1), compare registers (CR10, CR11, and CR13), and capture register (CR12)
- Timer 3 (TM3), compare registers (CR30 and CR31), and capture register (CPT30)
- Event divider counter (EDV) and compare register (EDVC)

The TM1-CR13 coincidence signal can be used for automatic unmasking of V_{SYNC} or as the output trigger of the real-time output port.

★ **Figure 3-10. Block Diagram of Super Timer Unit (TM0, FRC, TM1)**



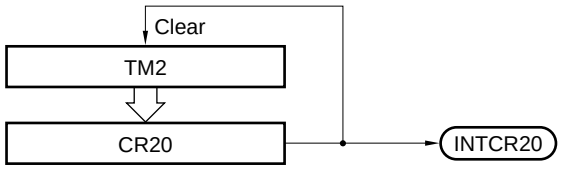
(4) Timer 2 unit

Timer 2 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer 2 (TM2) and a compare register (CR20).

The timer is cleared when the TM2-CR20 coincidence signal occurs, and at the same time, an interrupt is generated.

Figure 3-11. Block Diagram of Timer 2 Unit



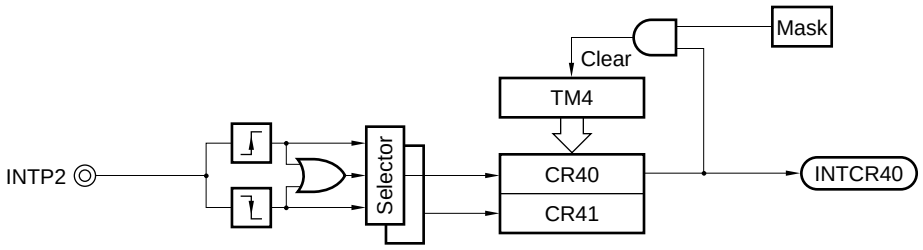
(5) Timer 4 unit

Timer 4 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer 4 (TM4), a capture/compare register (CR40), and a capture register (CR41).

The value of the timer is captured to CR40/CR41 when the INTP2 signal is input. This timer can be used to decode a remote controller signal.

Figure 3-12. Block Diagram of Timer 4 Unit



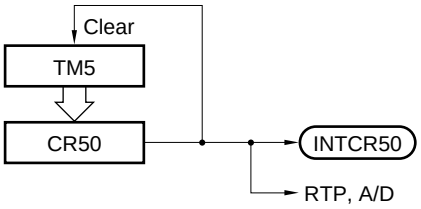
(6) Timer 5 unit

Timer 5 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer 5 (TM5) and a compare register (CR50).

The timer is cleared by the TM5-CR50 coincidence signal, and at the same time, an interrupt is generated.

Figure 3-13. Block Diagram of Timer 5 Unit



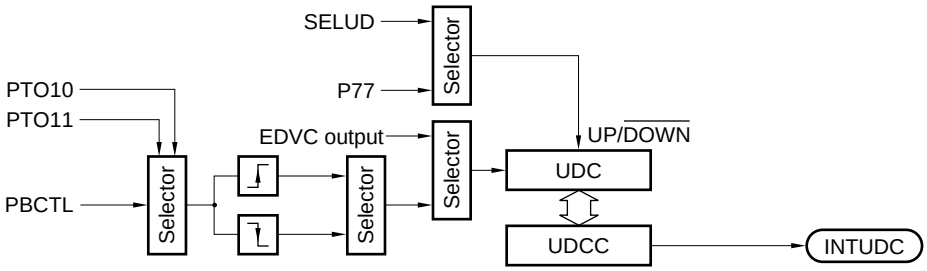
(7) Up/down counter unit

The up/down counter unit is a counter that realizes a linear time counter.

This unit consists of an up/down counter (UDC) and a compare register (UDCC).

The up/down counter counts up the rising edges of PBCTL and counts down the falling edges of PBCTL. When the value of the up/down counter coincides with the value of the compare register, or when the counter underflows, an interrupt is generated.

Figure 3-14. Block Diagram of Up/Down Counter Unit



(8) PWM output unit

The PWM output unit has three 16-bit accuracy output lines (PWM0, PWM1, and PWM5) and 8-bit accuracy output lines (PWM2 through PWM4). The carrier frequency of all the output lines is 62.5 kHz (f_{CLK} = 8 MHz). PWM0 and PWM1 can be used to control the drum motor and capstan motor.

Figure 3-15. Block Diagram of 16-Bit PWM Output Unit

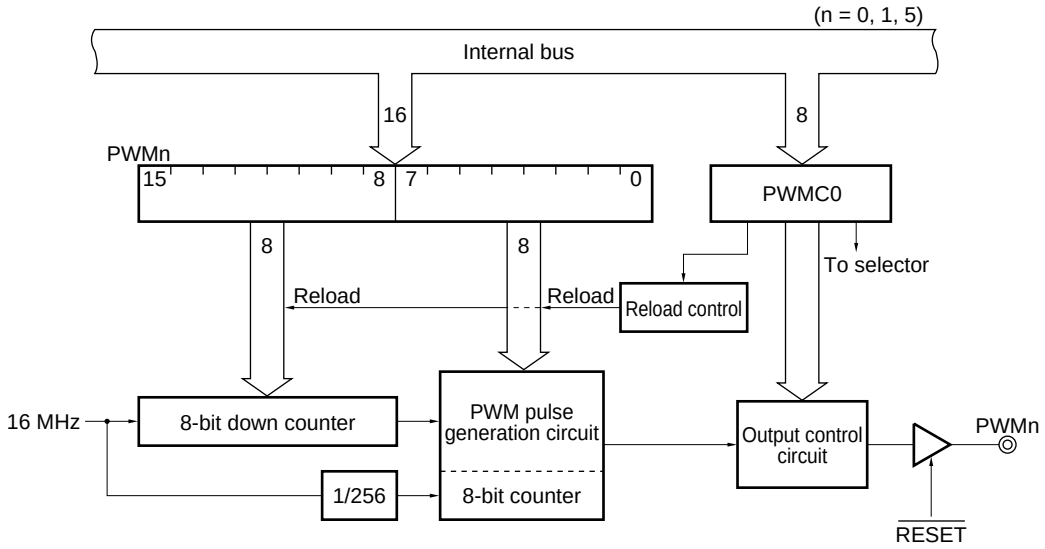
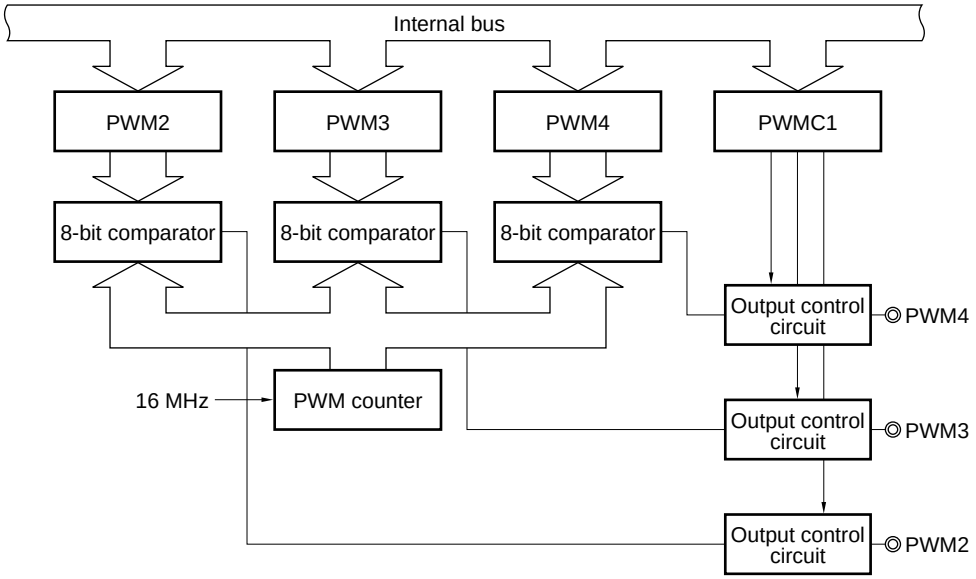


Figure 3-16. Block Diagram of 8-Bit PWM Output Unit



3.7 Serial Interface

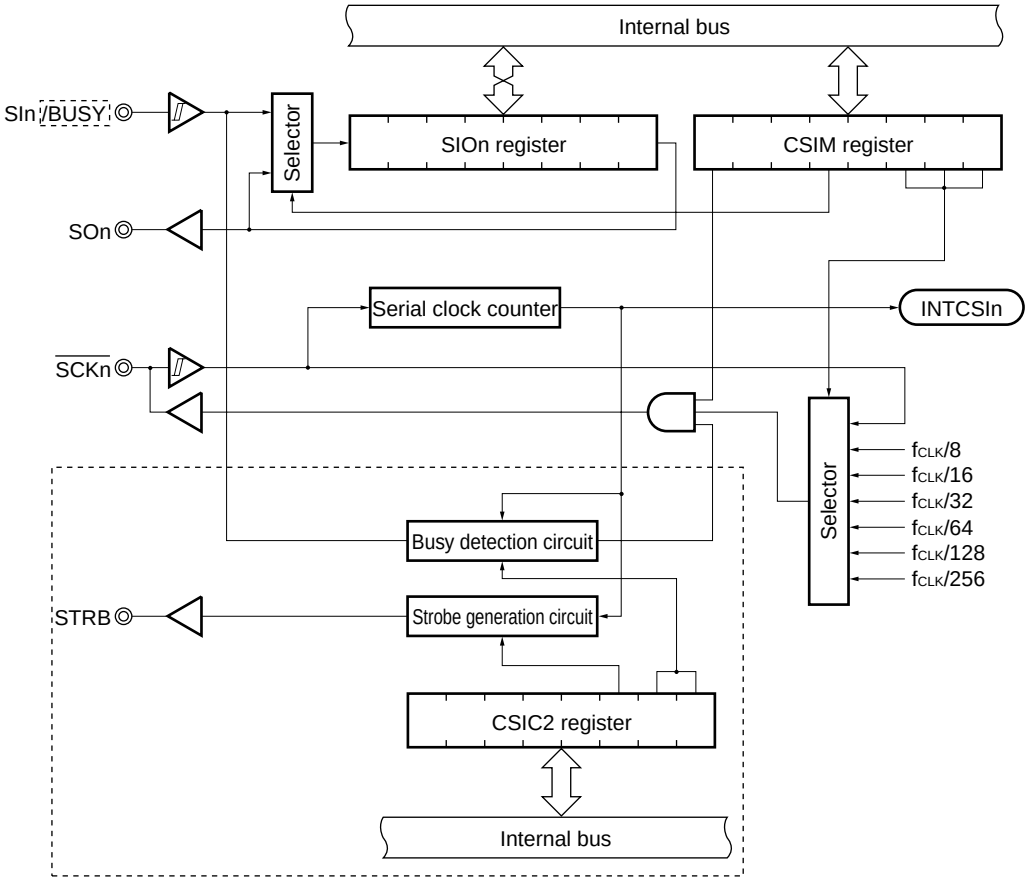
The μPD784916A is provided with the serial interfaces shown in Table 3-7.

Data can be automatically transmitted or received through these serial interfaces, when the macro service is used.

Table 3-7. Types of Serial Interfaces

Name	Function
Serial interface channel 1	• Clocked serial interface (3-wire) • Bit length: 8 bits • Clock rate: External clock/31.25 kHz/62.5 kHz/125 kHz/250 kHz/500 kHz/1 MHz (f_{CLK} = 8 MHz) • MSB first/LSB first selectable
Serial interface channel 2	• Clocked serial interface (3-wire) • Bit length: 8 bits • Clock rate: External clock/31.25 kHz/62.5 kHz/125 kHz/250 kHz/500 kHz/1 MHz (f_{CLK} = 8 MHz) • MSB first/LSB first selectable • BUSY/STRB control function

Figure 3-17. Block Diagram of Serial Interface Channel n (n = 1 or 2)



Remark The circuits enclosed in the broken line are provided for serial interface channel 2 only.

3.8 A/D Converter

The μPD784916A has an analog-to-digital (A/D) converter with 12 multiplexed analog inputs (ANI0 through ANI11).

This A/D converter is of successive approximation type, and the conversion result is held by an 8-bit A/D conversion result register (ADCR) (conversion time: 10 μs at f_{CLK} = 8 MHz).

A/D conversion can be started in the following two modes:

- Hardware start: Conversion is started by a hardware trigger[Note].
- Software start : Conversion is started by setting the A/D conversion mode register (ADM).

After conversion has been started, the A/D converter operates in the following modes:

- Scan mode : Sequentially selects more than one analog input to obtain data to be converted from all the pins.
- Select mode: Use only one pin for analog input to obtain successive data.

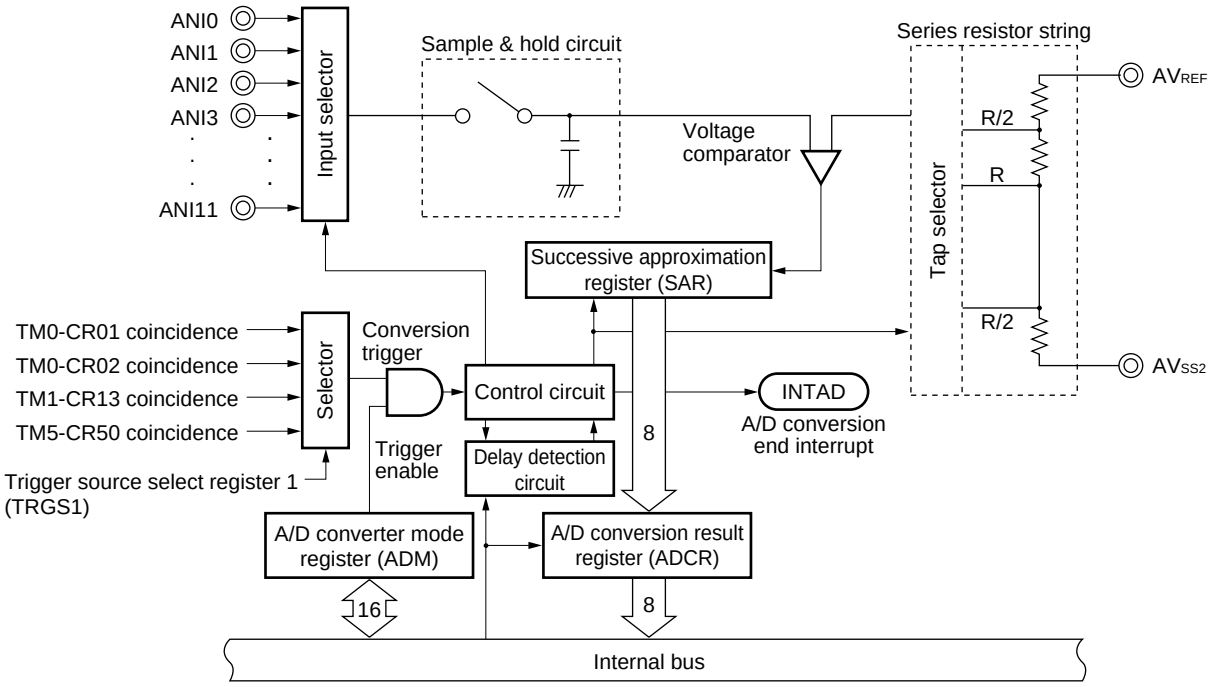
When the conversion result is transferred to ADCR, interrupt request INTAD is generated. By processing this interrupt with the macro service, the conversion result can be successively transferred to memory.

A mode in which starting A/D conversion of the next pin is kept pending until the value of ADCR is read is also available. When this mode is used, reading the conversion result by mistake when timing is shifted because an interrupt is disabled can be prevented.

Note A hardware trigger can be one of the following coincidence signals, one of which is selected by the trigger source select register 1 (TRGS1):

- TM0-CR01 coincidence signal
- TM0-CR02 coincidence signal
- TM1-CR13 coincidence signal
- TM5-CR50 coincidence signal

Figure 3-18. Block Diagram of A/D Converter



3.9 VCR Analog Circuits

The μPD784916A is provided with the following VCR analog circuits:

- CTL amplifier
- RECCTL driver (rewritable)
- DPG comparator
- DFG amplifier
- DPFG separation circuit (ternary separation circuit)
- CFG amplifier
- Reel FG comparator (2 channels)
- CSYNC comparator

(1) CTL amplifier/RECCTL driver

The CTL amplifier is used to amplify the playback control (PBCTL) signal that is reproduced from the CTL signal recorded on a VCR tape.

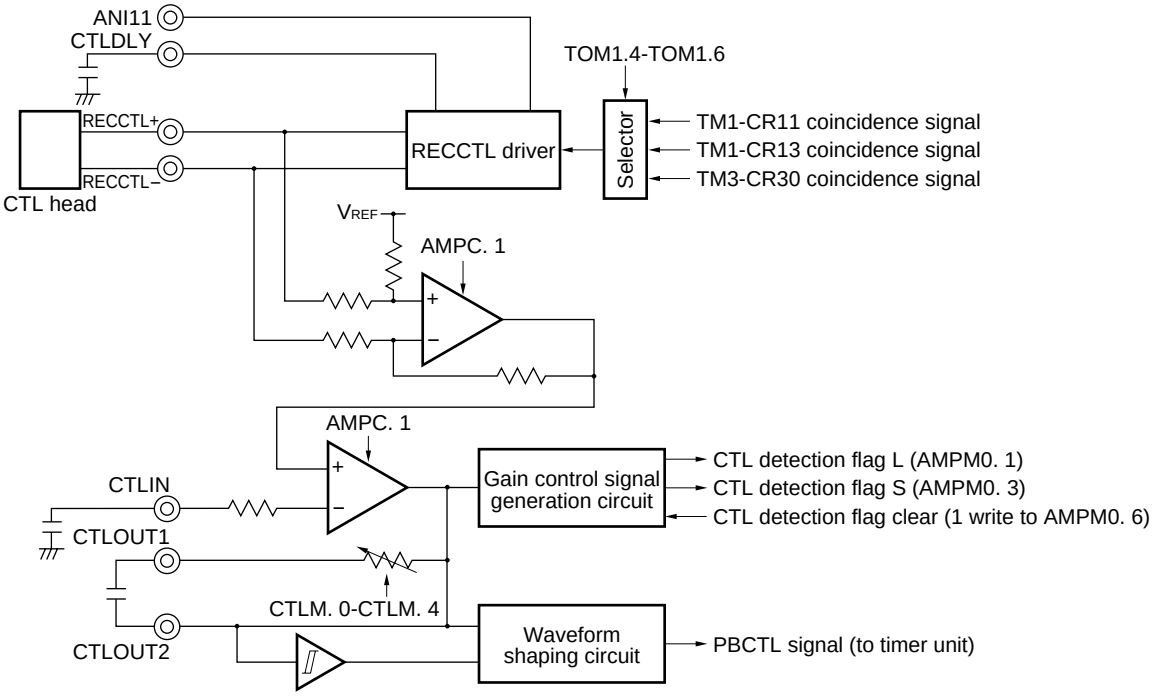
The gain of the CTL amplifier is set by the gain control register (CTLM). Thirty-two types of gains can be set in increments of about 1.78 dB.

The μPD784195 is also provided with a gain control signal generation circuit that monitors the status of the amplifier output to perform optimum gain control by program. The gain control signal generation circuit generates a CTL detection flag that identifies the amplitude status of the CTL amplifier output. By using this CTL detection flag, the gain of the CTL amplifier can be optimized.

The RECCTL driver writes a control signal onto a VCR tape.

This driver operates in two modes: REC mode that is used for recording, and rewrite mode used to rewrite the VISS signal. The output status of the RECCTL± pin is changed by hardware, by using the timer output from the super timer unit as a trigger.

Figure 3-19. Block Diagram of CTL Amplifier and RECCTL Driver



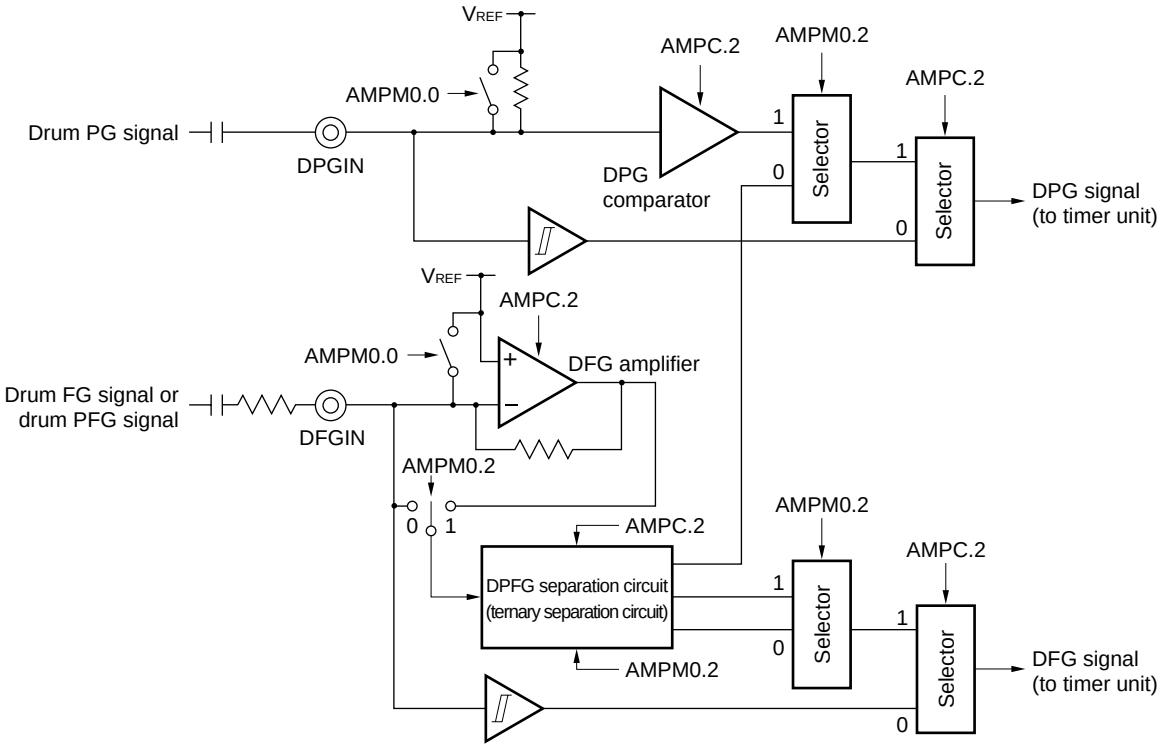
(2) DPG comparator, DFG amplifier, and DPFG separation circuit

The DPG comparator converts the drum PG (DPG) signal that indicates the phase information of the drum motor into a logic signal.

The DFG amplifier amplifies the drum FG (DFG) signal that indicates the speed information of the drum motor.

The DPFG separation circuit (ternary separation circuit) separates a drum PFG (DPFG) signal having speed and phase information into a DFG and DPG signals.

Figure 3-20. Block Diagram of DPG Comparator, DFG Amplifier, and DPFG Separation Circuit

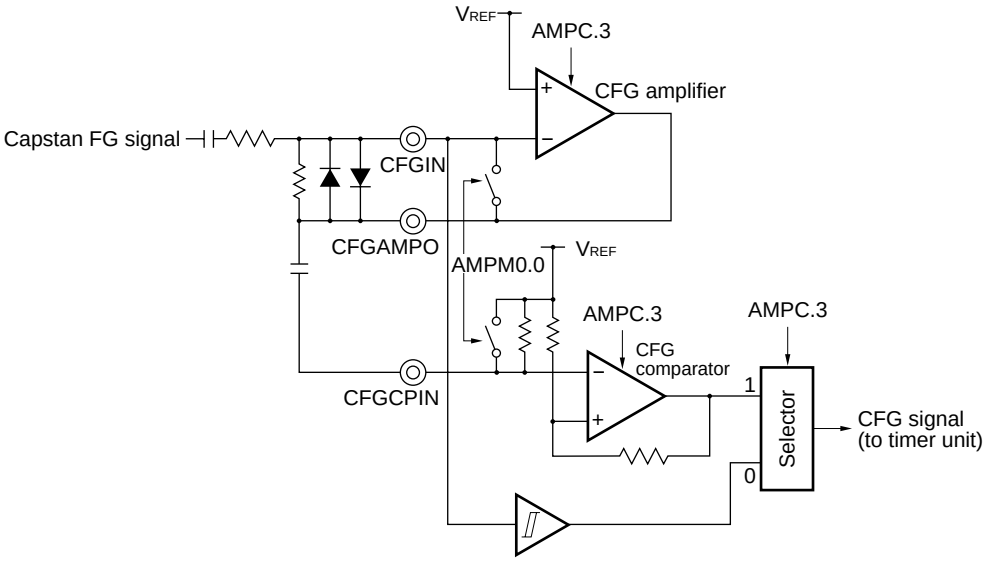


(3) CFG amplifier

The CFG amplifier amplifies the capstan FG (CFG) signal that indicates the speed information of the capstan motor. This amplifier consists of an operational amplifier and a comparator. The gain of the operational amplifier is set by using an external resistor.

When the gain of the operational amplifier is set to 50 dB, the output duty accuracy of the CFG signal can be improved to 50.0 ± 0.3%.

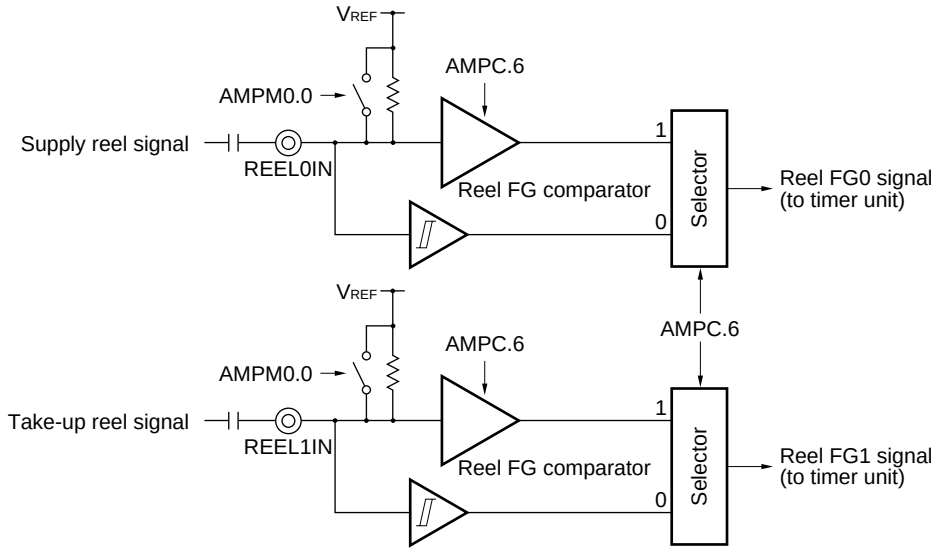
Figure 3-21. Block Diagram of CFG Amplifier



(4) Reel FG comparators

The reel FG comparator converts a reel FG signal that indicates the speed information of the reel motor into a logic signal. Two comparators, one for take-up and the other for supply, are provided.

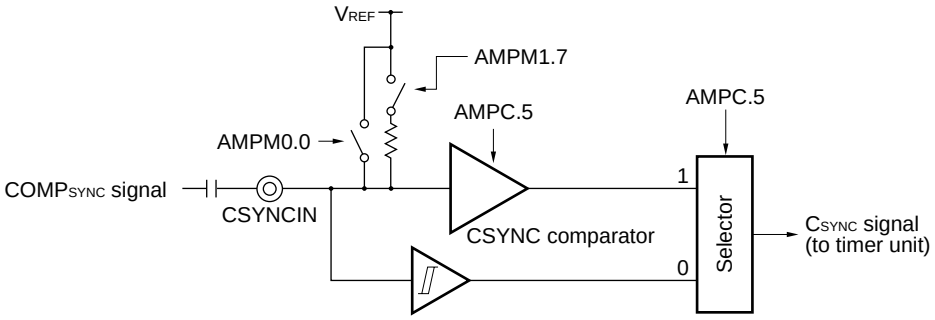
Figure 3-22. Block Diagram of Reel FG Comparators



(5) CSYNC comparator

The CSYNC comparator converts the COMPSYNC signal into a logic signal.

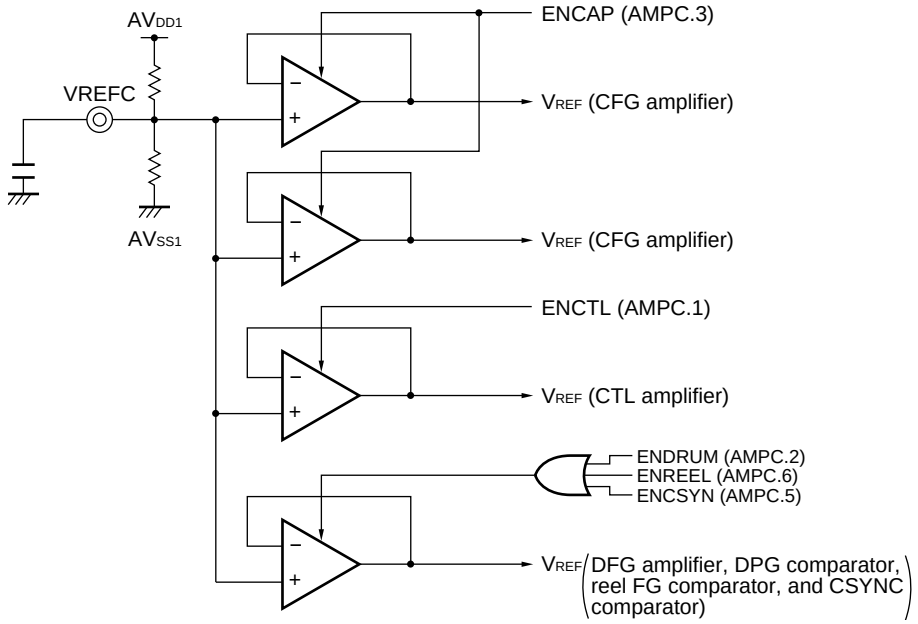
Figure 3-23. Block Diagram of COMPSYNC Comparator



(6) Reference amplifier

The reference amplifier generates a reference voltage (V_{REF}) to be supplied to the internal amplifiers and comparators of the μPD784916A.

Figure 3-24. Block Diagram of Reference Amplifier



Remark Multiple reference amplifiers are provided to assure the accuracy of the amplifiers and comparators.

3.10 Watch Function

The μPD784916A has a watch function that counts the overflow signals of the watch timer by hardware. As the clock, the subsystem clock (32.768 kHz) is used.

Because this watch function is independent of the CPU, it can be used even while the CPU is in the standby mode (STOP mode) or is reset. In addition, this function can be used at a low voltage of V_{DD} = 2.7 V (MIN.).

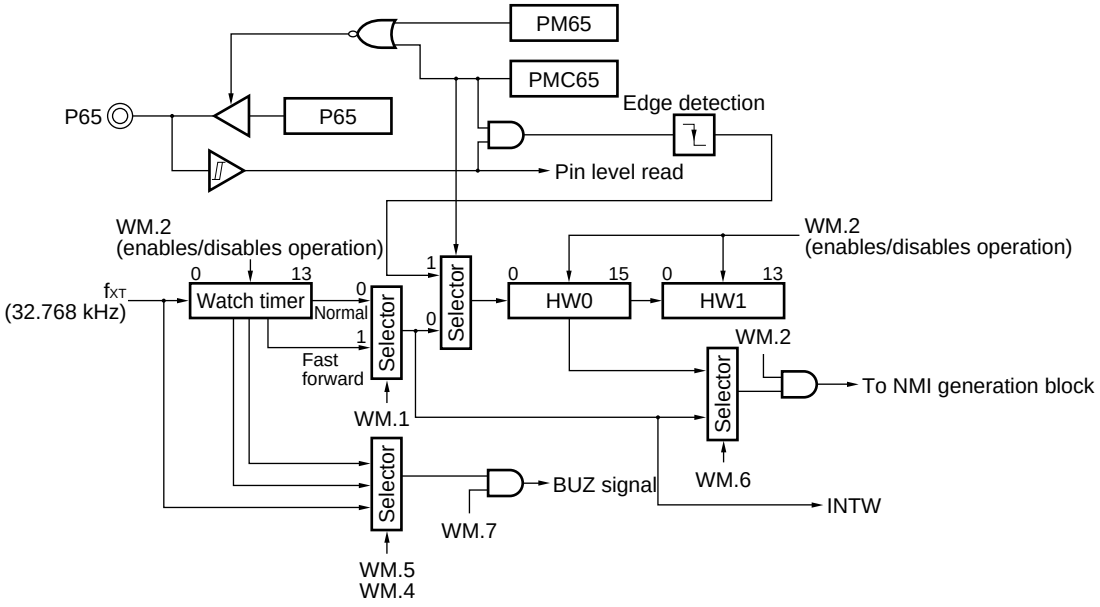
Therefore, by using only the watch function with the CPU set in the standby mode or reset, a watch operation can be performed at a low voltage and low current dissipation.

In addition, the watch function can also be used while the CPU is in the normal operation mode, because a dedicated counter is provided.

The watch function can be used to count up to about 17 years of data.

The hardware watch counters (HW0 and HW1) are shared with external input counters. These counters execute counting at the falling edge of input to the P65 pin, and can be used to count the H_{SYNC} signals.

★ **Figure 3-25. Block Diagram of Watch Counter**



3.11 Clock Output Function

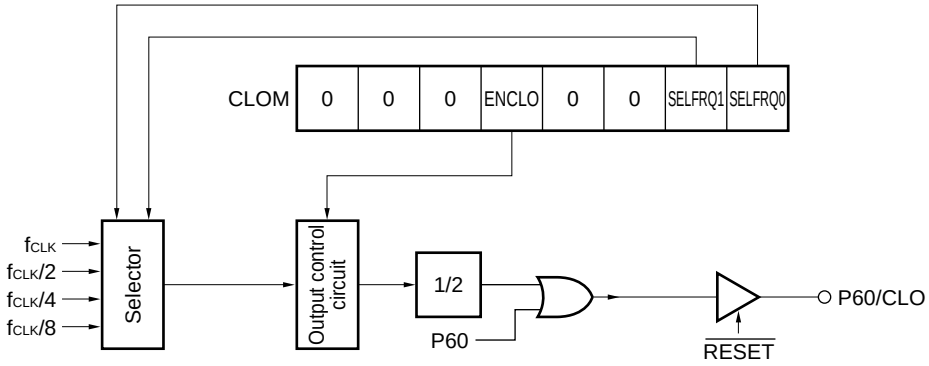
The μPD784916A can output a square wave (with a duty factor of 50%) to the P60/CLO pin as the operating clock for the peripheral devices or other microcomputers. To enable or disable the clock output, and to set the frequency of the clock, the clock output mode register (CLOM) is used.

When setting the frequency, the division ratio can be set to f_{CLK}/n (where n = 2, 4, 8, or 16) ($f_{CLK} = f_{OSC}/2$: f_{OSC} is the oscillation frequency of the oscillator).

Figure 3-26 shows the configuration of the clock output circuit.

The clock output (CLO) pin is shared with P60.

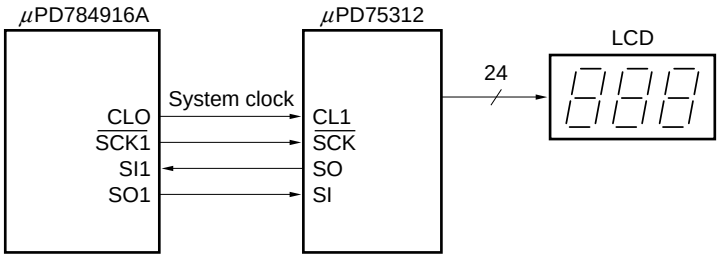
Figure 3-26. Block Diagram of Clock Output Circuit



Remark f_{CLK}: internal system clock

Caution Do not use the clock output function in the STOP mode. Clear ENCLO (CLOM.4) to 0 in the STOP mode.

Figure 3-27 Application Example of Clock Output Function



4. INTERNAL/EXTERNAL CONTROL FUNCTION

4.1 Interrupt Function

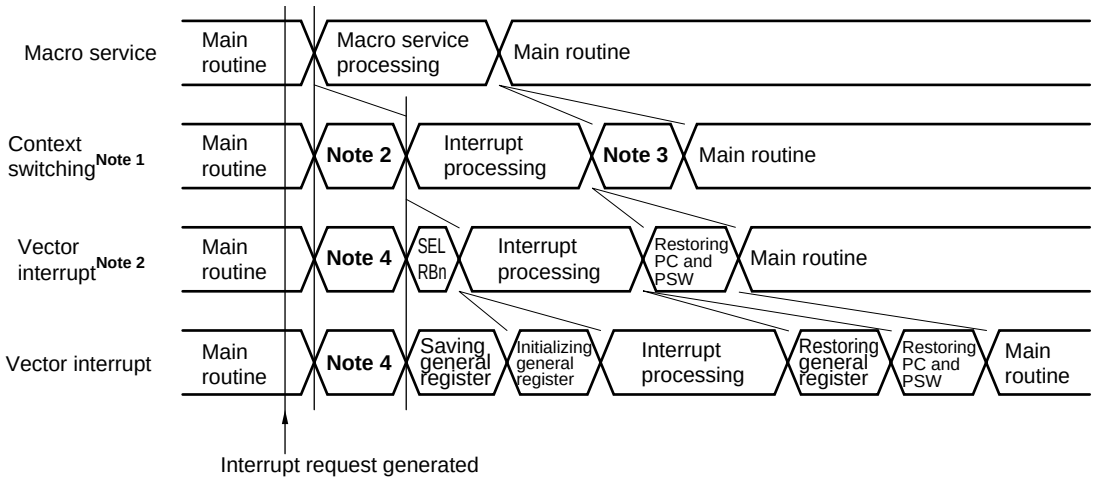
The μPD784916A has as many as 30 interrupt sources, including internal and external sources. For 26 sources, a high-speed interrupt processing mode such as context switching or macro service can be specified by software.

Table 4-1 lists the interrupt sources.

Table 4-1. Interrupt Sources

Interrupt Request Type	Priority	Interrupt Request Source		Interrupt Control Register Name	Macro Service	Context Switching	Macro Service Control Word Address	Vector Table Address
		Name	Trigger					
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	No	No	–	0000H
Non-maskable	–	NMI	NMI pin input edge	–			–	0002H
Maskable	0	INTP0	INTP0 pin input edge	PIC0	Yes	Yes	FE06H	0006H
	1	INTCPT3	EDVC output signal (CPT3 capture)	CPTIC3			FE08H	0008H
	2	INTCPT2	DFGIN pin input edge (CPT2 capture)	CPTIC2			FE0AH	000AH
	3	INTCR12	PBCTL input edge/EDVC output signal (CR12 capture)	CRIC12			FE0CH	000CH
	4	INTCR00	TM0-CR00 coincidence signal	CRIC00			FE0EH	000EH
	5	INTCLR1	CSYNCIN pin input edge	CLRIC1			FE10H	0010H
	6	INTCR10	TM1-CR10 coincidence signal	CRIC10			FE12H	0012H
	7	INTCR01	TM0-CR01 coincidence signal	CRIC01			FE14H	0014H
	8	INTCR02	TM0-CR02 coincidence signal	CRIC02			FE16H	0016H
	9	INTCR11	TM1-CR11 coincidence signal	CRIC11			FE18H	0018H
	10	INTCPT1	Pin input edge/EC output signal (CPT1 capture)	CPTIC1			FE1AH	001AH
	11	INTCR20	TM2-CR20 coincidence signal	CRIC20			FE1CH	001CH
	12	INTTB	Time base from FRC	TBIC			FE20H	0020H
	13	INTAD	A/D converter conversion end	ADIC			FE22H	0022H
	14	INTP2	INTP2 pin input edge	PIC2			FE24H	0024H
		INTCR40	TM4-CR40 coincidence signal	CRIC40				
	15	INTUDC	UDC-UDCC coincidence/UDC underflow	UDCIC			FE26H	0026H
	16	INTCR30	TM3-CR30 coincidence signal	CRIC30			FE28H	0028H
	17	INTCR50	TM5-CR50 coincidence signal	CRIC50			FE2AH	002AH
	18	INTCR13	TM1-CR13 coincidence signal	CRIC13			FE2CH	002CH
	19	INTCSI1	End of serial transfer (channel 1)	CSIIC1			FE2EH	002EH
	20	INTW	Overflow of watch timer	WIC			FE30H	0030H
	21	INTP1	INTP1 pin input edge	PIC1			FE34H	0034H
	22	INTP3	INTP3 pin input edge	PIC3			FE36H	0036H
	23	INTCSI2	End of serial transfer (channel 2)	CSIIC2			FE3AH	003AH
Operand error	–	–	Illegal operand of MOV STBC, #byte or LOCATION instruction	–	No	No	–	003CH
Software	–	–	Execution of BRK instruction	–			–	003EH
	–	–	Execution of BRKCS instruction	–		Yes	–	–

Figure 4-1. Differences in Operation Depending on Interrupt Processing Mode



Notes 1. When the register bank switching function is used and when initial values are set in advance to the registers

2. Selecting a register bank and saving PC and PSW by context switching

3. Restoring register bank, PC, and PSW by context switching

4. Saves PC and PSW to stack and loads vector address to PC

4.1.1 Vector interrupt

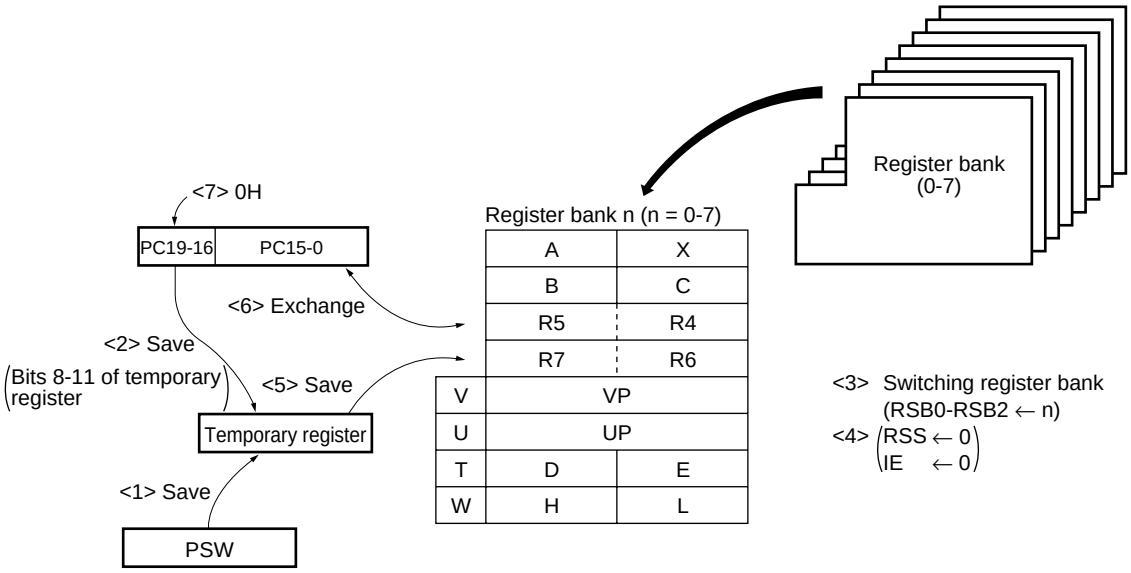
When an interrupt is acknowledged, an interrupt processing program is executed according to the data stored in the vector table area (the first address of the interrupt processing program created by the user).

Four levels of priorities can be specified by software for the vector interrupts of the μPD784916A.

4.1.2 Context switching

When an interrupt request is generated or when the BRKCS instruction is executed, a specific register bank is selected by hardware, and execution branches to a vector address set in advance in the register bank. At the same time, the current contents of the program counter (PC) and program status word (PSW) are saved to the registers in the register bank. Because the contents of PC and PSW are not saved to the stack area, execution can be branched to an interrupt processing routine more quickly than the vector interrupt.

Figure 4-2. Context Switching Operation When Interrupt Request Is Generated



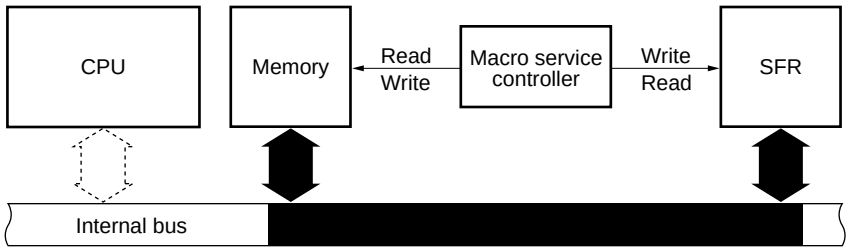
4.1.3 Macro service

The macro service is a function to transfer data between the memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR and directly transfers the data.

Because the status of the CPU is not saved or restored, data can be transferred more quickly than context switching.

The processing that can be executed with the macro service is described below.

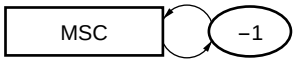
Figure 4-3. Macro Service



(1) Counter mode

In this mode, the value of the macro service counter (MSC) is decremented when an interrupt occurs. This mode can be used to execute the division operation of an interrupt or count the number of times an interrupt has occurred.

When the value of the macro service counter has been decremented to 0, a vector interrupt occurs.



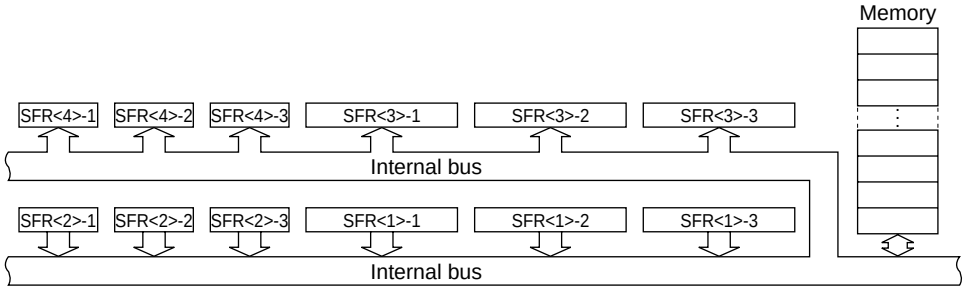
(2) Compound data transfer mode

When an interrupt occurs, data are simultaneously transferred from an 8-bit SFR to memory, a 16-bit SFR to memory (word), memory (byte) to an 8-bit SFR, and memory (word) to a 16-bit SFR (3 points MAX. for each transfer).

This mode can also be used to exchange data, instead of transferring data.

This mode can be used for automatic transfer/reception by the serial interface or automatic updating of data/timing by the serial output port.

When the value of the macro service counter reaches to 0, a vector interrupt occurs.



(3) Macro service type A

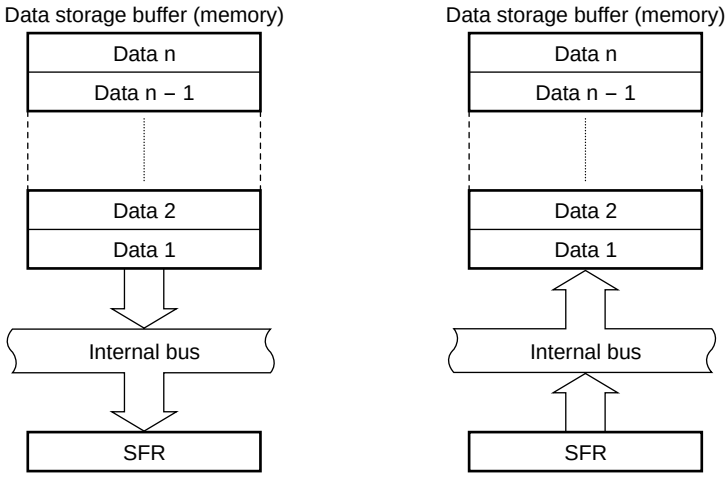
When an interrupt occurs, data is transferred from an 8-/16-bit SFR to memory (byte/word) or from memory (byte/word) to an 8-/16-bit SFR.

Data is transferred the number of times set in advance by the macro service counter.

This mode can be used to store the result of A/D conversion or for automatic transfer (or reception) by the serial interface.

Because transfer data is stored at an address FE00H to FEFFH, if only a small quantity of data is to be transferred, the data can be transferred at high speeds.

When the value of the macro service counter is decremented to 0, a vector interrupt occurs.

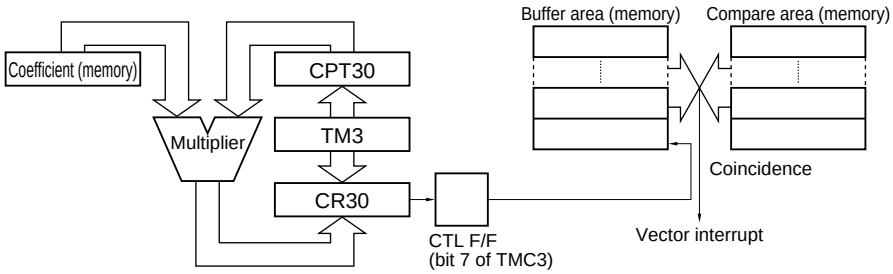


(4) Data pattern identification mode (VISS detection mode)

This mode of macro service is for detection of the VISS signal and is used in combination with a pulse width detection circuit.

When an interrupt occurs, the content of bit 7 of an SFR (usually, TMC3) specified by SFR pointer 1 is shifted into the buffer area. At the same time, the data in the buffer area is compared with the data in the compare area. If the two data coincide, an interrupt request is generated. When the value of the macro service counter is decremented to 0, a vector interrupt occurs.

It can be specified by option that the value of an SFR (usually, CPT30) specified by SFR pointer 2 be multiplied by a coefficient and the result of this multiplication be stored to an SFR (usually, CR30) specified by SFR pointer 3 (this operation is to automatically update an identification threshold value when the tape speed fluctuates).

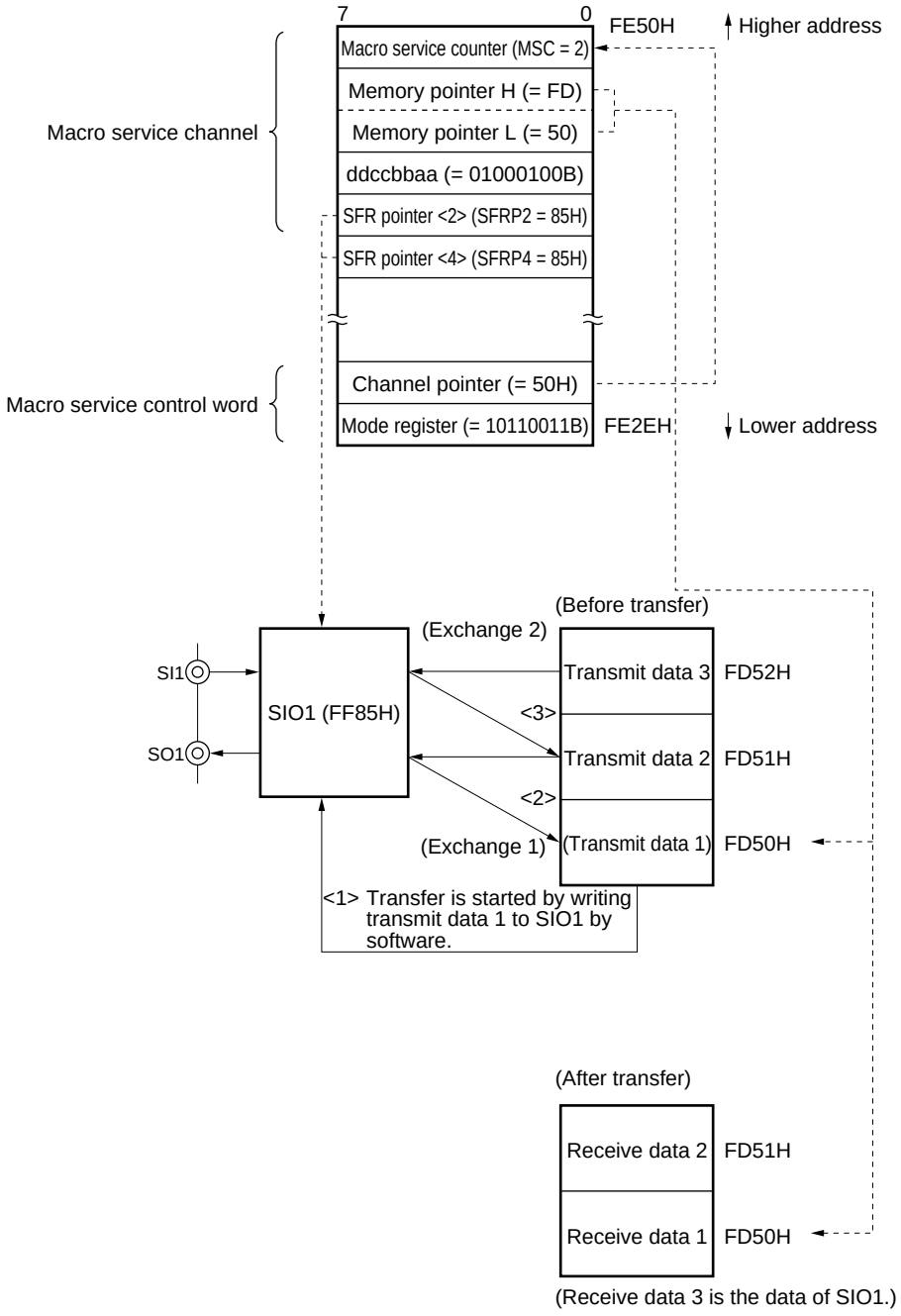


4.1.4 Application example of macro service

(1) Automatic transfer/reception of serial interface

Automatic transfer/reception of 3-byte data by serial interface channel 1

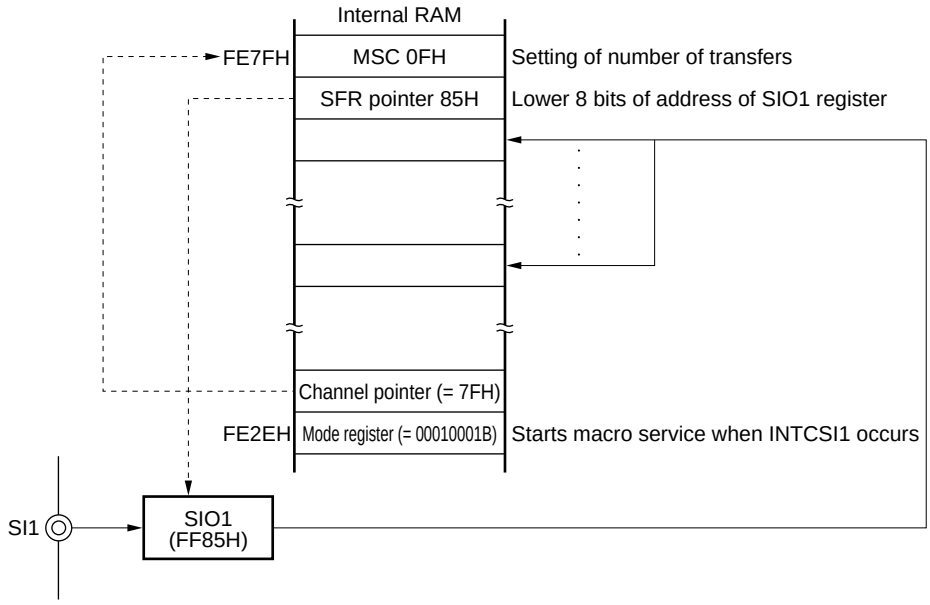
Setting of macro service register: compound data transfer mode (exchange mode)



(2) Reception operation of serial interface

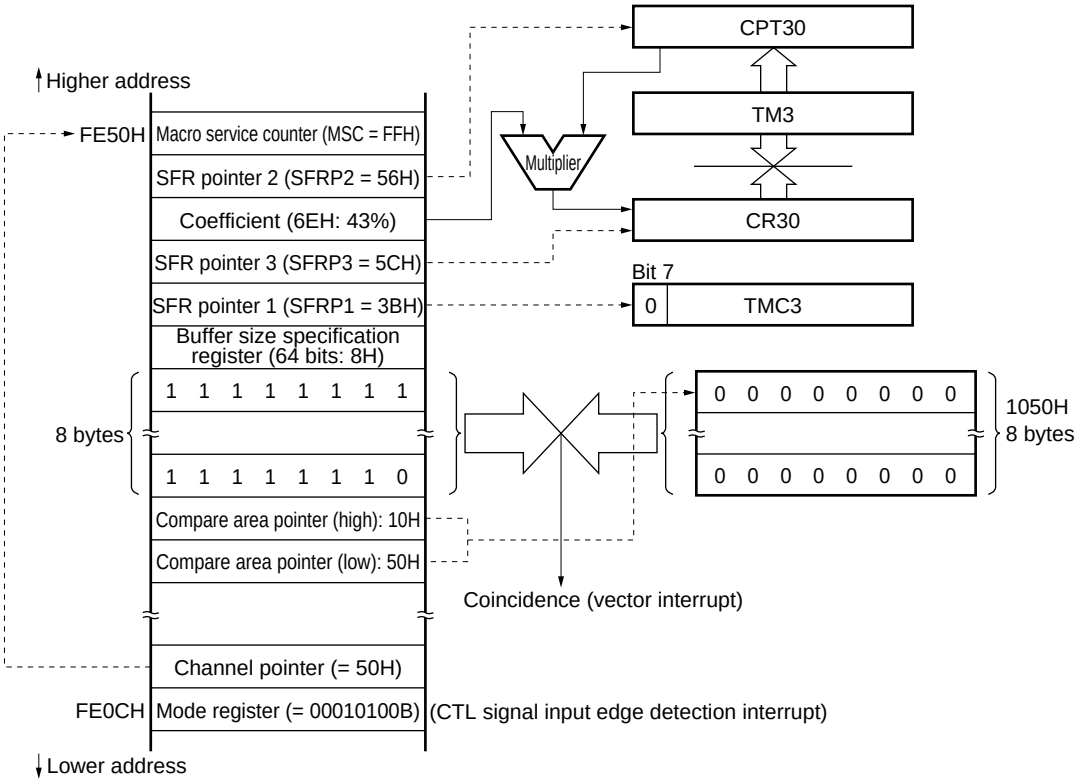
Transfer of receive data by serial interface channel 1 (16 bytes)

Setting of macro service mode register: macro service type A (1-byte transfer from SFR to memory)



(3) VISS detection operation

Setting of macro service mode register: data pattern identification mode (with multiplication, 8-byte comparison)



4.2 Standby Function

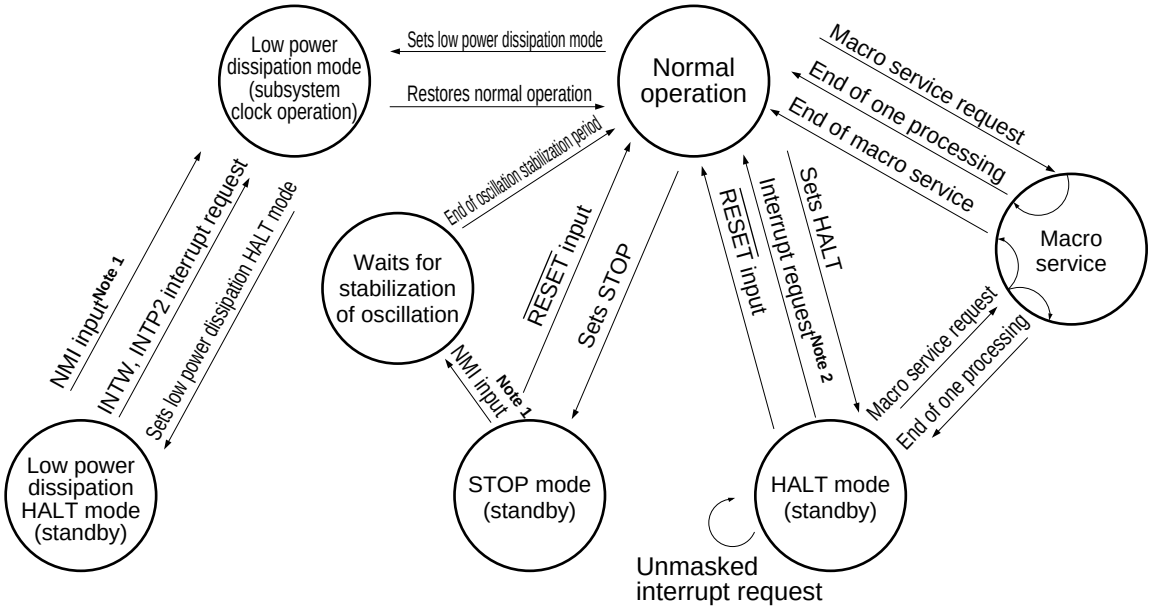
The standby function serves to reduce the power dissipation of the chip and is used in the following modes:

Mode	Function
HALT mode	Stops operating clock of CPU. Reduces average power dissipation when used in combination with normal mode for intermittent operation
STOP mode	Stops oscillator. Stops all internal operations of chip to minimize current dissipation to leakage current only
Low power dissipation mode	Stops main system clock with subsystem clock used as system clock. CPU can operate with subsystem clock to reduce power dissipation
Low power dissipation HALT mode	Standby function in low power dissipation mode. Stops operating clock of CPU. Reduces power dissipation of overall system

These modes are programmable.

The macro service can be started in the HALT mode.

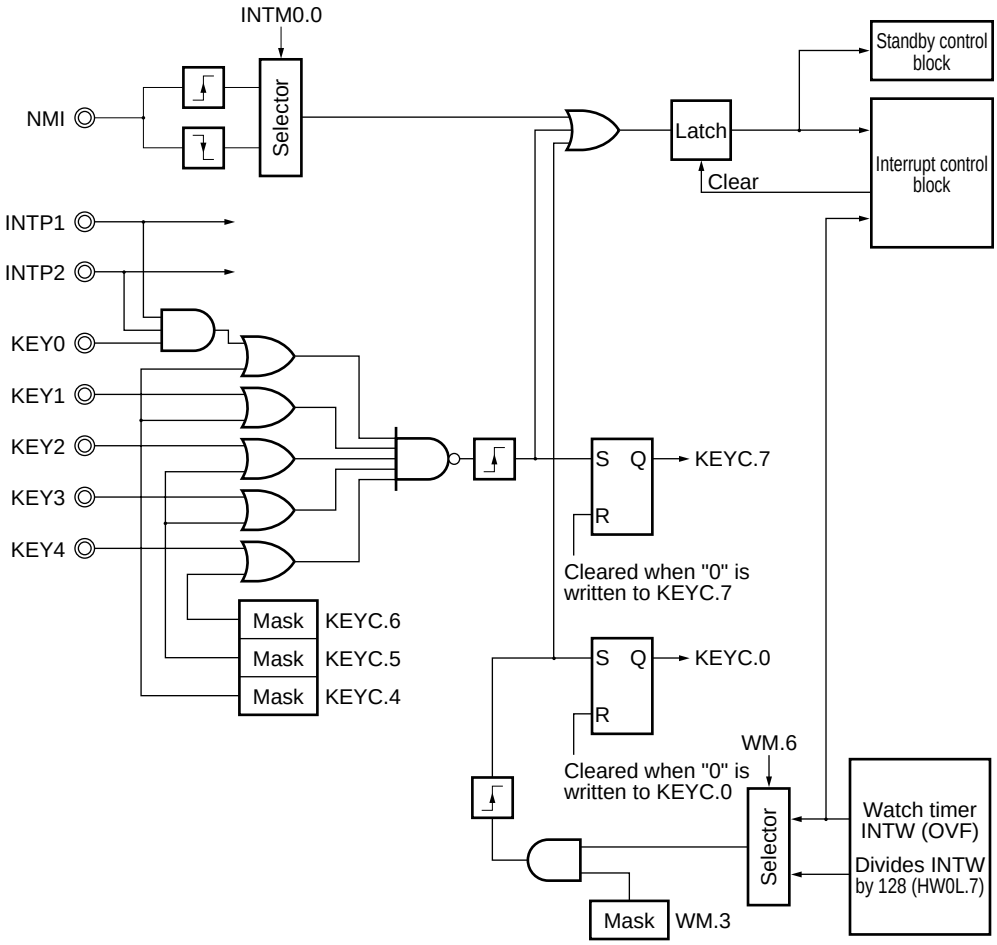
Figure 4-4. Status Transition of Standby Function



Notes 1. NMI input means starting NMI by NMI pin input, watch interrupt, or key interrupt input.

2. Unmasked interrupt request

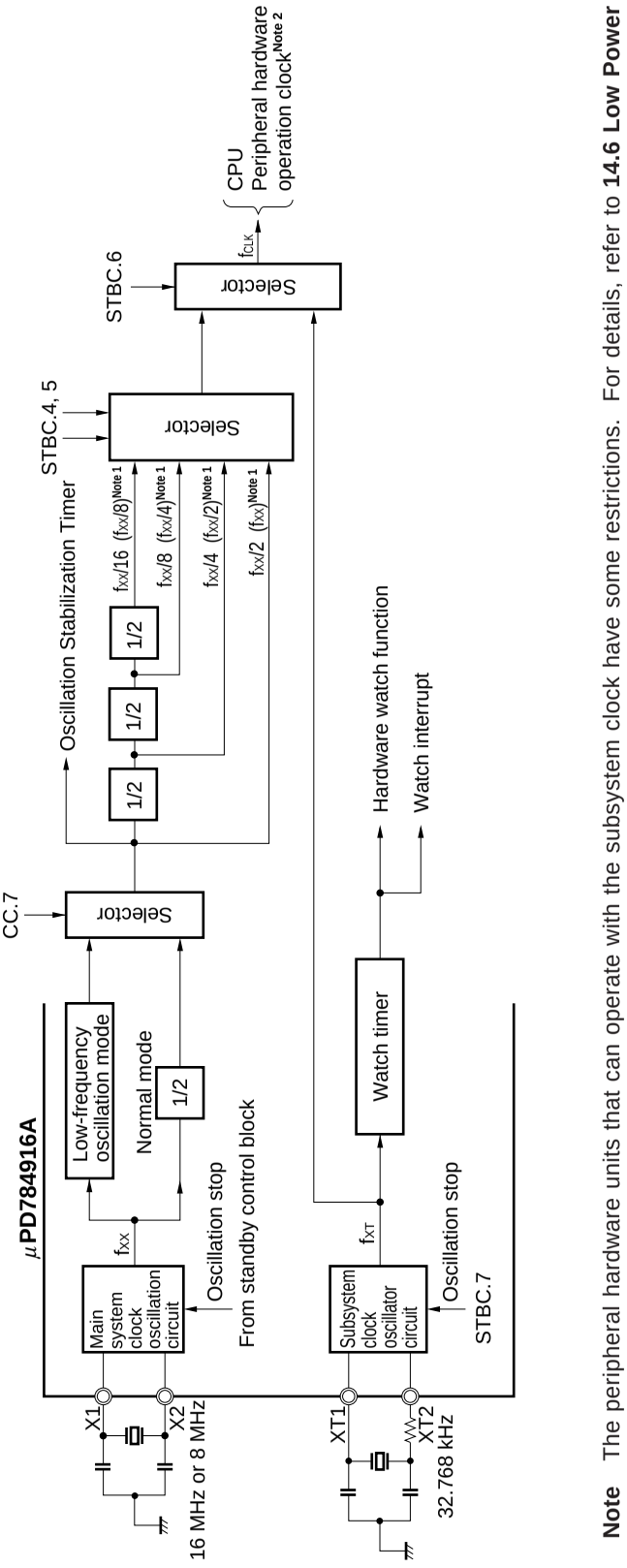
Figure 4-5. Relations among NMI, Watch Interrupt, and Key Interrupt When STOP Mode Is Released



4.3 Clock Generator Circuit

The clock generator circuit generates and controls the internal system clock (CLK) to be supplied to the CPU and peripheral circuits. Figure 4-6 shows the configuration of this circuit.

★ **Figure 4-6. Block Diagram of Clock Generator Circuit**



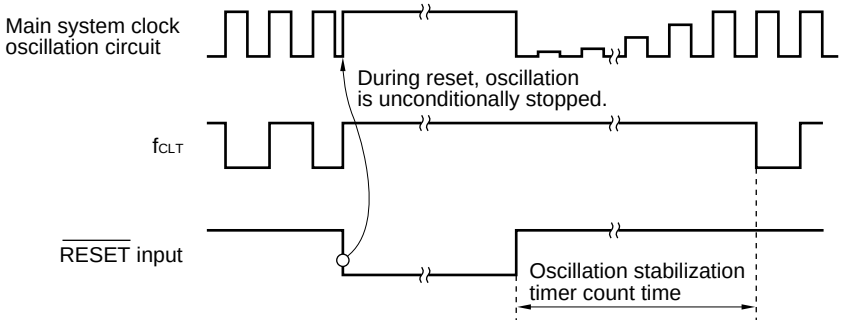
Note The peripheral hardware units that can operate with the subsystem clock have some restrictions. For details, refer to **14.6 Low Power Dissipation Mode** in **μPD784915 Subseries User's Manual**.

4.4 Reset Function

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized (reset status). During the reset period, oscillation of the system clock is unconditionally stopped, so that the current dissipation of the overall system can be reduced.

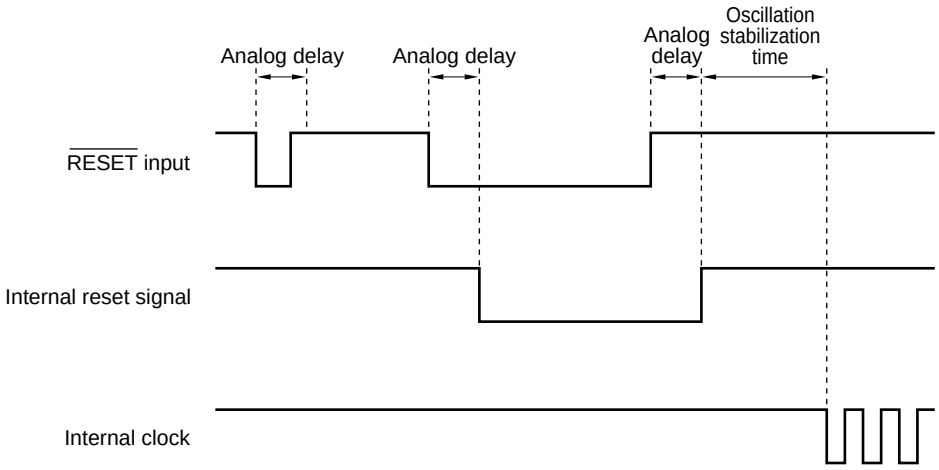
When the $\overline{\text{RESET}}$ pin goes high, the reset status is cleared. After the count time of the oscillation stabilization timer (32.8 ms at 16 MHz or 65.6 ms at 8 MHz) has elapsed, the contents of the reset vector table are set to the program counter (PC), and execution branches to the address set to the PC, and the program is executed starting from the branch destination address. Therefore, execution can be reset and started from any address.

Figure 4-7. Oscillation of Main System Clock during Reset Period



The $\overline{\text{RESET}}$ pin is provided with an analog delay noise rejecter circuit to prevent malfunctioning due to noise.

Figure 4-8. Accepting Reset Signal



5. INSTRUCTION SETS

(1) 8-bit instructions (( ): combination realized by describing A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

2nd Operand / 1st Operand	# byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+]	[WHL–]	n	None Note 2
A	(MOV) ADD Note 1	(MOV) (XCH) (ADD) Note 1	MOV XCH (ADD) Note 1	(MOV) Note 6 (XCH) Note 6 (ADD) Notes 1,6	MOV (XCH) (ADD) Note 1	(MOV) (XCH) ADD Note 1	MOV XCH ADD Note 1	MOV	(MOV) (XCH) (ADD) Note 1	(MOV) (XCH) (ADD) Note 1		
r	MOV ADD Note 1	(MOV) (XCH) (ADD) Note 1	MOV XCH ADD Note 1	MOV XCH ADD Note 1	MOV XCH ADD Note 1	MOV XCH					ROR Note 3	MULU DIVUW INC DEC
saddr	MOV ADD Note 1	(MOV) Note 6 (ADD) Note 1	MOV ADD Note 1	MOV XCH ADD Note 1								INC DEC DBNZ
sfr	MOV ADD Note 1	MOV (ADD) Note 1	MOV ADD Note 1									PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD Note 1	MOV									
mem [saddrp] [%saddrg]		MOV ADD Note 1										
mem3												ROR4 ROL4
r3 PSWL PSWH	MOV	MOV										
B, C												DBNZ
STBC, WDM	MOV	(MOV)										
[TDE+]		(ADD) Note 1 MOVM Note 4							MOVBK Note 5			
[TDE–]		(MOV) (ADD) Note 1 MOVM Note 4								MOVBK Note 5		

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2. Either the second operand is not used, or the second operation is not an operand address.

3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.

4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.

5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.

6. If saddr2 instead of saddr is used in this combination, the code length of some instructions is short.

(2) 16-bit instructions (( ): combination realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

2nd Operand / 1st Operand	# word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None Note 2
AX	(MOVM) ADDW Note 1	(MOVW) (XCHW) (ADDW) Note 1	(MOVW) (XCHW) (ADDW) Note 1	(MOVW) Note 3 (XCHW) Note 3 (ADDW) Notes 1, 3	MOVW (XCHW) (ADDW) Note 1	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW Note 1	(MOVW) (XCHW) (ADDW) Note 1	MOVW XCHW ADDW Note 1	MOVW XCHW ADDW Note 1	MOVW XCHW ADDW Note 1	MOVW				SHRW SHLW	MULW Note 4 INCW DECW
saddrp	MOVW ADDW Note 1	(MOVW) Note 3 (ADDW) Note 1	MOVW ADDW Note 1	MOVW XCHW ADDW Note 1							INCW DECW
sfrp	MOVW ADDW Note 1	MOVW (ADDW) Note 1	MOVW ADDW Note 1								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. SUBW and CMPW are the same as ADDW.

2. Either the second operand is not used, or the second operation is not an operand address.

3. If saddr2 instead of saddr is used in this combination, the code length of some instructions is short.

4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions (( ): combination realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

2nd Operand / 1st Operand	# imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used, or the second operation is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

2nd Operand / 1st Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit iaddr16.bit !addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used, or the second operation is not an operand address.

(5) Call/return and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Operand of instruction address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLT	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = 25°C)

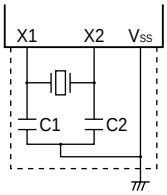
Parameter	Symbol	Condition	Ratings	Unit
★ Supply voltage	V_{DD}	$\|V_{DD} - AV_{DD1}\| \le 0.5$ V	–0.5 to +7.0	V
	AV_{DD1}	$\|V_{DD} - AV_{DD2}\| \le 0.5$ V	–0.5 to +7.0	V
	AV_{DD2}	$\|AV_{DD1} - AV_{DD2}\| \le 0.5$ V	–0.5 to +7.0	V
	AV_{SS1}		–0.5 to +0.5	V
	AV_{SS2}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Analog input voltage (ANI0-ANI11)	V_{IAN}	$V_{DD} \ge AV_{DD2}$	–0.5 to AV_{DD2} + 0.5	V
		$V_{DD} < AV_{DD2}$	–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	Pin 1	15	mA
		Total of all pins	100	mA
High-level output current	I_{OH}	Pin 1	–10	mA
		Total of all pins	–50	mA
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings therefore specify the values exceeding which the product may be physically damaged. Never exceed these values when using the product.

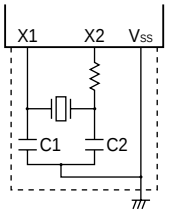
Operating Conditions

Clock Frequency	Operating Temperature (T_A)	Operating Conditions	Supply Voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 16 MHz	–10 to +70°C	All functions	+4.5 to +5.5 V
		CPU function only	+4.0 to +5.5 V
32 kHz ≤ f_{XT} ≤ 35 kHz		Subclock operation (CPU, watch, and port functions only)	+2.7 to +5.5 V

Oscillator Characteristics (main clock) (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Crystal oscillator		Oscillation frequency (f_{XX})	4	16	MHz

Oscillator Characteristics (subclock) (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Crystal oscillator		Oscillation frequency (f_{XT})	32	35	kHz

Caution When using the main system clock and subsystem clock oscillation circuits, wire the portion enclosed by the broken line in the above figures as follows to avoid the adverse influence of wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring in the neighborhood of a signal line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit to the same potential as V_{SS}. Do not ground the capacitor to a ground pattern to which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

Exercise particular care in using the subsystem clock oscillation circuit because the amplification factor of this circuit is kept low to reduce the power dissipation.

DC Characteristics (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ Low-level input voltage	V_{IL1}	Pins other than those listed in Notes 1 and 4 below		0		0.3 V_{DD}	V
	V_{IL2}	Pins listed in Notes 1 and 4 below		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
High-level input voltage	V_{IH1}	Pins other than those listed in Note 1 below		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Pins listed in Note 1 below		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 5.0 mA (pins in Note 2)				0.6	V
	V_{OL2}	I_{OL} = 2.0 mA				0.45	V
	V_{OL3}	I_{OL} = 100 μA				0.25	V
High-level output voltage	V_{OH1}	I_{OH} = –1.0 mA		V_{DD} – 1.0			V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 0.4			V
Input leakage current	I_{LI}	0 ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode	f_{XX} = 16 MHz f_{XX} = 8 MHz (low-frequency oscillation mode) Internally, 8-MHz main system clock operation		30	50	mA
			f_{XT} = 32.768 kHz Subclock operation (CPU, watch, port) V_{DD} = 2.7 V		50	80	μA
	I_{DD2}	HALT mode	f_{XX} = 16 MHz f_{XX} = 8 MHz (low-frequency oscillation mode) Internally, 8-MHz main clock operation		10	25	mA
			f_{XT} = 32.768 MHz Subclock operation (CPU, watch, port) V_{DD} = 2.7 V		25	50	μA
Data hold voltage	V_{DDDR}	STOP mode		2.5			V
Data hold current[Note 3]	I_{DDDR}	STOP mode V_{DDDR} = 5.0 V	Subclock oscillates		18	50	μA
★		STOP mode V_{DDDR} = 2.7 V	Subclock oscillates		2.5	10	μA
		STOP mode V_{DDDR} = 2.5 V	Subclock stops		0.2	7.0	μA
Pull-up resistor	R_L	V_I = 0 V		25	55	110	kΩ

Notes 1. $\overline{\text{RESET}}$, IC, NMI, INTP0-INTP2, P61/$\overline{\text{SCK1}}$/BUZ, P63/SI1, $\overline{\text{SCK2}}$, SI2/BUSY, P65/HWIN, P91/KEY0-P95/KEY4

2. P46, P47

3. In the STOP mode in which the subclock oscillation is stopped, disconnect the feedback resistor, and connect the XT1 pin to V_{DD}.

4. P40 to P47, P50 to P57

AC Characteristics

CPU and peripheral circuit operation clock (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition		TYP.	Unit
CPU operation clock cycle time	t_{CLK}	f_{XX} = 16 MHz	V_{DD} = AV_{DD} = 4.0 to 5.5 V CPU Function only	125	ns
		f_{XX} = 16 MHz			
		f_{XX} = 8 MHz	low-frequency oscillation mode (Bit 7 of CC = 1)		
Peripheral operation clock cycle time	t_{CLK1}	f_{XX} = 16 MHz		125	ns
		f_{XX} = 8MHz	low-frequency oscillation mode (Bit 7 of CC = 1)		

Serial interface

(1) SIOn: n = 1 or 2 (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	f_{CLK1}/8	1.0		μs
			f_{CLK1}/16	2.0		μs
			f_{CLK1}/32	4.0		μs
			f_{CLK1}/64	8.0		μs
			f_{CLK1}/128	16		μs
			f_{CLK1}/256	32		μs
Serial clock high- and low-level widths	t_{WSKH}	Input	External clock	420		ns
	t_{WSKL}	Output	Internal clock	t_{CYSK}/2 – 50		ns
SIn setup time (vs. $\overline{SCKn}$ ↑)	t_{SSSK}			100		ns
SIn hold time (vs. $\overline{SCKn}$ ↑)	t_{HSSK}			400		ns
SOn output delay time (vs. $\overline{SCKn}$ ↓)	t_{DSSK}			0	300	ns

Remarks 1. f_{CLK1}: operating clock of peripheral circuit (8 MHz)

2. n = 1 or 2

(2) SIO2 only (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{SCK2}$(8) ↑→STBR ↑	t_{DSTRB}		t_{WSKH}	t_{CYSK}	
Strobe high-level width	t_{WSTRB}		t_{CYSK} – 30	t_{CYSK} + 30	ns
BUSY setup time (vs. BUSY detection timing)	t_{SBUSY}		100		ns
BUSY hold time (vs. BUSY detection timing)	t_{HBUSY}		100		ns
BUSY inactive →$\overline{SCK2}$(1) ↓	t_{LBUSY}			t_{CYSK} + t_{WSKH}	

Remarks 1. The value in ( ) following $\overline{SCK2}$ indicates the number of $\overline{SCK2}$.

2. BUSY is detected after the time (n+2) x t_{CYSK} (n = 0, 1, and so on) has elapsed relative to $\overline{SCK2}$ (8) ↑.

3. BUSY inactive →$\overline{SCK2}$ (1) ↓ is the value when data write to SIO2 has been completed.

Other operations (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter		Symbol	Condition		MIN.	MAX.	Unit
Timer input signal low-level width		t_{WCTL}	When DFGIN, CFGIN, DPGIN, REEL0IN, or REEL1IN logic level is input		t_{CLK1}		ns
Timer input signal high-level width		t_{WCTH}	When DFGIN, CFGIN, DPGIN, REEL0IN, or REEL1IN logic level is input		t_{CLK1}		ns
Timer input signal valid edge input cycle		t_{PERIN}	When DFGIN, CFGIN, or DPGIN is input		2		μs
CSYNCIN low-level width		t_{WCR1L}	When digital noise elimination circuit is not used		$8t_{CLK1}$		ns
			When digital noise elimination circuit is used (Bit 4 of INTM2 = 0)		$108t_{CLK1}$		ns
			When digital noise elimination circuit is used (Bit 4 of INTM2 = 1)		$180t_{CLK1}$		ns
CSYNCIN high-level width		t_{WCR1H}	When digital noise elimination circuit is not used		$8t_{CLK1}$		ns
			When digital noise elimination circuit is used (Bit 4 of INTM2 = 0)		$108t_{CLK1}$		ns
			When digital noise elimination circuit is used (Bit 4 of INTM2 = 1)		$180t_{CLK1}$		ns
Digital noise elimination circuit	Eliminated pulse width	t_{WSEP}	Bit 4 of INTM2 = 0			$104t_{CLK1}$	ns
			Bit 4 of INTM2 = 1			$176t_{CLK1}$	ns
	Passed pulse width		Bit 4 of INTM2 = 0		$108t_{CLK1}$		ns
			Bit 4 of INTM2 = 1		$180t_{CLK1}$		ns
NMI low-level width		t_{WNIL}	V_{DD} = AV_{DD} = 2.7 to 5.5 V		10		μs
NMI high-level width		t_{WNIH}	V_{DD} = AV_{DD} = 2.7 to 5.5 V		10		μs
INTP0, INTP3 low-level widths		t_{WIPL0}			$2t_{CLK1}$		ns
INTP0, INTP3 high-level widths		t_{WIPH0}			$2t_{CLK1}$		ns
INTP1, KEY0-KEY4 low-level widths		t_{WIPL1}	Mode other than STOP mode		$2t_{CLK1}$		ns
			In STOP mode, for releasing STOP mode		10		μs
INTP1, KEY0-KEY4 high-level widths		t_{WIPH1}	Mode other than STOP mode		$2t_{CLK1}$		ns
			In STOP mode, for releasing STOP mode		10		μs
INTP2 low-level width		t_{WIPL2}	In normal mode, with main clock	Sampling = f_{CLK}	$2t_{CLK1}$		ns
				Sampling = f_{CLK}/128	32 Note		μs
			Normal mode, with subclock	Sampling = f_{CLK}	61		μs
				Sampling = f_{CLK}/128	7.9 Note		ms
			In STOP mode, for releasing STOP mode		10		μs
INTP2 high-level width		t_{WIPH2}	In normal mode, with main clock	Sampling = f_{CLK}	$2t_{CLK1}$		ns
				Sampling = f_{CLK}/128	32 Note		μs
			Normal mode, with subclock	Sampling = f_{CLK}	61		μs
				Sampling = f_{CLK}/128	7.9 Note		ms
			In STOP mode, for releasing STOP mode		10		μs
$\overline{\text{RESET}}$ low-level width		t_{WRSL}			10		μs

Note If a high or low level is successively input two times during the sampling period, a high or low level is detected.

Remark t_{CKL1}: operating clock cycle time of peripheral circuit (125 ns)

Clock output operation (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CLO cycle time	t_{CYCL}		250	2000	ns
CLO low-level width	t_{CLL}	$t_{CYCL}/2 \pm 50$	75	1050	ns
CLO high-level width	t_{CLH}	$t_{CYCL}/2 \pm 50$	75	1050	ns
CLO rise time	t_{CLR}			50	ns
CLO fall time	t_{CLF}			50	ns

Data hold characteristics (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 2.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}	Special pins (pins in **Note**)	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

Note $\overline{\text{RESET}}$, IC, NMI, INTP0-INTP2, P61/$\overline{\text{SCK1}}$/BUZ, P63/SI1, $\overline{\text{SCK2}}$, SI2/BUSY, P65/HWIN P91/KEY0-P95/KEY4

Watch function (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Subclock oscillation hold voltage	V_{DDXT}		2.7		V
Hardware watch function operating voltage	V_{DDW}		2.7		V

Subclock oscillation stop detection flag (T_A = –10 to +70°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Oscillation stop detection width	t_{OSCF}		45		μs

A/D converter characteristics (T_A = –10 to +70°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error		AV_{REF} = V_{DD}			2.0	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	Bit 4 of ADM = 0	160t_{CLK1}			μs
		Bit 4 of ADM = 1	80t_{CLK1}			μs
Sampling time	t_{SAMP}	Bit 4 of ADM = 0	32t_{CLK1}			μs
		Bit 4 of ADM = 1	16t_{CLK1}			μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Analog input impedance	Z_{AN}			1000		MΩ
AV_{REF} current	AI_{REF}			0.4	1.2	mA

VREF amplifier (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}		2.35	2.50	2.65	V
Charge current	I_{CHG}	Sets AMPM0.0 to 1 (pins in **Note**)	300			μA

Note RECCTL+, RECCTL–, CFGIN, CFGCPIN, DFGIN, DPGIN, CSYNCIN, REEL0IN, REEL1IN

CTL amplifier (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

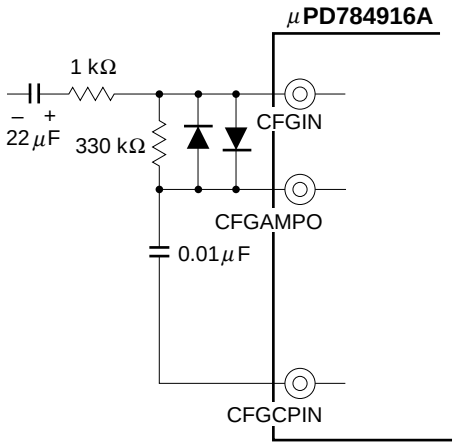
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CTL+, – input resistance	R_{ICTL}		2	5	10	kΩ
Feedback resistance	R_{FCTL}		20	50	100	kΩ
Bias resistance	R_{BCTL}		20	50	100	kΩ
Minimum voltage gain	G_{CTLMIN}		17	20	22	dB
Maximum voltage gain	G_{CTLMAX}		71	75		dB
★ Gain selecting step	S_{GAIN}			1.77		dB
★ In-phase elimination ratio	CMR	DC, voltage gain: 20 dB		30		dB
High comparator set voltage of waveform shaping	$V_{PBCTLHS}$		V_{REF} + 0.47	V_{REF} + 0.50	V_{REF} + 0.53	V
High comparator reset voltage of waveform shaping	$V_{PBCTLHR}$		V_{REF} + 0.27	V_{REF} + 0.30	V_{REF} + 0.33	V
Low comparator set voltage of waveform shaping	$V_{PBCTLLS}$		V_{REF} – 0.53	V_{REF} – 0.50	V_{REF} – 0.47	V
Low comparator reset voltage of waveform shaping	$V_{PBCTLLR}$		V_{REF} – 0.33	V_{REF} – 0.30	V_{REF} – 0.27	V
Waveform shaping comparator Schmit width	V_{PBSH}		150	200	250	mV
High comparator voltage of CTL flag S	V_{FSH}		V_{REF} + 1.00	V_{REF} + 1.05	V_{REF} + 1.10	V
Low comparator voltage of CLT flag S	V_{FSL}		V_{REF} – 1.10	V_{REF} – 1.05	V_{REF} – 1.00	V
High comparator voltage of CTL flag L	V_{FLH}		V_{REF} + 1.40	V_{REF} + 1.45	V_{REF} + 1.50	V
Low comparator voltage of CTL flag L	V_{FLL}		V_{REF} – 1.50	V_{REF} – 1.45	V_{REF} – 1.40	V

CFG amplifier (AC coupling) (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage gain 1	G_{CFG1}	f_i = 2 kHz, open loop	50			dB
Voltage gain 2	G_{CFG2}	f_i = 30 kHz, open loop	34			dB
CFGAMPO High-level output current	I_{OHCFG}	DC	–1			mA
★ CFGAMPO Low-level output current	I_{OLCFG}	DC	0.1			mA
High comparator voltage	V_{CFGH}		V_{REF} + 0.09	V_{REF} + 0.12	V_{REF} + 0.15	V
Low comparator voltage	V_{CFGL}		V_{REF} – 0.15	V_{REF} – 0.12	V_{REF} – 0.09	V
Duty accuracy	P_{DUTY}	**Note**	49.7	50.0	50.3	%

Note The conditions include the following circuit and input signal.

Input signal : Sine wave input (5 mV_{p-p})
f_i = 1 kHz
Voltage gain: 50 dB



DFG amplifier (AC coupling) (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage gain	G_{DFG}	f_i = 900 Hz, open loop	50			dB
Feedback resistance	R_{FDFG}		160	400	640	kΩ
Input protection resistance	R_{IDFG}			150		Ω
High comparator voltage	V_{DFGH}		V_{REF} + 0.07	V_{REF} + 0.10	V_{REF} + 0.14	V
Low comparator voltage	V_{DFGL}		V_{REF} – 0.14	V_{REF} – 0.10	V_{REF} – 0.07	V

Caution Set the input resistance connected to the DFGIN pin to 16 kΩ or below. Connecting a resistor exceeding that value may cause the DFG amp to oscillate.

DPG comparator (AC coupling) (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IDPG}		20	50	100	kΩ
High comparator voltage	V_{DPGH}		V_{REF} + 0.02	V_{REF} + 0.05	V_{REF} + 0.08	V
Low comparator voltage	V_{DPGL}		V_{REF} – 0.08	V_{REF} – 0.05	V_{REF} – 0.02	V

Ternary separation circuit (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IPFG}		20	50	100	kΩ
High comparator voltage	V_{PFGH}		V_{REF} + 0.5	V_{REF} + 0.7	V_{REF} + 0.9	V
Low comparator voltage	V_{PFGL}		V_{REF} – 1.4	V_{REF} – 1.2	V_{REF} – 1.0	V

CSYNC comparator (AC coupling) (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{ICSYN}		20	50	100	kΩ
High comparator voltage	V_{CSYNH}		V_{REF} + 0.07	V_{REF} + 0.10	V_{REF} + 0.13	V
Low comparator voltage	V_{CSYNL}		V_{REF} – 0.13	V_{REF} – 0.10	V_{REF} – 0.07	V

Reel FG comparator (AC coupling) (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

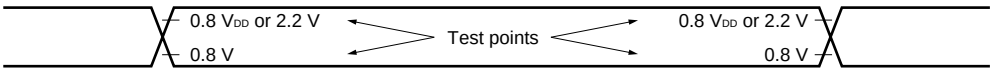
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IRLFG}		20	50	100	kΩ
High comparator voltage	V_{RLFGH}		V_{REF} + 0.02	V_{REF} + 0.05	V_{REF} + 0.08	V
Low comparator voltage	V_{RLFGL}		V_{REF} – 0.08	V_{REF} – 0.05	V_{REF} – 0.02	V

RECCTL driver (T_A = 25°C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

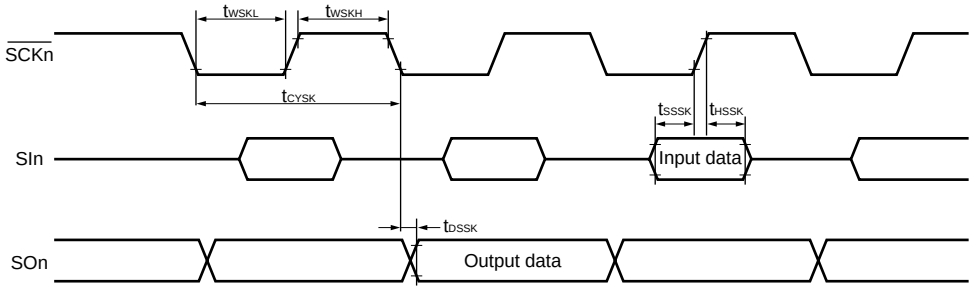
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RECCTL+, – high-level output voltage	V_{OHREC}	I_{OH} = –4 mA	V_{DD} – 0.8			V
RECCTL+, – low-level output voltage	V_{OLREC}	I_{OL} = 4 mA			0.8	V
CTLDLY internal resistance	R_{CTL}		40	70	140	kΩ
CTLDLY charge current	I_{OHCTL}	Use of internal resistor	–3			mA
CTLDLY discharge current	I_{OLCTL}		–3			mA

Timing waveform

AC timing test point

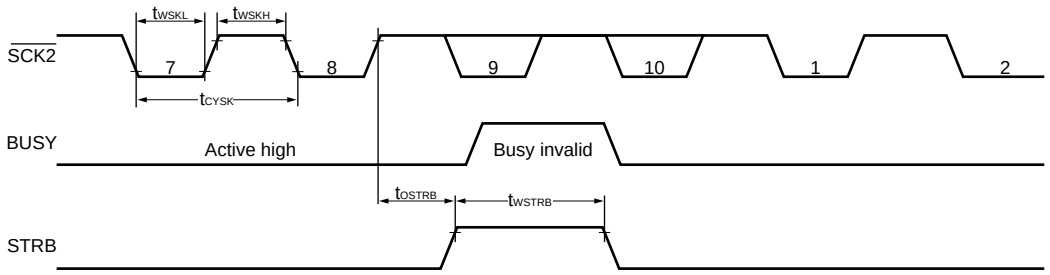


Serial transfer timing (SIOn: n = 1 or 2)

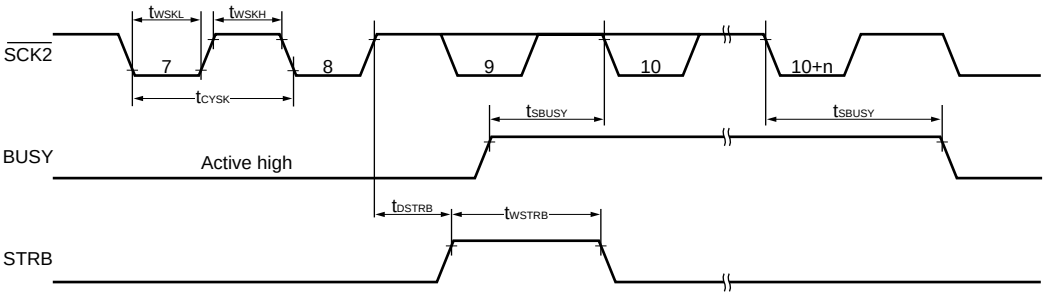


Serial transfer timing (SIO2 only)

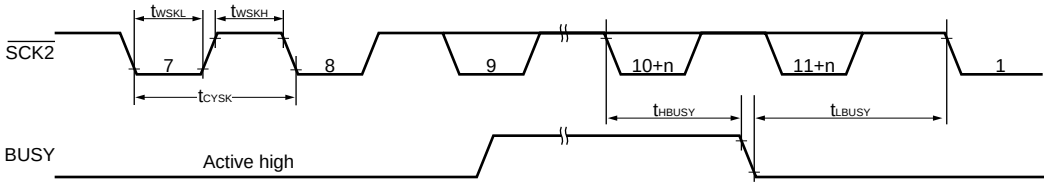
No busy processing



Continuation of busy processing



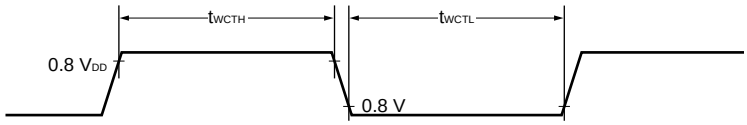
End of busy processing



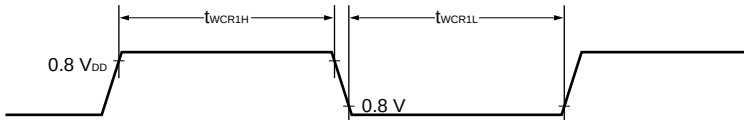
Caution When an external clock is selected as the serial clock, do not use the busy control or strobe control.

Super timer unit input timing

When DFGIN, CFGIN, DPGIN, REEL0IN, or REEL1IN logic level is input

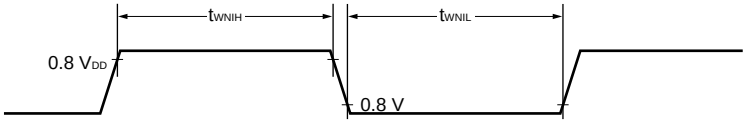


When CSYNCIN logic level is input

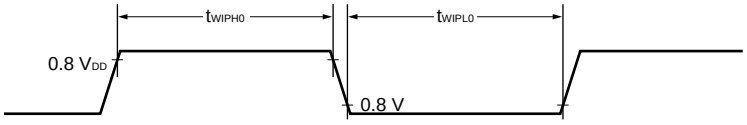


Interrupt input timing

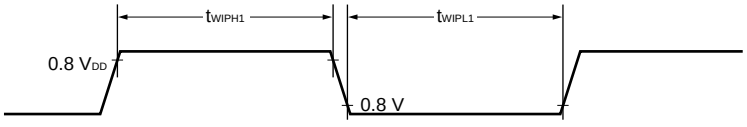
NMI



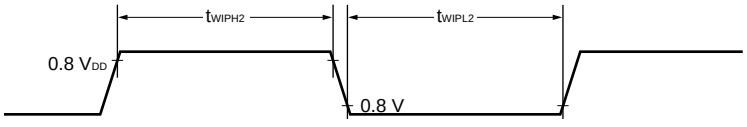
INTP0, INTP3



INTP1, KEY0-KEY4

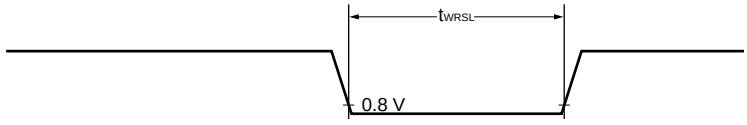


INTP2

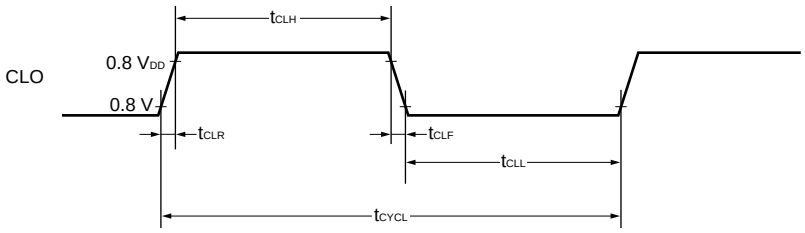


Reset input timing

$\overline{\text{RESET}}$

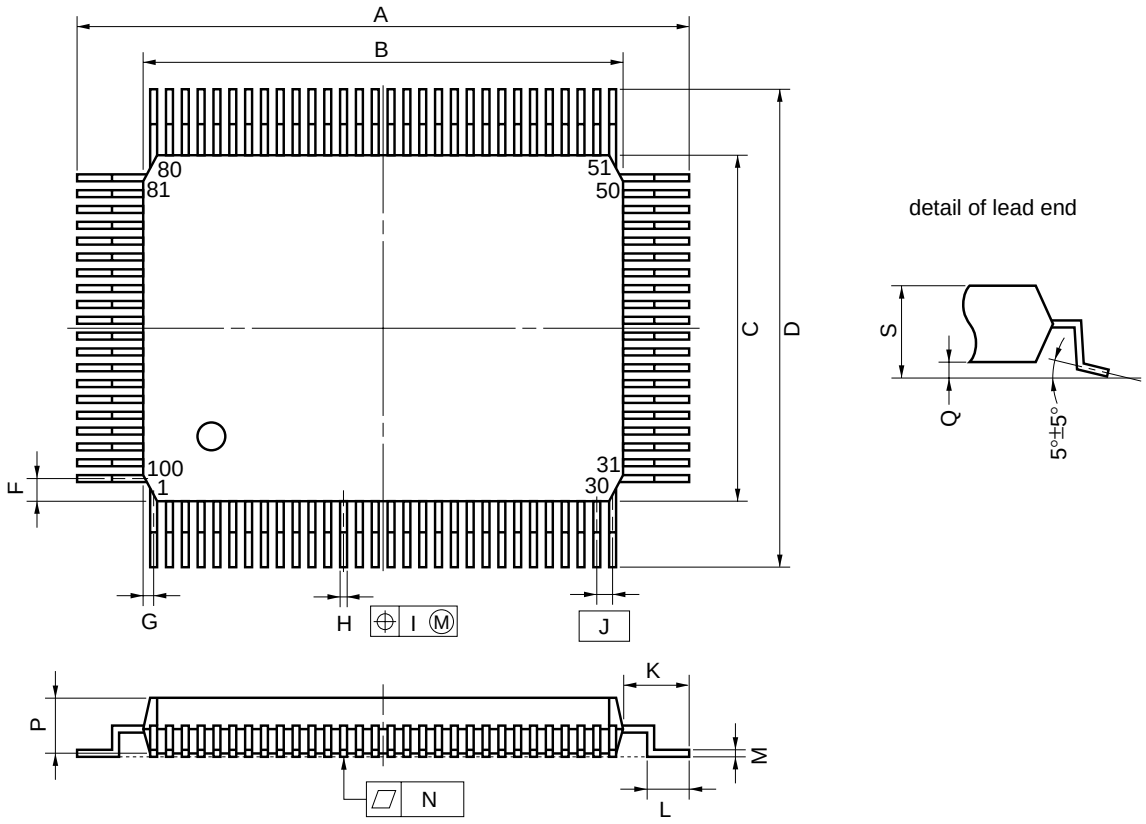


Clock output timing



7. PACKAGE DRAWING

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark

External Dimensions of the ES version are the same as those of the mass-produced version.

★ 8. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD784915A and 784916A.

For details of the recommended soldering conditions, refer to the NEC document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 18-1. Soldering Conditions for Surface-Mount Type

μPD784915AGF-×××-3BA : 100-pin plastic QFP (14 × 20 mm)
μPD784916AGF-×××-3BA : 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max. Duration: 10 sec. max. Number of times: 1 Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	–

Caution Using more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784916A.

Language Processing Software

RA78K4[Note 1]	78K/IV Series common assembler package
CC78K4[Note 1]	78K/IV Series common C compiler package
CC78K4-L[Note 1]	78K/IV Series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P4916GF	PROM programmer adapter connected to PG-1500
PG-1500 controller[Note 2]	PG-1500 control program

Debugging Tools

IE-784000-R	78K/IV Series common in-circuit emulator
IE-784000-R-BK	78K/IV Series common break board
IE-784000-R-EM	78K/IV Series common emulation board
IE-784915-R-EM1	μPD784915 Subseries evaluation emulation board
IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine
IE-70000-98-IF-B	Interface adapter when PC-9800 Series (except notebook PC) is used as the host machine
IE-70000-98N-IF	Interface adapter and cable when PC-9800 Series notebook PC is used as the host machine
IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as the host machine
EP-784915GF-R	μPD784915 Subseries common emulation probe
EV-9200GF-100	Conversion socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA)
SM78K4[Note 3]	78K/IV series common system simulator
ID78K4[Note 3]	IE-784000-R integrated debugger
DF784915[Note 4]	μPD784915 Subseries common device file

Real-time OS

RX78K/IV[Note 4]	78K/IV Series common real-time OS
MX78K4[Note 2]	78K/IV Series common OS

Notes 1.
- PC-9800 Series (MS-DOS™) based
- IBM PC/AT and compatibles (PC DOS™, Windows™, MS-DOS, IBM DOS™) based
- HP9000 Series 700™ (HP-UX™) based
- SPARCstation™ (SunOS™) based
- NEWS™ (NEWS-OS™) based

2.
- PC-9800 Series (MS-DOS) based
- IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, IBM DOS) based

3.
- PC-9800 Series (MS-DOS + Windows) based
- IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, IBM DOS) based
- HP9000 Series 700 (HP-UX) based
- SPARCstation (SunOS) based

4.
- PC-9800 Series (MS-DOS) based
- IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, IBM DOS) based
- HP9000 Series 700 (HP-UX) based
- SPARCstation (SunOS) based

Remark The RA78K4, CC78K4, SM78K4, and ID78K4 are used in combination with DF784915.

APPENDIX B. RELATED DOCUMENTS

Documents related to devices

Document Name	Document Number	
	Japanese	English
μPD784915 Subseries User's manual - Hardware	U10444J	U10444E
μPD784915 Data Sheet	U11044J	U11044E
μPD784915A, 784916A Data Sheet	U11022J	This document
μPD78P4916 Data Sheet	U11045J	U11045E
μPD784915 Subseries Appllication Note	U11361J	U11361E
μPD784915 Subseries Special function register table	U10976J	–
78K/IV Series User's manual - Instruction	U10905J	U10905E
78K/IV Series Instruction table	U10594J	–
78K/IV Series Instruction set	U10595J	–
78K/IV Series Application note - Software fundamental	U10095J	U10095E

Documents related to development tools (user's manual)

Document Name		Document Number	
		Japanese	English
RA78K Series Assembler package	Language	U11162J	U11162E
	Operation	U11334J	U11334E
RA78K Series Structured assembler preprocessor		U11743J	U11743E
CC78K4 Series	Language	EEU-961	–
	Operation	EEU-960	–
CC78K Series Library source file		U12322J	–
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) based		EEU-5008	U10540E
IE-784000-R		EEU-5004	EEU-1534
IE-784915-R-EMI		U10931J	–
SM78K4 System Simulator Windows™ based	Reference	U10093J	U10093E
SM78K Series System Simulator	External parts user open interface specifications	U10092J	U10092E
ID78K4 Integrated debugger - PC-9801, 9821 Series (Windows) based	Reference	U10440J	U10440E
ID78K4 Integrated debugger - HP9000 Series 700 (HP-UX) based	Reference	U11960J	–

Documents related to embedded software (user's manual)

Document Name		Document Number	
		Japanese	English
RX78K/IV Real-time OS	Basics	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–
78K/IV Series OS MX78K4	Fundamental	U11779J	–

Caution The documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other related documents

Document Name	Document Number	
	Japanese	English
IC package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	–
Semiconductor Devices Quality Guarantee Guide	C11893J	MEI-1202
Microcomputer Product Series Guide	U11416J	–

Caution The documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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J96. 8

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