USAR ACPITroller™ 342 Robust 8042 Keyboard / ACPI-Embedded Controller

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Preliminary
USAR System Management family product specifications

Description

The USAR ACPITroller™ 342 UR8HC342 is a single IC that functions both as an 8042-type Human Input Device Controller (HIDC) and an ACPI-compliant Embedded Controller (EC). The UR8HC342 provides the typical functionality of an 8042-type HID Controller with embedded key and motion scanning. In addition, the UR8HC342 functions as an ACPI-compliant Embedded Controller (EC) and SMBus host.

The IC achieves unparalleled minimum power consumption (typically less than 1µA) due to USAR's patented Zero-Power™ technologies for both PS/2 ports and the SMBus port - an industry first. The USAR ACPITroller™ 342 can power down even when devices are connected and active. Based on USAR's patented Zero-Power™ technology, the UR8HC342 always operates in the "STOP" mode, independently of the configuration and without any data or event losses.

Using the UR8HC342, system designers can implement systems that take advantage of the SMBus, the Smart Battery System, and the ACPI specifications, all using a single IC. The UR8HC342 can be customized easily through an extensive library of hardware and firmware modules in order to accommodate specialized configurations at low production cost.

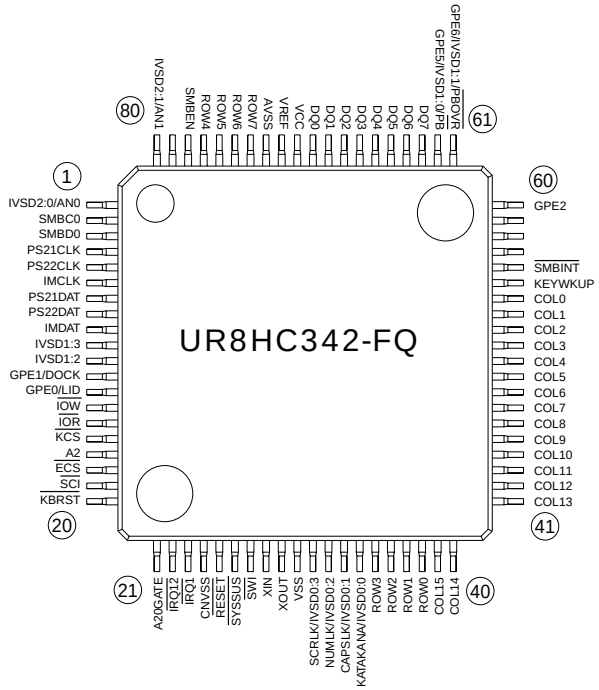
Features

- Acts as an 8042 HID and ACPI Embedded Controller
- Typically consumes less than 1µA
- Two external PS/2 ports for external keyboard and mouse with auto-detect and hot-plug support
- Patented Zero-Power™ operation of all PS/2 ports and the SMBus port - an industry first
- Simultaneous operation of external and internal input devices
- AlphaMouse™ Pointing Devices Manager provides Mousewheel support- a first for an EC
- Acts as a keyboard controller and encoder for an 8 x 16 keyboard matrix; supports all three keyboard scan code sets
- AlphaKey™ keyboard manager enables matrix programming
- Support of up to 6 ACPI GPE interrupt inputs
- 100% compatible with the ACPI specifications
- SMBus compatible host complies with version 1.0 of the SBS/SMBus specifications
- Firmware filters any dangerous SMBus commands
- Offers Internal Virtual SMBus Devices (IVSDs) such as GPIO or 10-bit A/D
- Three-volt and five-volt operation
- Customized versions available

Applications

- Handhelds / Notebooks
- Industrial / Vertical systems
- ACPI-compatible systems
- Single Board Computers

Pin Assignments

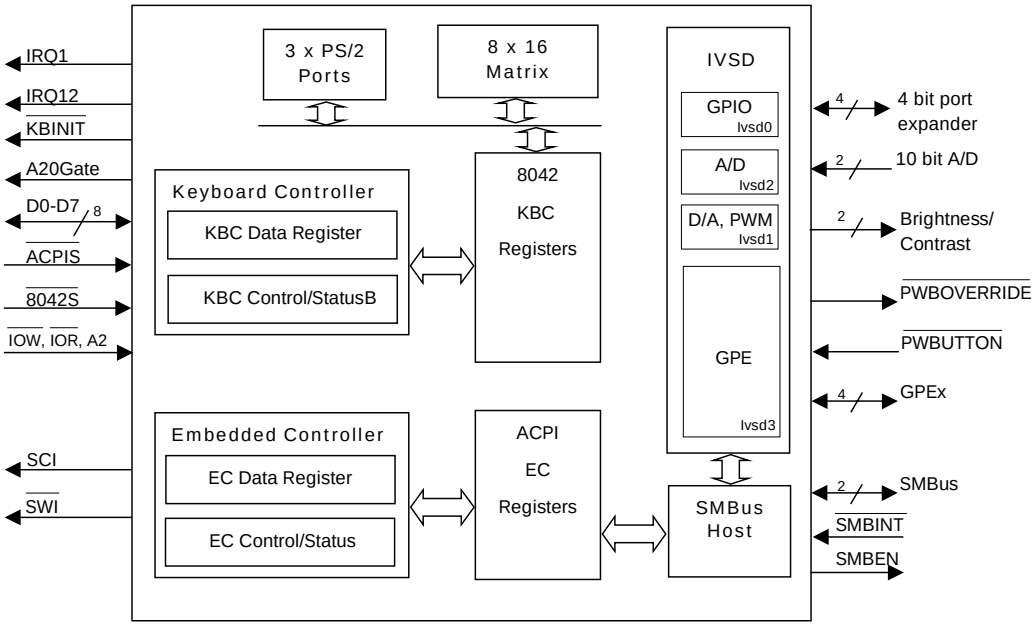


Ordering Code

Package options	Pitch in mm's	TA = 0°C to +75°C
80-pin, Plastic LQFP	0.5	UR8HC342-XX-FQ
Other materials	Type	Part number
Technical Reference Manual	Document	DOC8-342-TR-XXX

XX = Optional for customization
XXX = Denotes revision number

USAR ACPITroller™ 342 Block Diagram



Pin Definitions

Pin Numbers Mnemonic	LQFP	Name and Function
Power Supply		
AVSS	73	Analog Signal Ground
CNVSS	24	Should be tied to ground
VCC	71	Vcc 3-5 Volts
VREF	72	Analog circuitry reference voltage
VSS	30	Ground
Oscillator pins		
XIN	28	Oscillator input (8 MHz operating freq)
XOUT	29	Oscillator output
Reset		
_RESET	25	Controller hardware reset pin
System bus interface pins		
_8042S	16	8042 keyboard controller port select signal input
_ACPIS	18	ACPI embedded controller port select signal output
_IOR	15	X-bus/ISA address I/O signal input
_IOW	14	X-bus/ISA address I/O write signal input
_IRQ1	23	Keyboard interrupt output
_IRQ12	22	Mouse interrupt output
_KBINIT	20	Keyboard initialize output
A2	17	X-bus / ISA address 2 input
A20GATE	21	A20 Gate output signal
DQ0-DQ7	70-63	X-bus/ ISA parallel data I/O ports
ACPI & SMBus Signals		
SCI	19	System control interrupt output
_SMBINT	56	SMBus interrupt
_SWI	27	System wake-up event interrupt output
_SYSSUS	26	System suspend input
IVSD00/SCROLL_LOCK	31	This pin can be programmed to act as a keyboard LED or as a GPIO pin of internal virtual SMBus device 0 (IVSDO)(4-bit port expander)
IVSD01/NUM_LOCK	32	This pin can be programmed to act as a keyboard LED or as a GPIO pin of internal virtual SMBus device 0 (IVSDO)(4-bit port expander)
IVSD02/CAP_LOCK	33	This pin can be programmed to act as a keyboard LED or as a GPIO pin of internal virtual SMBus device 0 (IVSDO)(4-bit port expander)
IVSD03/KATAKANALED	34	This pin can be programmed to act as a keyboard LED or as a GPIO pin of internal virtual SMBus device 0 (IVSDO)(4-bit port expander)
IVSD10/PWM1	62	IVSD1 bit 0 or PWM output
IVSD11/PWM2	61	IVSD1 bit 1 or PWM output
IVSD12/DA1/PWM1	11	This pin can be configured as GPIO, as D/A output, or PWM output

Pin Definitions

Mnemonic	Pin Numbers LQFP (con't)	Name and Function
ACPI & SMBus Signals		
IVSD13/DA2/PWM2	10	This pin can be configured as GPIO, as D/A output, or PWM output
IVSD20	1	This pin can be configured as a 10-bit A/D input or logic I/O
IVSD20	1	This pin can be configured as a 10-bit A/D input or logic I/O
IVSD13/DA2/PWM2	10	This pin can be configured as GPIO, as D/A output, or PWM output
IVSD20	1	This pin can be configured as a 10-bit A/D input or logic I/O
IVSD21/AN1	80	This pin can be configured as a 10-bit A/D input or logic I/O.
IVSD22/AN2	79	IVSD2 bit or A/D input
IVSD30/GPE0/LID	13	IVSD3 bit 0 or ACPI general purpose event (GPE); capable of detecting both negative and positive signal transitions; typically serves the LID ACPI function
IVSD31/GPE1/DOCK	12	IVSD3 bit 1 or ACPI GPE; capable of detecting both negative and positive signal transitions; typically serves the DOCK ACPI function
IVSD32/GPE2/_PWBUTTON	60	IVSD3 bit 2 or ACPI GPE; typically an ACPI ""Power Button"" input.
IVSD33/GPE3/ /_PWBOVERRIDE	59	IVSD3 bit 3 or ACPI GPE; typically an ACPI ""Power Button Override"" input
IVSD34/GPE4	58	IVSD3 bit 4 or ACPI GPE 4
IVSD35/GPE5	57	IVSD3 bit 5 or ACPI GPE 5
SCL0	2	This pin acts as the clock line for the SMBus
SDA0	3	This pin acts as the data line for the SMBus
SMBEN	78	This output pin allows the SMBus latch to notify the ACPITroller™ Basic when SMBus activity has been detected. It is used to wake the ACPITroller™ Basic from sleep mode, and to disable all PS/2 inputs while SMBus processing is taking place.
Scanned Matrix Pins		
COL0-COL15	54-39	Column matrix outputs
KEYWKUP	55	Key wake-up output
ROW0-ROW7	38-74	Row matrix inputs
PS/2 Ports		
IMCLK	6	PS/2 clock line for internal mouse
IMDAT	9	PS/2 data line for internal mouse
PS20CLK	5	Clock line for external PS/2 port 0; both external PS/2 ports support hot-plug ins and auto-select for keyboard or mouse
PS20DAT	8	Data line for external PS/2 port 0
PS21CLK	4	Clock line for external PS/2 port 1
PS21DAT	7	Data line for external PS/2 port 1

Note 1: An underscore in front of the pin mnemonic denotes an active low signal.

Features

The following pages contain brief descriptions of the features provided by USAR's UR8HC342. For more detailed information, please refer to the USAR UR8HC342 ACPITroller™ 342 Technical Reference Manual, document number DOC8-342-TR-XXX.

ACPI Embedded Controller Interface

USAR's UR8HC342 ACPI embedded controller (EC) interfaces to the Host's ISA bus via two I/O addresses. Three registers (Status, Command and Data) occupy the two I/O addresses. The operating system can communicate with the EC using the standard ACPI embedded controller command set. The host can either issue a command byte to the command register directly or send a data byte to the data port.

8042 Human Input Device Controller Interface (HIDC)

The HIDC portion of USAR's UR8HC342 interfaces the Host via two I/O addresses: 0x60 and 0x64. Three registers occupy the two I/O locations: Command, Status and Data. Any byte written by the Host system to the Command register is interpreted as a command. The UR8HC342 supports all the standard 8042 commands as well as many expanded commands.

Expanded commands provide such functionality as the ability to create password protection and disable an auxiliary input device.

SMBus Host Controller Interface

The SMBus host manages one Zero-Power™ SMBus port for an SMBus device, such as a smart battery. USAR's SMBus controller interfaces the system via ISA and complies with the latest (v1.0) SBS and SMBus specifications.

The SMBus Host Controller Interface allows the Host processor, under control of the operating system, to manage both real and virtual devices on the SMBus, including those belonging to the Smart Battery System. Such devices include contrast/backlight controllers and temperature sensors. The SMBus Host Controller interface allows the OS to directly address devices on the SMBus. It provides a method of communicating with SMBus devices through a block of registers that reside in the Embedded Controller space. In addition, the USAR UR8HC342's SMBus Host Controller handles certain SMBus functions related to alerts and error conditions.

Interrupts and General Purpose Events

The UR8H359 provides up to 5 customizable ACPI General Purpose Events (GPE). The IC generates two types of interrupts: SCI and SWI. The type of interrupt generated depends on the type of event that caused it. When a standard SMBus command occurs, the EC generates an SCI interrupt. For any other General Purpose Events (GPE), an SWI interrupt occurs. GPE events can include lid and dock events or power button presses.

SWI interrupts have the ability to wake-up the system if it is in suspend. SCI interrupts cannot do this.

Power Management

The USAR ACPITroller™ 342 typically consumes less than 1 µA. For further power savings, the three PS/2 ports use USAR's patented Zero-Power™ PS/2 technology and the one SMBus port uses USAR's patented Zero-Power™ SMBus technology. The IC can power down even when devices are connected and active, and wake up when needed without data loss.

Internal Virtual SMBus Devices

Modeled on SMBus devices, Internal Virtual SMBus Devices (IVSDs) are general-purpose devices that can be used for system tasks. The Host can address these devices through the ACPI EC interface in the same way it would address any external device residing on a SMBus port.

The IVSDs are implemented on shared pins of the UR8HC342. Specific pins can be used in other keyboard or embedded controller functions and the ISVDs need to be enabled through the configuration registers residing either in the EC or in the HID controller area. Once the devices are enabled, they can be accessed by the Host through standard interfaces defined in the relevant industry specification.

IVSDs can include port expanders, flat panel digital controls, 10 bit A/D or GPIO port.

AlphaMouse™ Pointing Devices Manager

The USAR AlphaMouse™ pointing devices manager can simultaneously support up to three mice (including those with MouseWheel) connected to both the external and internal PS/2 ports of the USAR ACPITroller™ 342. Different types of standard mice (two-button, three-button, MouseWheel) can be connected simultaneously, as the AlphaMouse™ pointing device manager multiplexes the input. The manager supports hot plugging and hot swapping of standard two-button and three-button mice without a special driver, and of MouseWheel-enabled mice with a standard MouseWheel-capable driver.

The USAR AlphaMouse™ pointing devices manager receives its pointing device input through one or more of the USAR ACPITroller™ 342 PS/2 ports. The PS/2 Ports Driver will auto-detect the type of device connected to each PS/2 port. If the device reports itself as a pointing device, it will connect it to the USAR AlphaMouse™ pointing devices manager for proper initialization and further data and command handling. The USAR AlphaMouse™ pointing device manager communicates with the host system through the mouse port of the HID controller.

AlphaMouse™ Features

- Handles both internal and external mouse command communications
- Hot-plug and hot swapping support for external mice
- Transparent MouseWheel support for external mouse
- Simulates MouseWheel support for internal mouse
- Simulates MouseWheel operation, by merging normal mouse data with AlphaKey™ keyboard codes
- Merges internal and external mouse data
- Operates safely with PS/2 mouse protocol

AlphaKey™ Features

- Supports IBM standard 101/102 keyboard including Windows®, On-Now Power keys and Japanese keyboard keys
- Allows full OEM programmability, including programmable scan matrix
- Offers support of OEM-defined firmware procedures that can be invoked by key presses
- Unique Zero-Power™ operation of the scanned matrix and the PS/2 embedded port
- Provides “Protocol Safe” handling of external PS/2 devices
- Allows hot-plug connection of external keyboard
- External and internal keyboards operate simultaneously; data is merged
- Auto-detects type of device in any external PS/2 port
- Interoperability between 3-Volt and 5-Volt PS/2 devices without the need for external level-shifting circuitry
- Supports all three Scan Code Sets
- Offers N-Key rollover and ghost key detection
- Enables single-hand data entry through “Sticky Key” mode of operation
- Supports embedded numeric keypad

AlphaKey™ Keyboard Manager

The AlphaKey™ Keyboard Manager is the most advanced keyboard management module in the industry today and the first one to integrate the laptop keyboard matrix with system management tasks through ACPI and SMBus.

USAR’s AlphaKey™ provides OEMs with extreme flexibility both with PS/2 keyboard functionality as well as with designating which system management tasks users can control through the keyboard.

The USAR AlphaKey™ Keyboard Manager communicates with the HID Controller, the ACPI EC, the Virtual SMBus Device Manager and the external PS/2 ports of the UR8HC342.

USAR’s AlphaKey™ will simultaneously support both an external keyboard (including Windows® and Japanese layout keyboards) and an internal scanned key matrix. The internal scanned matrix layout can be programmed through an extended set of keyboard commands. AlphaKey™ handles PS/2 keyboard commands, supports external keyboard hot-plug-ins and merges internal and external data as if they were coming from one source.

In addition, OEMs can assign and download custom-defined keyboard macros or procedures that can be invoked through simple key presses to the AlphaKey’s™ internal RAM memory.

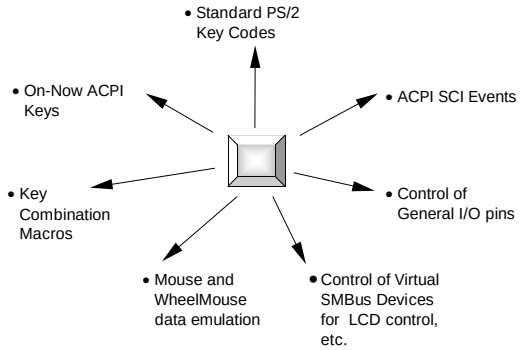
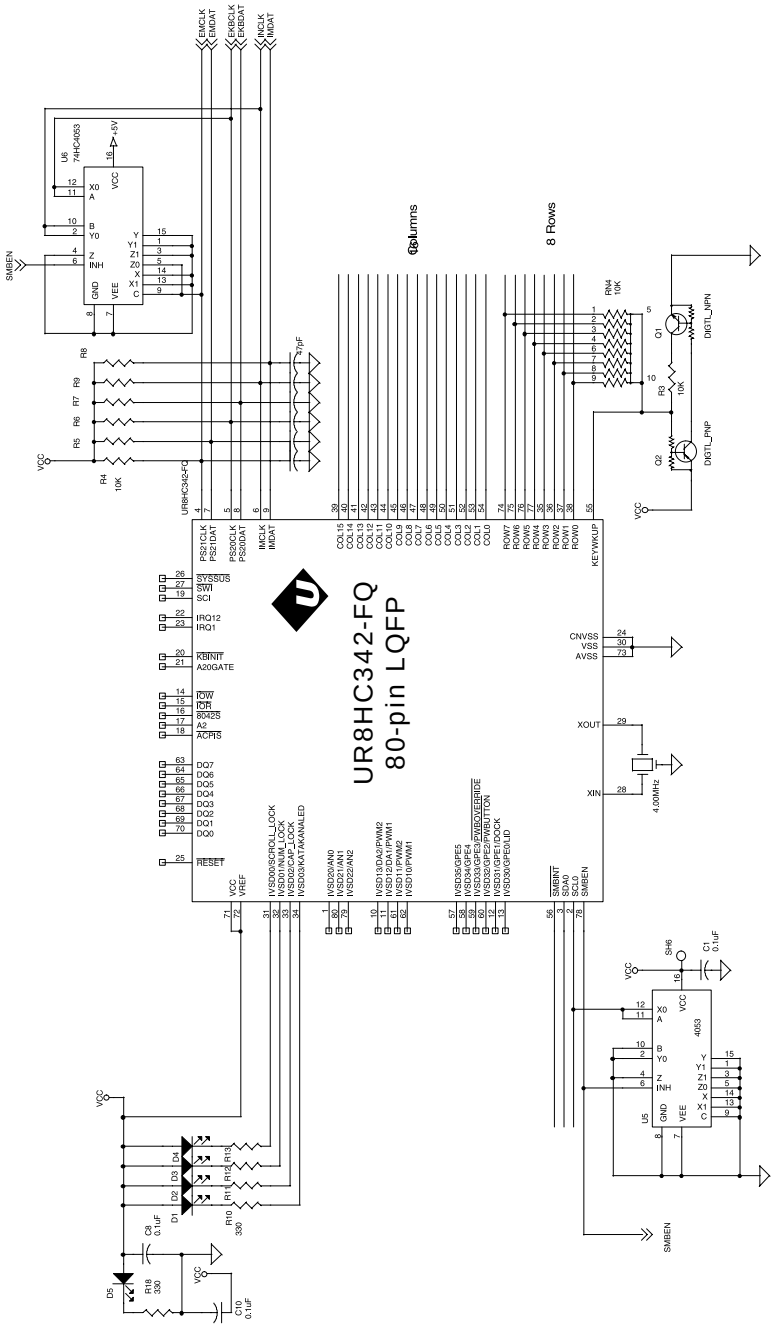
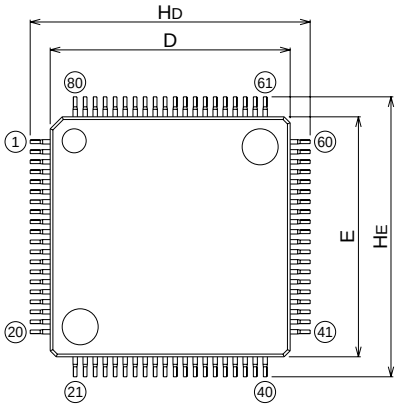


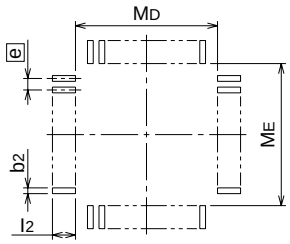
Figure 1: AlphaKey™ features

Suggested Interfacing for the USAR ACPITroller™ 342 UR8HC342-FQ

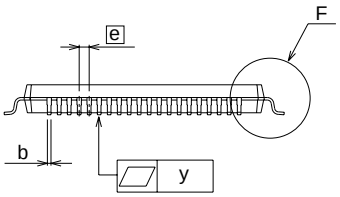


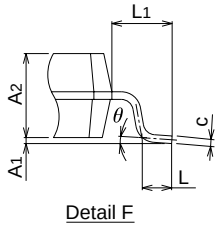
Mechanical Information for FQ (80 Pin LQFP) Package





Recommended Mount Pad





Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	12.4	–
M_E	–	12.4	–

Notes for Electricals

Note1:

Current Consumption values do not include any loading on the Output pins or Analog Reference Current for the built-in A/D or D/A modules.

Note 2:

Since the built-in A/D module consumes current only during short periods of time (when A/D conversion is actually requested), the Analog Reference Current for the built-in A/D module is not a significant contributor to the overall power consumption.

Note 3:

The Analog Reference Current for the built-in D/A module correlates linearly to the Output Voltage. For D/A output of 0V, the Analog Reference Current is null. For D/A outputs approaching Full Scale (AVREF), the maximum Analog Reference Current is indicated in this Table. This current is a significant contributor to the overall power consumption.

UR8HC342 Electrical Characteristics, continued

Recommended Operating Conditions, Digital Section

(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	3.0	5.5	V
Input logic high voltage					
All pins except 2-9	V_{IH}	0.8V_{DD}		V_{DD}	V
Pins 2-9 (PS/2 ports xxxDAT, xxxCLK, GIO16/SW16, GIO17/SW17)	V_{IH}	0.8V_{DD}		5.5	V
Input logic low voltage					
All pins except 28	V_{IL}	0		0.2V_{DD}	V
Pin 28 (OSCI)	V_{IL}	0		0.16V_{DD}	V
Input current V_I = V_{SS}, V_{DD})	I_{IL} / I_{IL}	-5.0	0	5.0	µA
Input Pull-up Current (pins 56-58 / IP6-IP8, V_I = V_{SS})	I_{PUP}	-120		-10	µA
Output voltage					
I_{OH} = -1.0 mA	V_{OH}	V_{DD}-1.0			V
I_{OL} = 1.6 mA	V_{OL}			0.4	V
Current Consumption (see note 1 below)					
Full Speed Mode (Fosc=4MHz)	I_{DD}		3.5	7.0	mA
Reduced Power Mode (Fosc=4MHz)	I_{DD}		750		µA
Stop Mode (Interrupts active, Fosc=0)				1.0 (T_A = 25ºC)	
	I_{DD}		.1	10(T_A = 85ºC)	µA

Recommended operating conditions, analog section

(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

Parameter	Symbol	Min	Typ	Max	Unit
Analog Signal Ground	AV_{SS}		0		V
Analog Reference Voltage	AV_{REF}	2.7	V_{DD}	V_{DD}	V
A/D Resolution-				10	Bits
A/D Absolute Accuracy				± 4	LSb
A/D Analog Input Voltage Range	V_{IA}	AV_{SS}		AVREF	V
A/D Analog Input Current	I_{IA}			5.0	µA
Analog Reference Current (see note 2) (A/D is active)	I_{AVREF}			200	µA
D/A Resolution-				8	Bits
D/A Absolute Accuracy -				2.5	%
D/A Output Impedance	R_O	1	2.5	4.0	KOhms
Analog Reference Current (see note 3) (D/A is active, Output = Full Scale)	I_{AVREF}			3.2	mA

Note 1: please see left
Note 2: please see left
Note 3: please see left

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A Semtech Company

USAR®

For sales information
and product literature,
contact:

USAR – A Semtech Company
568 Broadway
New York, NY 10012
info@usar.com
http://www.usar.com
212 226 2042 Telephone
212 226 3215 Telefax

In Japan:
Semtech Japan
Tel: 81-45-948-5925
Fax: 81-45-948-5930

In Taiwan:
Semtech Asia/Pacific Sales
Tel: 011-886-2-2748-3380
Fax: 011-886-2-2748-3390

Koryo Electronics Co., Ltd.
Telephone +886-2-2698-1143
E-mail alex.chen@koryo.com.tw

In Korea:
Semtech Korea
Tel: 011-82-2-527-4377
Fax: 011-82-2-527-4376

In Europe
Semtech Limited
Tel: +44-1592-630350
Fax: +44-1592-774781