FAIRCHILD SEMICONDUCTOR™

June 2005
Revised June 2005

USB1101
USB 2.0 FS Peripheral Transceiver (Preliminary)

General Description

The USB1101 provides a USB FS Transceiver functionality with voltage level translation that is compliant to USB Specification Rev 2.0. The device allows interfacing of USB Application specific devices with supply voltages ranging from 1.65V to 3.6V with the physical layer of Universal Serial Bus. It is capable of operating at 12Mbits/s (full speed) data rates and hence is fully compliant to USB Specification Rev 2.0. It supports the DAT_VP/SE0_VM interface on the host side but offers reduced pin count and package size. The USB1101 has host side supply rail for 1.65V to 3.6V.

Features

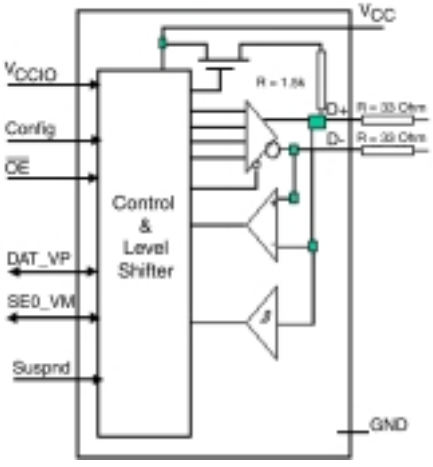
- Complies with USB Specification Rev 2.0
- Supports DAT_VP/SE0_VM host mode
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports full speed (12Mbits/s) data rates
- Ideal for portable electronic devices
- MicroPak™ technology package (10 pin) 1.6mm x 2.1mm
- Host side V_{CCIO} 1.65V to 3.6V

Applications

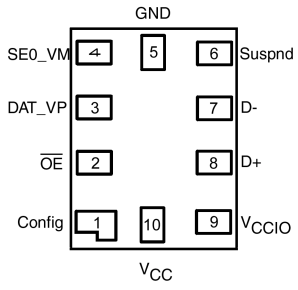
- PDA
- PC Peripherals
- Cellular Phones
- MP3 Players
- Digital Cameras
- Information Appliance

Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
USB1101L10X	MAC010A	UB	10-Lead MicroPak, 1.6 mm x 2.1mm	5k Units on Tape and Reel



Connection Diagram



(Bottom View)

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Pin Description

Pin Number	Pin Name	I/O	Pin Description
1	Config	I	USB connect or disconnect software control input. Configures 3.3V to internal 1.5kΩ resistor on D+ when HIGH. If device is used as Downstream port then this pin is hard-wired to GND.
2	$\overline{OE}$	I	Output Enable (active LOW) When $\overline{OE}$ = L transmit mode is enabled When $\overline{OE}$ = H receive mode (CMOS level is relative to V_{CCIO}) is enabled.
3	DAT_VP	I/O	When in transmit mode(Note 2) DAT_VP is a single-ended host data input (CMOS level relative to V_{CCIO}). When in receive mode(Note 1) and Suspnd = L DAT_VP is a single ended data output comprised of the differential input data from the D+/D– inputs (see Table 2); When in receive mode(Note 1) with Suspnd = H DAT_VP outputs the D+ data. (see Table 1 and Table 2) Output drive is 2mA (min) buffer
4	SE0_VM	I/O	When in transmit mode(Note 2) SE0_VM is a data input (CMOS level relative to V_{CCIO}). When in receive mode(Note 1) and Suspnd = L, SE0_VM is used as an output (see Table 2) (see Table 1 and Table 2). Output drive is 4ma (min) buffer
5	GND	GND	GND
6	Suspnd	I	Enables a low power state (CMOS level is relative to V_{CCIO}). In receive mode(Note 1) with Suspnd = L the DAT_VP pin will be a function of the D+/D– lines. In receive mode(Note 1) with Suspnd = H DAT_VP will have the value of D+ such that the device can still monitor out-of-suspend signaling.
7, 8	D–, D+	AI/O	Data+, Data–. Differential data bus conforming to the USB standard
9	V_{CCIO}	Pwr	Supply Voltage for host side digital I/O pins (1.65V to 3.6V)
10	V_{CC}	Pwr	Supply Voltage Input (3.0V to 3.6V)

Note 1: $\overline{OE}$ = H

Note 2: $\overline{OE}$ = L

Functional Description

The USB1101 transceiver is designed as an Upstream facing port device to convert CMOS data into USB differential bus signal levels and to convert USB differential bus signal to CMOS data. If you wish to use these as downstream devices, Config must be hard-wired to GND.

To minimize EMI and noise the outputs are edge rate controlled with the rise and fall times controlled and defined for full speed data rates only (12Mbits/s). The rise and fall times are balanced between the differential pins to minimize skew.

The USB1101 supports the DAT_VP/SE0_VM format from the OTG Transceiver Specification using the DAT_SE0 Mode. Table 1 describes the specific pin functionality selection and Table 2 describes the specific Truth Tables for Driver, Receiver, and Suspended operating functions.

The USB1101 has the capability of serving Self Powered power supply configurations only but interfaces to mixed voltage supply applications.

TABLE 1. Function Select

Suspnd	$\overline{OE}$	D+, D–	DAT_VP	SE0_VM	Function
L	L	Transmitting	Host Data Input	SE0_VM Host Input	Normal Driving
L	H	Receiving (Note 3)	D+, D– Diff Output	SE0_VM Output	Receiving
H	L	Transmitting (Note 4)	Host Data Input	SE0_VM Host Input	Driving while Suspended
H	H	Driver is 3-STATE (Note 4)	DAT_VP Output	SE0_VM Output	Suspended (Internal Low Power Mode)

Note 3: Signal levels is function of connection, Config and/or pull-up/pull-down resistors.

Note 4: For Suspnd = HIGH mode the differential receiver is inactive.

TABLE 2. Driver, Receiver, and Suspend Function Select

Suspnd = L	**Transmit Mode**				
Inputs			**Outputs**		
$\overline{\textbf{OE}}$	**DAT_VP**	**SEO_VM**	**D+**	**D–**	
L	L	L	L	H	Differential Logic 0
L	H	L	H	L	Differential Logic 1
L	L	H	L	L	SE0
L	H	H	L	L	SE0
Suspnd = L	**Receive Mode**				
Inputs			**Outputs**		
$\overline{\textbf{OE}}$	**D+**	**D–**	**DAT_VP**	**SEO_VM**	
H	L	L	DIFF (Note 5)	H	
H	H	L	H	L	
H	L	H	L	L	
H	H	H	DIFF (Note 5)	L	
Suspnd = L	**Receive Mode**				**While Suspended**
Inputs			**Outputs**		
$\overline{\textbf{OE}}$	**D+**	**D–**	**DAT_VP**	**SEO_VM**	
H	L	L	L (Note 6)	H	
H	H	L	H (Note 6)	L	
H	L	H	L (Note 6)	L	
H	H	H	H (Note 6)	L	
Suspnd = H	**Transmit Mode**				
Inputs			**Outputs**		
$\overline{\textbf{OE}}$	**DAT_VP**	**SEO_VM**	**D+**	**D–**	
L	L	L	L	H	Differential Logic 0
L	H	L	H	L	Differential Logic 1
L	L	H	L	L	SE0
L	H	H	L	L	SE0

Note 5: DIFF denotes that the output of the differential receiver is output via DAT_VP when Suspnd = L. This output should also not be gated by the SE0 or SE1 condition when a skew between D+ and D– signals could result in the short SE0 or SE1 conditions. Please refer to Expectation Notes for further information.

Note 6: This is the internal single ended output that is output on to DAT_VP when Suspnd = H and in receive mode.

Power Supply Configurations and Options

The modes of power supply operation include:

1. Self Powered Mode: V_{CC} is connected to 3.3V source (3.0V to 3.6V). This external supply connection provides the 3.3V for the USB pull-up source, the receiver input and driver output circuitry.
2. Sharing Mode: V_{CCIO} is connected and V_{CC} is ≤ 0.8V. In this mode the D+ and D– pins are 3-STATE and the USB1101 allows external signals up to 3.6V to share the D+ and D– bus lines. Internally the circuitry limits leakage from D+ and D– pins (maximum 10μA) and V_{CCIO} such that the device is in low power state.
3. Disable Mode: V_{CCIO} is ≤ 0.5V and V_{CC} is connected. In this mode the D+ and D– pins are 3-STATE and the device is in low power state.

A summary of the Supply Configuration is described in Table 3.

TABLE 3. Power Supply Configuration Options

Pin	**Power Supply Mode Configuration**		
	Sharing	**Self Powered**	**Disable**
V_{CC}	≤ 0.8V or Not Connected	Connected to 3.3V Source	Connected to 3.3V Source
V_{CCIO}	1.65V to 3.6V Source	1.65V to 3.6V Source	≤ 0.5V or Not Connected
D+, D–	3-STATE	Function of Mode Set Up	3-STATE
DAT_VP, SE0_VM	H	Function of Mode Set Up	(Invalid)

Absolute Maximum Ratings(Note 7)

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
V_{CC}	Supply Voltage		−0.5	4.6	V
V_{CCIO}	I/O Supply Voltage		−0.5	4.6	V
I_{IK}	DC Input Current	$V_I < 0$		−18.0	mA
V_I	DC Input Voltage	(Note 8)	−0.5	V_{CCIO} + 0.5	V
I_{OK}	DC Output Diode Current	$V_O > V_{CC}$ or < 0		±18.0	mA
V_O	DC Output Voltage	(Note 8)	−0.5	V_{CCIO} + 0.5	V
I_O	DC Output Source or Sink Current for D+, D− Pins SE0_VM/DAT_VP	V_O = 0 to V_{CC}		±12.0 ±12.0	mA
I_{CC}, I_{GND}	DC V_{CC} or GND Current			±100	mA
V_{ESD}	ESD Immunity Voltage HBM (Mil-std. 883E)	I_O, GND, V_{CC} Pins (Note 8)	2000	TBD	V
	MM (ESD_STM 5.2)	V_{CCIO} + 0.5 Pins (Note 9)	200	TBD	V
	CDM (ESD_STM 5.3.1)	I_O, GND, V_{CC} Pins (Note 10)	1000	2000	V
	HBM (Mil-std. 883E)	Pins D+, D− (Note 11)	TBD	TBD	V
		USB Connector	TBD	TBD	V
T_{STO}	Storage Temperature Range		−40.0	+125	°C
P_{TOT}	Power Dissipation	I_{CC}		60.0	mW

System ESD Testing

System	Parameter	Conditions	Limits		Units
			Min	Max	
ESDsys	IEC61000-4-2 (Note 12)	USB Connector	TBD	TBD	V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
V_{CC}	DC Supply Voltage		3.0	3.6	V
V_{CCIO}	I/O DC Voltage		1.65	3.6	V
V_I	DC Input Voltage Range		0	3.6	V
$V_{AI/O}$	DC Input Range for AI/O	Pins D+ and D−	0	3.6	V
T_{AMB}	Operating Ambient Temperature		−40.0	+85.0	°C

Note 7: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 8: HBM: Mil-Std_883E compliance. Socketed testing of three units per zap voltage (3+ pulses and 3− pulses). I_O v I_O, I_O v GND, I_O v V_{CC}, V_{CC} v GND.

Note 9: MM: ESD_STM 5.2 compliance. Socketed testing of three units per zap voltage (3+ pulses and 3− pulses). I_O v I_O, I_O v GND, I_O v V_{CC}, V_{CC} v GND.

Note 10: CDM: ESD_STM 5.3.1 compliance. Devices (3 per level) are charged, entire package, and discharged through a single pin contacted to each individual pin on the DUT. NC pins are not stressed. Positive and negative charge is placed on the DUT (sitting atop a metallic plate). Maximum stress voltage applicable at FSME is 2000V.

Note 11: This test is an extension of HBM Mil_Std 883E. However, this test is confined to the differential pins only.

Note 12: IEC61000-4-2 system level testing: System level testing done on this parts evaluation system boar.

DC Electrical Characteristics (Supply Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted): V_{CC} = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V

Symbol	Parameter	Conditions	Limits			Units
			Temperature = −40°C to + 85°C			
			Min	Typ	Max	
I_{CC}	Operating Supply Current (V_{CC})	Transmitting and receiving at 12Mbit/s; C_{LOAD} = 50pF (D_+, D_-)		4.0	8.0	mA
$I_{CC(IDLE)}$	Supply Current During FS IDLE and SE0 (V_{CC})	IDLE: $V_{D+} \geq 2.7$, $V_{D-} \leq 1.3V$; SE0: $V_{D+} \leq 0.3V$, $V_{D-} \leq 1.3V$			300 (Note 14)	µA
$I_{CC(DISABLE)}$	Disabled Supply Current	Suspnd = H or L; $\overline{OE}$ = H or L; Config = L $D_+ = D_- = DAT\_VP = SE0\_VM$ = H or L $V_{CCIO} = \leq 0.3V$			20.0	µA
$I_{CC(SUSPNDR)}$	Suspend V_{CC} Supply Current (Internal Resistor Pull-up)	Suspnd = OE = Config = H D_+ = Open			40.0	µA
$I_{CCIO(STATIC)}$	I/O Static V_{CCIO} Supply Current	IDLE, SE0			20.0	µA
$I_{CCIO(SHARING)}$	I/O Sharing Mode V_{CCIO} Supply Current	V_{CC} Not Connected or ≤ 0.5V or 0V			20.0	µA
$I_{CCIO(SUSPNDR)}$	Suspend V_{CCIO} Supply Current	Suspnd = Config = HIGH; $\overline{OE}$ = HIGH or LOW D_+ = Open			20.0	µA
$I_{D\pm(SHARING)}$	Sharing Mode Load Current on D_+, D_- Pins	V_{CC} Not Connected or ≤ 0.8V Config = LOW; $V_{D\pm}$ = 3.6V	−10.0		10.0	µA
V_{CCTH}	V_{CC} Threshold Detection Voltage (Self Powered)	3.0 ≤ V_{CC} ≤ 3.6V				V
		Supply Lost			0.8	
		Supply Present	2.4 (Note 15)			
V_{CCHYS}	V_{CC} Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		450		mV
V_{CCIOTH}	V_{CCIO} Threshold Detection Voltage	3.0V ≤ V_{CC} ≤ 3.6V				V
		Supply Lost			0.5	
		Supply Present	1.4			
$V_{CCIOHYS}$	V_{CCIO} Threshold Detection Hysterias Voltage	V_{CC} = 3.3V		450		mV

Note 13: Not tested in production, value based on characterization.

Note 14: Excludes any current from load and V_{SW} current to the 1.5kΩ and 15kΩ pull-up/pull-down resistors (200 µA typ).

Note 15: Minimum value for V_{CCTH} = 2.0V for supply present condition for V_{CCIO} = 1.8V.

DC Electrical Characteristics (Digital Pins - excludes D+, D– Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CCIO} = 1.65V to 3.6V

Symbol	Parameter	Condition	Limits		Unit
			Temperature = –40°C to + 85°C		
			Min	Max	
INPUT LEVELS					
V_{IL}	LOW Level Input Voltage			0.3 V_{CCIO}	V
V_{IH}	HIGH Level Input Voltage		0.6 V_{CCIO}		V
OUTPUT LEVELS					
V_{OL}	LOW Level Output Voltage	I_{OL} = 2 mA		0.4	V
		I_{OL} = 100 µA		0.15	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 2 mA	V_{CCIO} – 0.4		V
		I_{OH} = 100 µA	V_{CCIO}–0.15		
LEAKAGE CURRENT					
I_{LI}	Input Leakage Current	V_{CCIO} = 1.65V to 3.6V		±1.0	µA
CAPACITANCE					
C_{IN}, $C_{I/O}$	Input Capacitance	Pin to GND		10.0	pF

DC Electrical Characteristics (Analog I/O Pins - D+, D– Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Condition	Limits		Unit
			Temperature = –40°C to + 85°C		
			Min	Max	
INPUT LEVELS - Differential Receiver					
V_{DI}	Differential Input Sensitivity	| $V_{I(D+)}$ - $V_{I(D–)}$ |	0.2		V
V_{CM}	Differential Common Mode Voltage		0.8	2.5	V
INPUT LEVELS - Single-ended Receiver					
V_{IL}	LOW Level Input Voltage			0.8	V
V_{IH}	HIGH Level Input Voltage		2.0		V
V_{HYS}	Hysteresis Voltage		0.4	0.7	V
Output Levels					
V_{OL}	LOW Level Output Voltage	Config = HIGH for Internal 1.5kΩ to 3.6V		0.3	V
V_{OH}	HIGH Level Output Voltage	R_L = 15KΩ to GND	2.8 (Note 16)		V
LEAKAGE CURRENT					
I_{OZ}	Input Leakage Current OFF State			±1.0	µA
CAPACITANCE					
$C_{I/O}$	I/O Capacitance	Pin to GND		20.0	pF
RESISTANCE					
Z_{DRV}	Driver Output Impedance	Steady State	34.0 (Note 17)	44.0	Ω
Z_{IN}	Driver Input Impedance		10.0		MΩ
R_{PU}	Pull-up Resistance (Note 18)	IDLE	900	1575	Ω
R_{SW}	Switch Resistance			10.0 (Note 19)	Ω

Note 16: If V_{OHmin} = V_{CC} – 0.2V.

Note 17: Includes external 33Ω ± 1% on both pins D+ and D–.

Note 18: See USB2.0 Resistor ECN.

Note 19: Not production tested, guaranteed by design.

AC Electrical Characteristics (A I/O Pins, Full Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V, C_L = 50pF

Symbol	Parameter	Condition	Limits			Unit	Figure Number
			Temperature = −40°C to + 85°C				
			Min	Typ	Max		
DRIVER CHARACTERISTICS							
t_R	Output Rise Time	C_L = 50 – 125pF	4.0		20.0	ns	Figures 1, 5
t_F	Output Fall Time	10% to 90% $\lvert V_{OH} - V_{OL} \rvert$	4.0		20.0		
t_{RFM}	Rise/Fall Time Match	t_R / t_F Excludes First Transition from IDLE State	90.0		111.1	%	
V_{CRS} (Note 20)	Output Signal Crossover Voltage	Excludes First Transition from IDLE State	1.3	$V_{CC}/2 \pm$ 200 mV (Note 21)	2.0	V	Figures 2, 4
DRIVER TIMING							
t_{PLH}	Propagation Delay				18.0	ns	Figures 2, 5
t_{PHL}	(DAT_VP, SE0_VM to D+ / D–)				18.0		
t_{PHZ}	Driver Disable Delay				15.0	ns	Figures 4, 6
t_{PLZ}	($\overline{OE}$ to D+ / D–)				15.0		
t_{PZH}	Driver Enable Delay				15.0	ns	Figures 4, 6
t_{PZL}	(OE to D+ / D–)				15.0		
RECEIVER TIMING							
t_{PLH}	Propagation Delay (Diff)				18.0	ns	Figures 3, 7
t_{PHL}	(D+ / D– to DAT_VP)				18.0		
t_{PLH}	Single Ended Receiver Propagation Delay				18.0	ns	Figures 3, 7
t_{PHL}	(D+ / D– to DAT_VP, SE0_VM)				18.0		
t_{PLH}	Suspend to DAT_VP				15.0	ns	
t_{PHL}					15.0		

Note 20: Not production tested, guaranteed by design.

Note 21: Typical conditions (25°C, 3.3V).

Loading and Waveforms

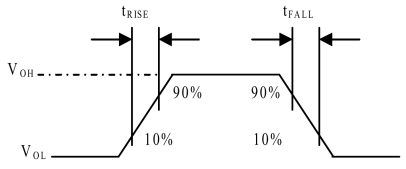


FIGURE 1. Rise and Fall Time

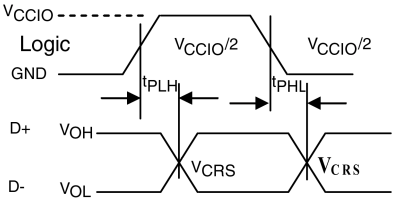


FIGURE 2. DAT_VP, SE0_VM to D+ / D–

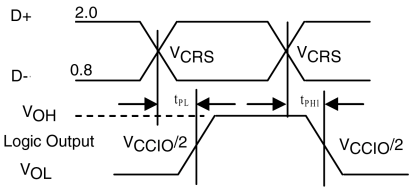


FIGURE 3. D+ / D– to DAT_VP, SE0_VM

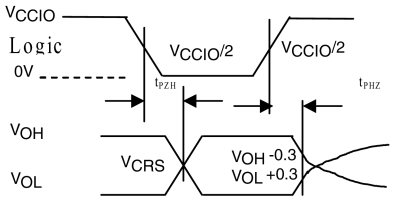


FIGURE 4. $\overline{OE}$ to D+ / D–

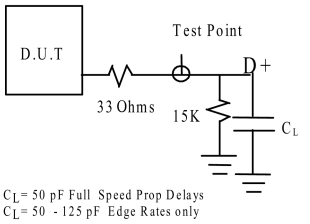


FIGURE 5. Load for D+ / D–

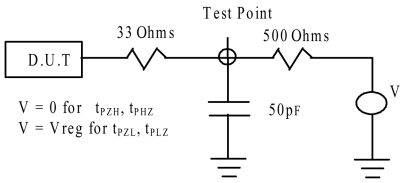


FIGURE 6. Load for Enable and Disable Time

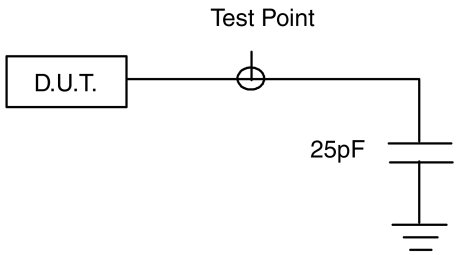
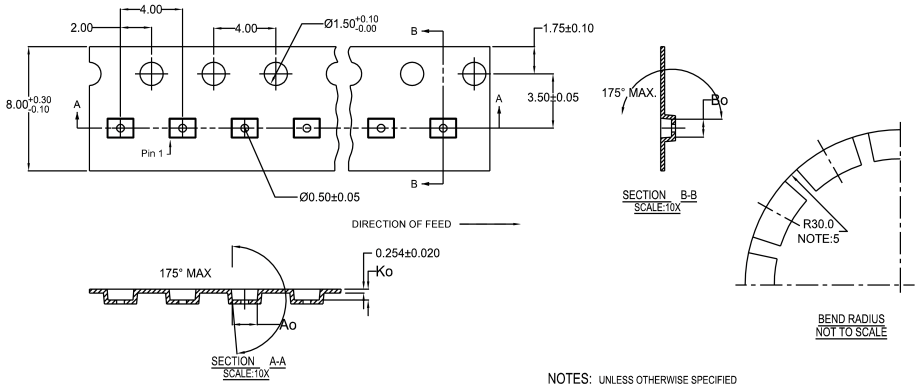


FIGURE 7. Load for DAT_VP, SE0_VM in Receive Mode

Tape and Reel Specification

Tape Format For Micropak 10

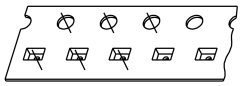
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L10X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed



10	300056	2.30± 0.05	1.78± 0.05	0.68 ± 0.05
8	300038	1.78± 0.05	1.78± 0.05	0.68 ± 0.05
6	300033	1.60± 0.05	1.15± 0.05	0.70 ± 0.05

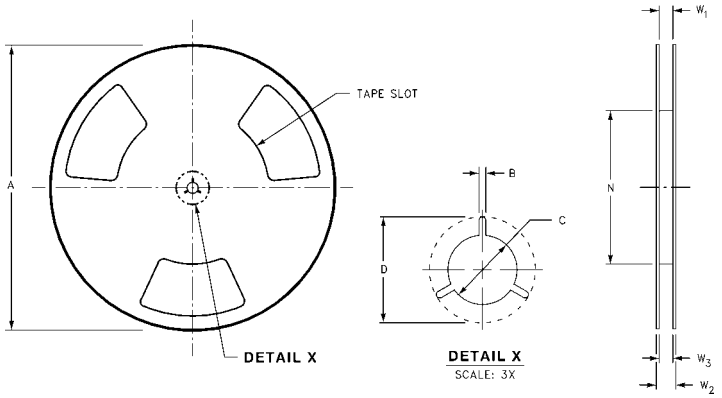
NOTES: UNLESS OTHERWISE SPECIFIED

1. ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ±0.30MM
2. NO INDICATED CORNER RADIUS IS 0.127MM
3. CAMBER NOT TO EXCEED 1MM IN 100MM
4. SMALLEST ALLOWABLE BENDING RADIUS
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



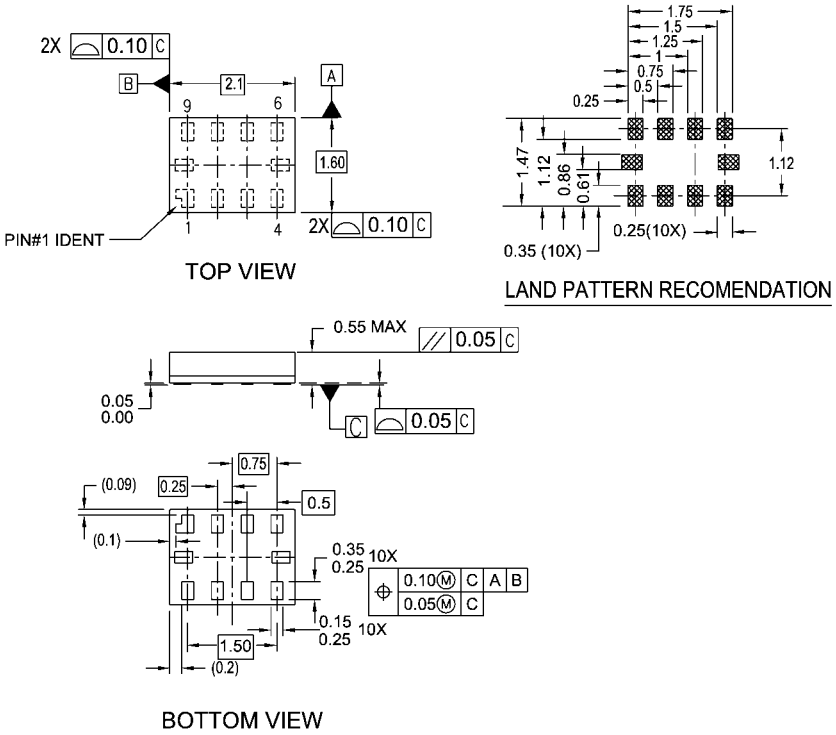
SCALE: 6X

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. PACKAGE CONFORMS TO JEDEC MO255, VARIATION UABD

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES CONFORMS TO ASME Y14.5M, 1994.

MAC010ARevB

10-Lead MicroPak, 1.6 mm x 2.1mm
Package Number MAC010A