V104

PRELIMINARY

10 BIT LVDS RECEIVER FOR VIDEO

General Description

The V104 10 Bit LVDS Receiver for Video is designed to support video data transmission between display engines and video processing engines for television and projector applications. The V104 supports up to WXGA resolutions for Plasma, Rear Projection, Front Projection, CRT and LCD applications.

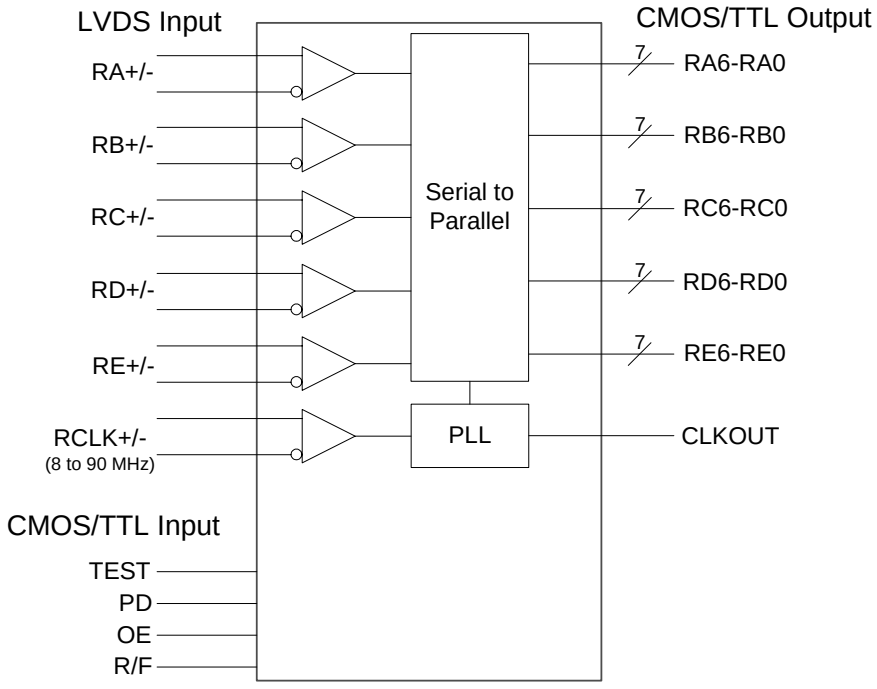
The V104 converts the 6 LVDS (Low Voltage Differential Signaling) video data stream pairs to 35 CMOS/TTL data bits with a rising or falling edge clock. The clock edge selection is performed using a dedicated pin.

In conjunction with the V103 transmitter, the V104 can transmit 10 bits per color (R, G, B) along with 5 bits of control and timing data (HSYNC, VSYNC, DE, CNTL1, CNTL2) over a low EMI, low bus width connection including connectors and standard LVDS cabling.

Features

- Pin & function compatible with the THC63LVD104A
- Wide pixel clock range: 8 - 90 MHz
- Supports resolutions from 480p to WXGA
- Internal PLL does not require external loop filter
- Clock edge selection for TTL alignment selectable
- Power down mode
- Single 3.3V supply
- Low power consumption CMOS design
- 64-pin TQFP lead free package

Block Diagram



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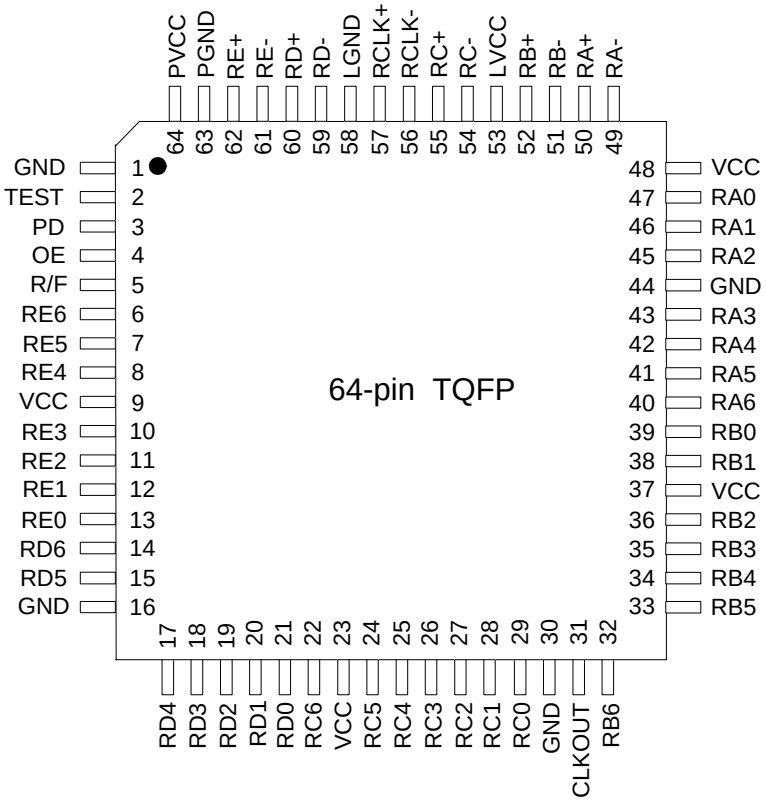
Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
50, 49	RA+, RA-	LVDS IN	LVDS Data In
52, 51	RB+, RB-	LVDS IN	LVDS Data In
55, 54	RC+, RC-	LVDS IN	LVDS Data In
60, 59	RD+, RD-	LVDS IN	LVDS Data In
62, 61	RE+, RE-	LVDS IN	LVDS Data In
57, 56	RCLK+, RCLK-	LVDS IN	LVDS Clock In
40, 41, 42, 43, 45, 46, 47	RA6 ~ RA0	OUT	CMOS/TTL Data Outputs
32, 33, 34, 35, 36, 38, 39	RB6 ~ RB0	OUT	CMOS/TTL Data Outputs
22, 24, 25, 26, 27, 28, 29	RC6 ~ RC0	OUT	CMOS/TTL Data Outputs
14, 15, 17, 18, 19, 20, 21	RD6 ~ RD0	OUT	CMOS/TTL Data Outputs

Pin Number	Pin Name	Pin Type	Pin Description
6, 7, 8, 10, 11, 12, 13	RE6 ~ RE0	OUT	CMOS/TTL Data Outputs.
2	TEST	IN	Not used. Tie LOW.
3	PD	IN	HIGH: normal operation; LOW: Power down (all outputs are “L”).
4	OE	IN	HIGH: Output enable (normal operation); LOW: Output disable (all outputs are high impedance).
5	R/F	IN	Output Clock triggering edge select. High: Rising edge; Low: Falling edge.
9, 23, 37, 48	VCC	Power	Power supply pins for TTL outputs and digital circuitry.
31	CLKOUT	OUT	Clock out.
1, 16, 30, 44	GND	Ground	Ground pins for TTL outputs and digital circuitry.
53	LVCC	Power	Power supply pins for LVDS inputs.
58	LGND	Ground	Ground pins for LVDS inputs.
64	PVCC	Power	Power supply pin for PLL circuitry.
63	PGND	Ground	Ground pin for PLL circuitry.

PD	R/F	OE	Data Outputs (Rxn)	CLKOUT
0	0	0	High impedance	High impedance
0	0	1	All 0	Fixed Low
0	1	0	High impedance	High impedance
0	1	1	All 0	Fixed Low
1	0	0	High impedance	High impedance
1	0	1	Data Out	Latches output data on falling edge
1	1	0	High impedance	High impedance
1	1	1	Data Out	Latches output data on rising edge

**Rxn
x = A, B, C, D, E
n = 0, 1, 2, 3, 4, 5, 6

External Components

The V104 requires no external components.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V104. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VCC	-0.3 V to +4.0 V
CMOS/TTL Input Voltage	-0.3 V to VCC+0.3 V
CMOS/TTL Output Voltage	-0.3 V to VCC+0.3 V
LVDS Receiver Input Voltage	-0.3 V to VCC+0.3 V
Output Current	-30 mA to 30 mA
Storage Temperature	-55 to +125°C
Junction Temperature	125°C
Soldering Temperature (10 seconds)	260°C
Maximum Power Dissipation @ +25°C	1.0 W

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

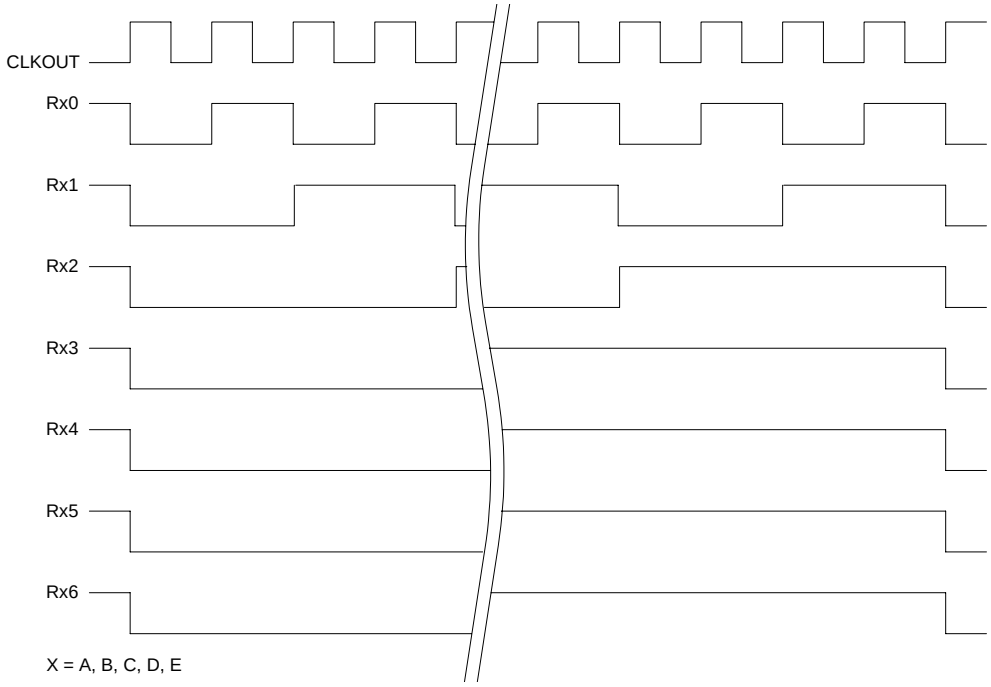
Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature 0 to +70°C

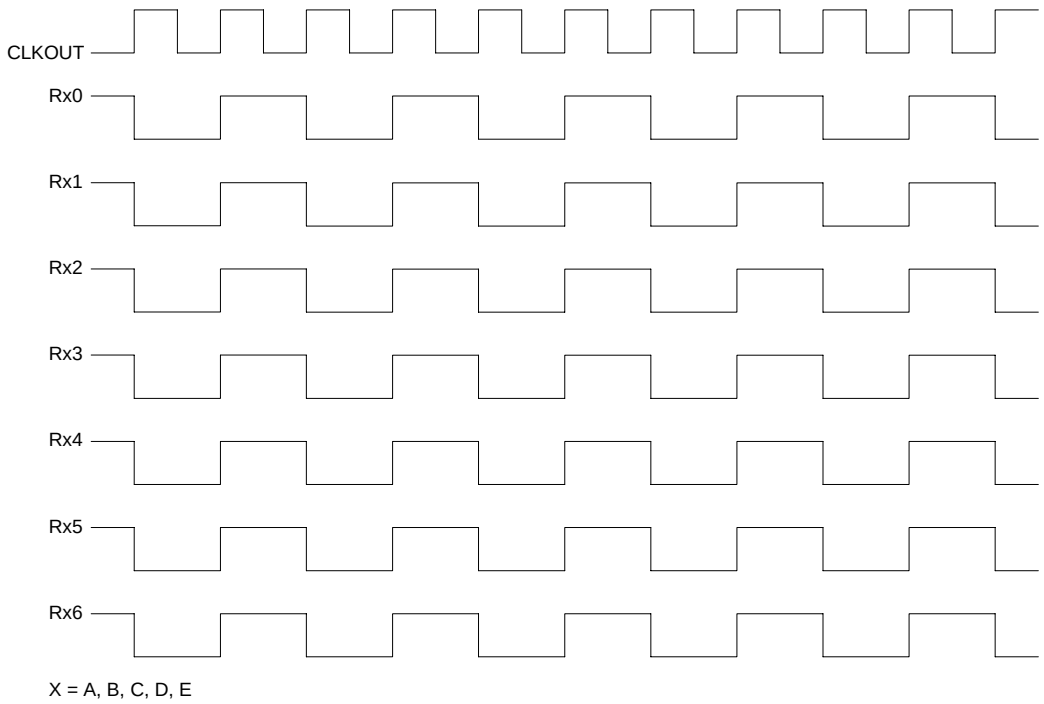
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS/TTL DC Specifications						
Input High Voltage	V_{IH}		2.00		VCC	V
Input Low Voltage	V_{IL}		GND		0.80	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA (data) I_{OH} = -8 mA (clock)	2.4			V
Output Low Voltage	V_{OL}	I_{OH} = -4 mA (data) I_{OH} = -8 mA (clock)			0.4	V
Input Current	I_{INC}	0V≤VIN≤VCC			±10	µA
LVDS Receiver DC Specifications						
Differential Input High Threshold	V_{TH}	V_{OC} = 1.2 V			100	mV
Differential Input Low Threshold	V_{TL}	V_{OC} = 1.2 V	-100			mV
Input Current	I_{INL}	V_{IN} = 2.4 V / 0V V_{IN} = 3.6 V			±20	µA

Parameter	Symbol	Conditions		Typ.	Max.	Units
Supply Current						
Receiver Supply Current (Gray Scale Pattern)	I_{RCCG}	f_{CLKOUT} = 90 MHz	C_L=8 pF, V_{CC} = 3.3 V	70		mA
Receiver Supply Current (Checker Pattern)	I_{RCCW}	f_{CLKOUT} = 90 MHz	C_L=8 pF, V_{CC} = 3.3 V	112		mA
Receiver Power Down Supply Current	I_{RCCS}	PD = L			10	µA

Incremental Pattern (Gray Scale)



Toggle Pattern (Checker)

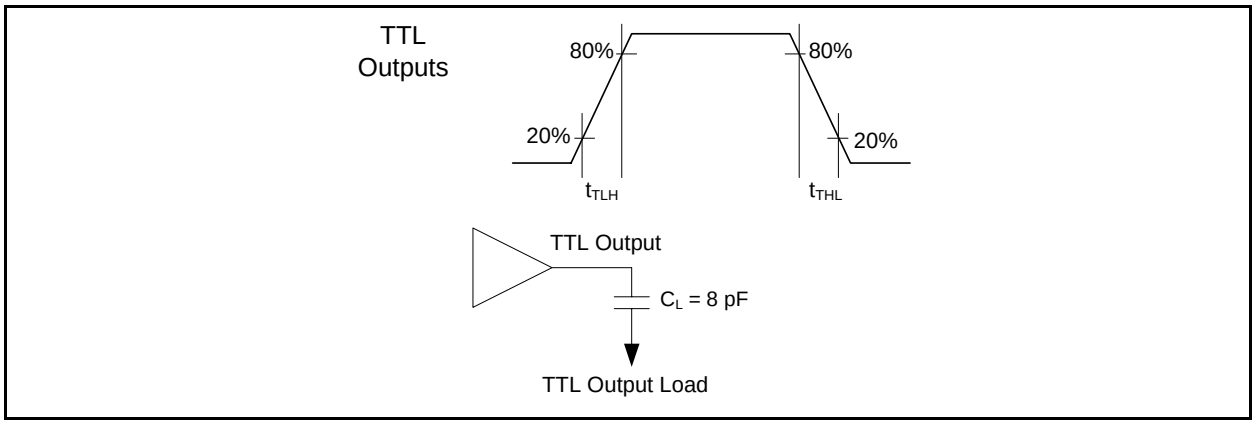


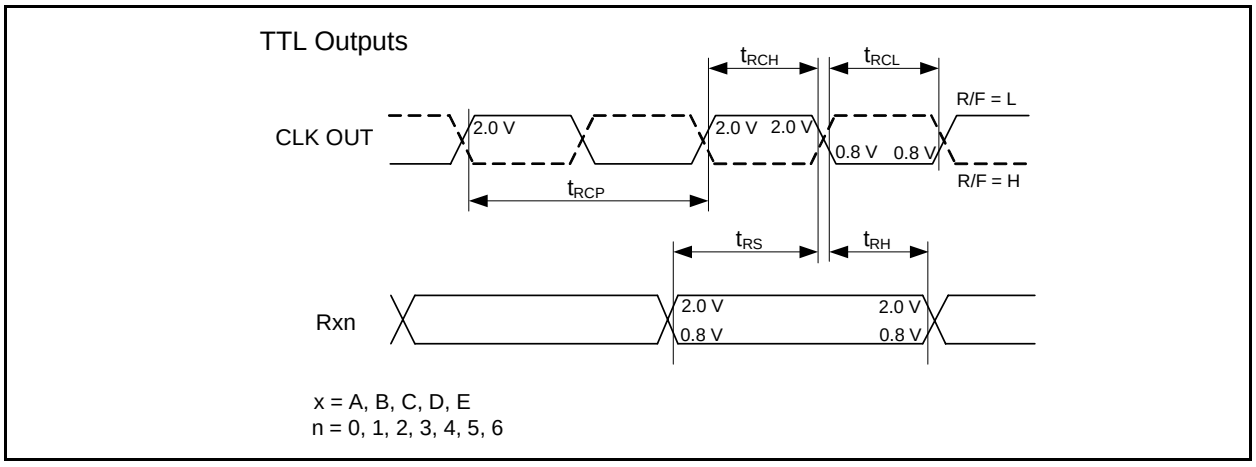
Parameter	Symbol	Min.	Typ.	Max.	Units
Switching Characteristics					
CLKOUT Period	t_{RCP}	11.1	T	125.0	ns
CLK IN High Time	t_{RCH}		(T-1)/2		ns
CLK IN Low Time	t_{RCL}		(T-1)/2		ns
TTL Data Setup to CLKOUT	t_{RS}	4.5			ns
TTL Data Hold from CLKOUT	t_{RH}	2.5			ns
TTL Low to High Transition Time	t_{TLH}		1.0	2.0	ns
TTL High to Low Transition Time	t_{THL}		1.0	2.0	ns
Input Data Position0	t_{RIP1}	-0.25	0.0	+0.25	ns
Input Data Position1	t_{RIP0}	$\frac{t_{RCIP}}{7}$ -0.25	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}$ +0.25	ns
Input Data Position2	t_{RIP6}	$2\frac{t_{RCIP}}{7}$ -0.25	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}$ +0.25	ns
Input Data Position3	t_{RIP5}	$3\frac{t_{RCIP}}{7}$ -0.25	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}$ +0.25	ns
Input Data Position4	t_{RIP4}	$4\frac{t_{RCIP}}{7}$ -0.25	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}$ +0.25	ns
Input Data Position5	t_{RIP3}	$5\frac{t_{RCIP}}{7}$ -0.25	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}$ +0.25	ns
Input Data Position6	t_{RIP2}	$6\frac{t_{RCIP}}{7}$ -0.25	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}$ +0.25	ns
Phase Lock Loop Set	t_{RPLL}			10.0	ms
CLKIN Period	t_{RCIP}	11.1		125.0	ns
Device-device data output skew		0		1.6	ns

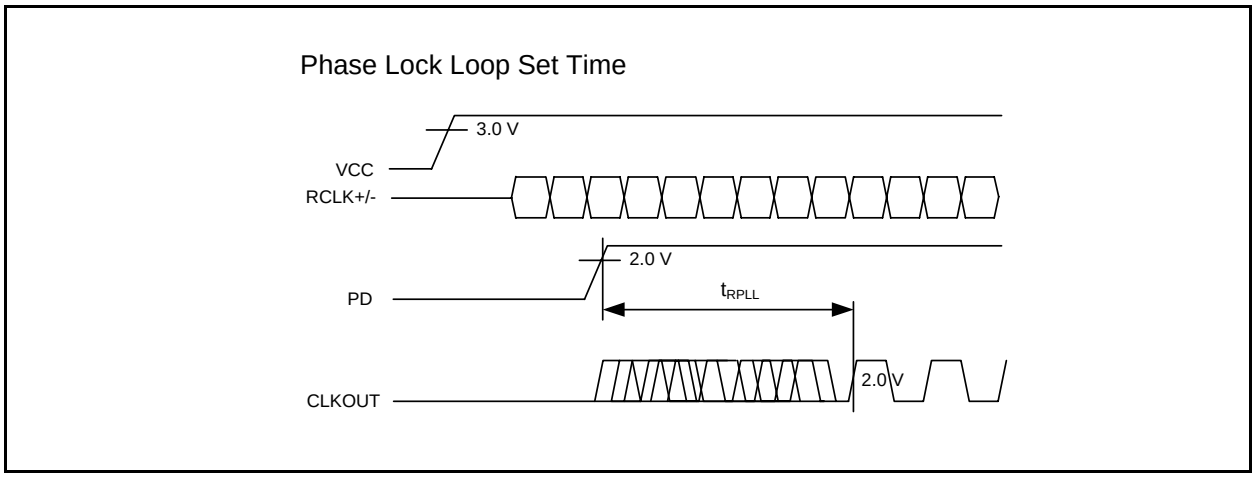
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		53		°C/W
	θ_{JA}	1 m/s air flow		40		°C/W
	θ_{JA}	3 m/s air flow		33		°C/W
Thermal Resistance Junction to Case	θ_{JC}			8		°C/W

AC Timing Diagrams

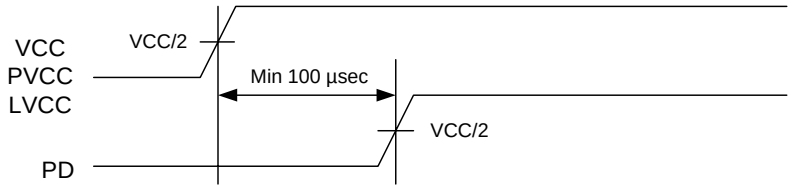




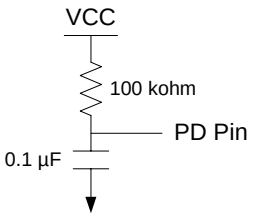


Power Up Sequence

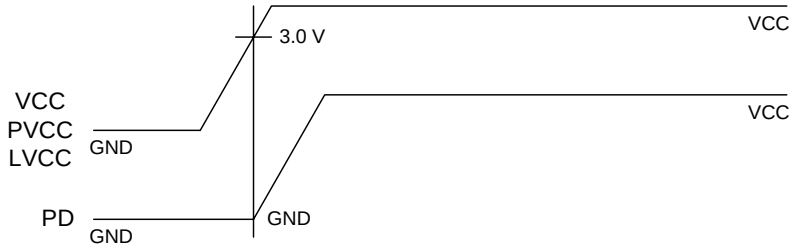
Sequence 1

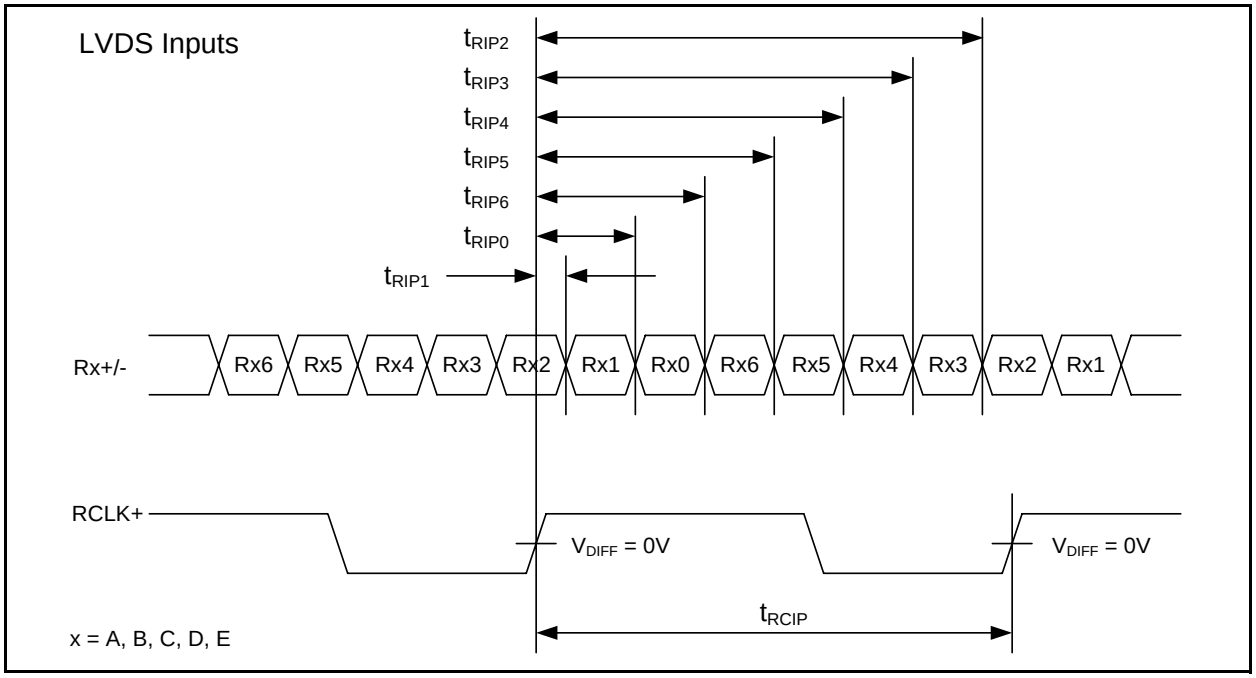


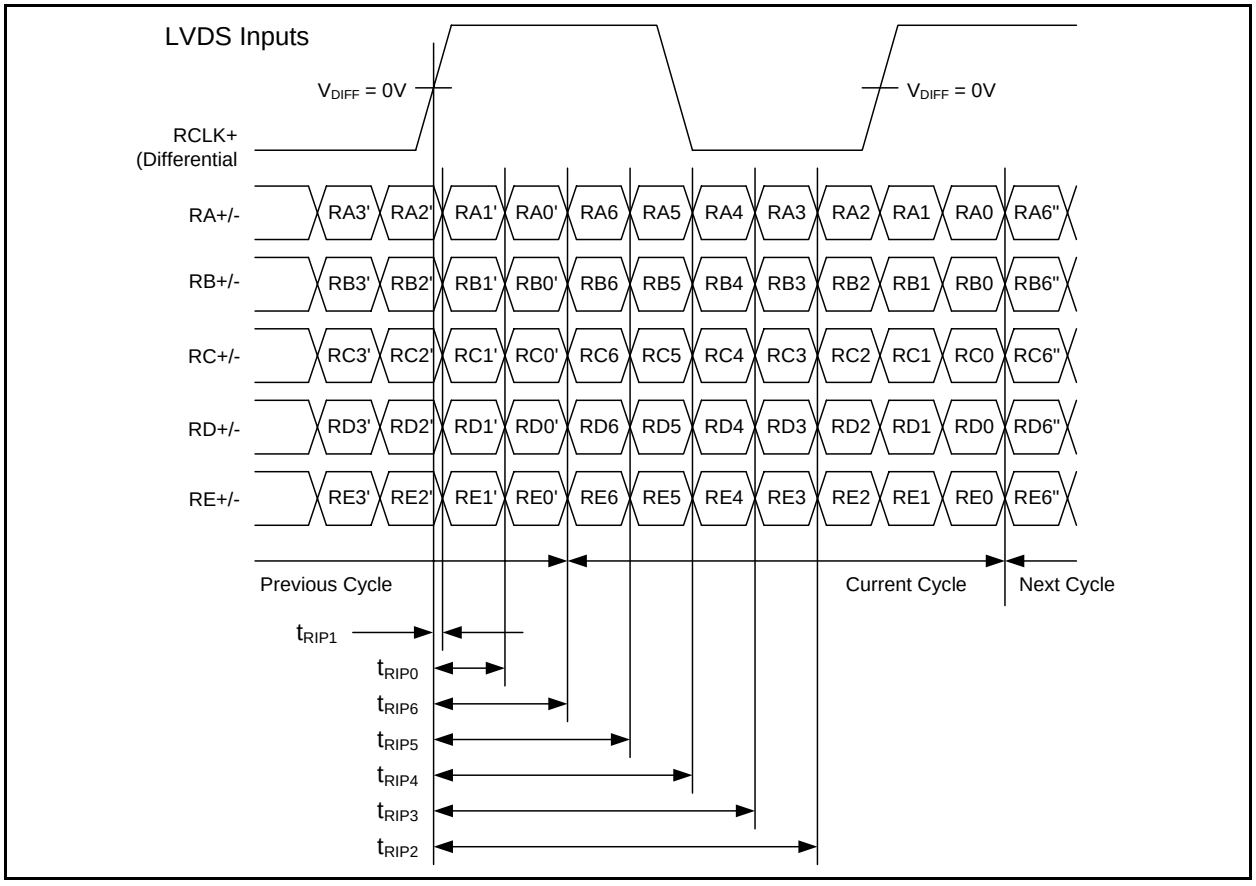
Recommended PD Pin Circuit



Sequence 2







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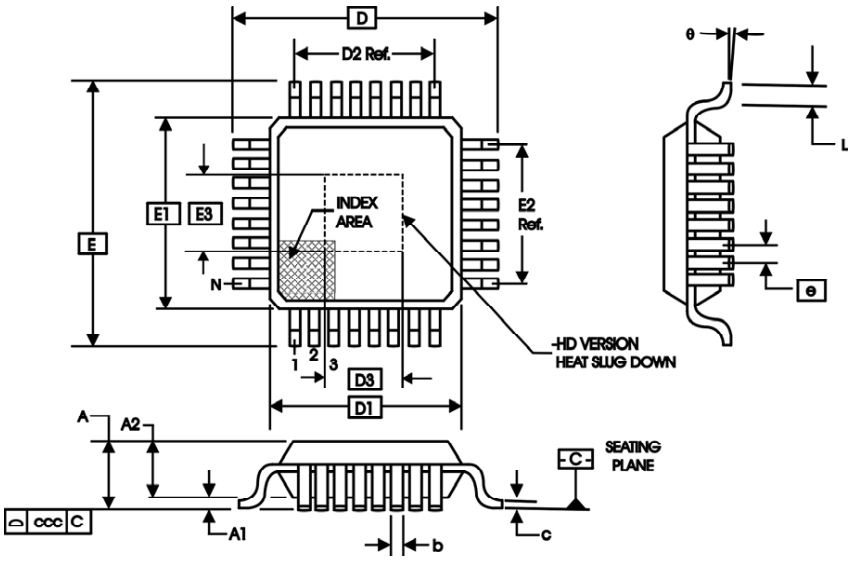
Package Outline and Package Dimensions (64-pin TQFP)

Package dimensions are kept current with JEDEC Publication No. 95, variation ACD.



ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MIN/MAX
N	64
A	-- / 1.20
A1	0.05 / 0.15
A2	0.95 / 1.05
b	0.17 / 0.27
c	0.09 / 0.20
D	12.00 BASIC
D1	10.00 BASIC
D2	7.50 Ref.
E	12.00 BASIC
E1	10.00 BASIC
E2	7.50 Ref.
e	0.50 BASIC
L	0.45 / 0.75
θ	0° / 7°
ccc	-- / 0.08
D3&E3	-

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
V104YLF	V104YLF	Tubes	64-pin TQFP	0 to +70° C
V104YLFT	V104YLF	Tape and Reel	64-pin TQFP	0 to +70° C