Winbond Electronics Corp.

100 MHZ CLOCK FOR BX CHIPSET (2 CHIP)

1. GENERAL DESCRIPTION

The W83196S-14 is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor. Twelve different frequency of CPU, and PCI clocks are externally selectable with smooth transitions.

The W83196S-14 provides I2C serial bus interface to program the registers to enable or disable each clock outputs and choose the 0.5% center type spread spectrum to reduce EMI.

The W83196S-14 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1V/nS slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1V/nS slew rate into 20 pF loads as maintaining 50 ±5% duty cycle. The fixed frequency outputs as REF, 24 MHz, and 48 MHz provide better than 0.5V/nS slew rate.

2. FEATURES

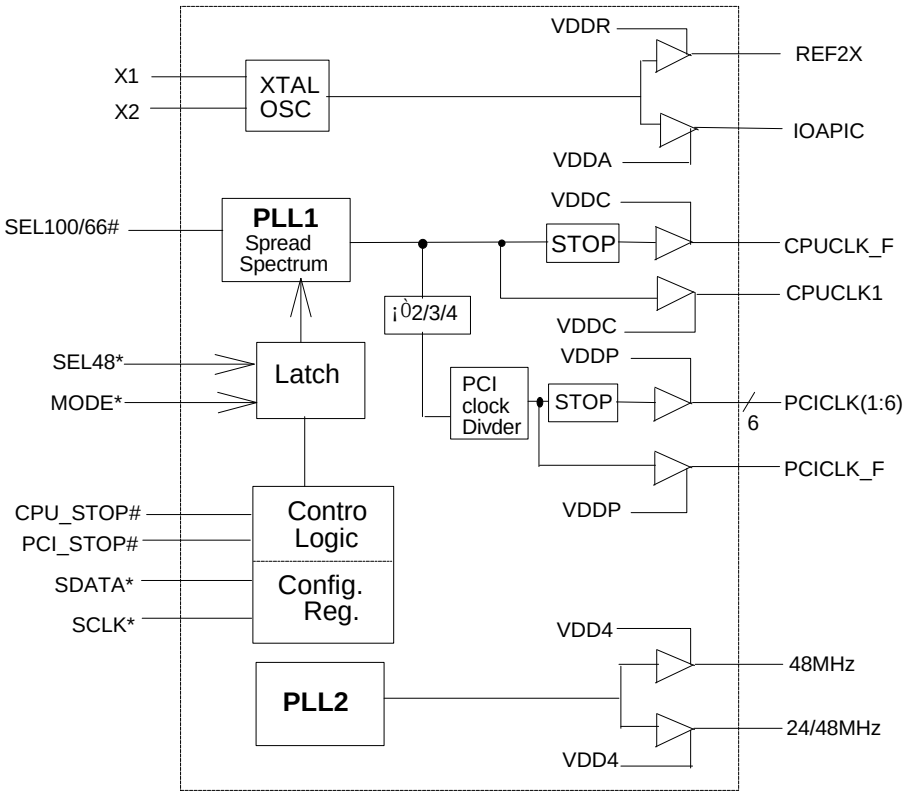
- Supports Pentium™ II CPUs with I^2C
- 12 sets of CPU frequencies selection
- 2 CPU clocks (one free running CPU clock)
- 7 PCI synchronous clocks(one free running PCI clock)
- Optional single or mixed supply:

  ($V_{DD}R$ = $V_{DD}Core$ = $V_{DD}P$ = $V_{DD}4$ = 3.3V ±5%)

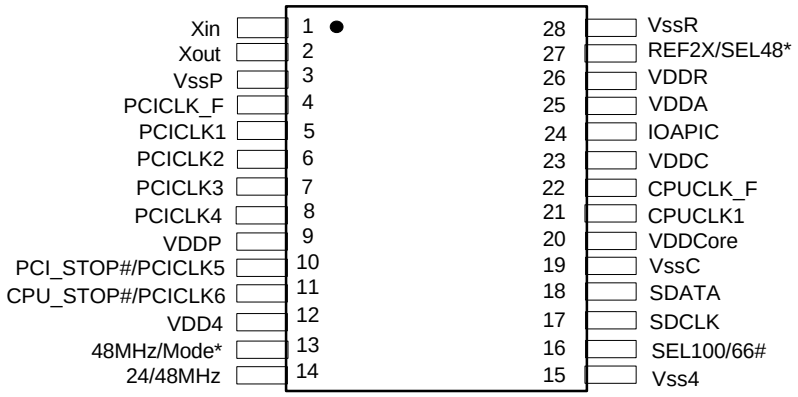
  ($V_{DD}A$ = $V_{DD}C$ = 2.5V ±5%)
- Skew form CPU to PCI clock 1.5 to 4.0 nS, CPU leads.
- CPU clock jitter less than 200 pS
- PCI_F, PCI1: 6 clock skew less than 500 pS
- Smooth frequency switch with selections from 66.8 MHz to 150 MHz CPU
- I^2C 2-Wire serial interface and I^2C read back
- ±0.5% center type spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes

  (mode as Tri-state or Normal)
- MODE pin for power management
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 28-pin SOP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Low active

* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	1	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	2	OUT	Crystal output at 14.318 MHz nominally.

5.2 CPU, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F CPUCLK1	22, 21	OUT	Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset and Cache. VDDC is the supply voltage for these outputs.
PCICLK [1:4] PCICLK_F	4, 5, 6, 7, 8	OUT	Low skew (<250 pS) PCI clock outputs.
PCICLK5/ PCI_STOP#	10	I/O	If Mode* =1 (default), then this pin is a PCICLK5 buffered output of the crystal. If Mode* = 0 , then this pin is PCI_STOP# input used in power management mode for synchronously stopping the all CPU clocks.
PCICLK6/ CPU_STOP#	11	I/O	If Mode* = 1 (default), then this pin is a PCICLK6 clock output. If Mode* = 0 , then this pin is CPU_STOP # and used in power management mode for synchronously stopping the all PCI clocks.

5.3 I2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA*	18	I/O	Serial data of I^2C 2-wire control interface
SDCLK*	17	IN	Serial clock of I^2C 2-wire control interface

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
SEL100/66#	16	IN	CPU clock frequency select pin.
IOAPIC	24	O	Provides 14.318 fixed frequency.
REF2X / SEL48*	27	I/O	Internal 250kΩ pull-up. Latched input for SEL48* at initial power up. SEL48* = 1 , pin14 is 24 MHz SEL48* = 0 , pin14 is 48 MHz Reference clock during normal operation.
24/48MHz	14	O	Frequency is set by the state of pin 27 on power up.
48MHz/Mode*	13	I/O	Internal 250kΩ pull-up. 48 MHz output for USB during normal operation. Latched input for Mode* at initial power up. Mode* = 0 , then pin10 is PCI_STOP#, and pin11 is CPU_STOP#. Mode* = 1.(default), pin10 is PCICLK5 and pin11 is PCLCLK6.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
VDDCore	20	Power supply for core logic and PLL circuitry. Connect to 3.3V supply.
VDDP	9	Power supply for PCICLK_F and PCICLK 1:6. Connect to 3.3V supply.
VDDA	25	Power supply for IOAPIC output, Connect to 2.5V supply
VDDC	23	Power supply for CPUCLK _F and CPUCLK1. Connect to 2.5V supply.
VDD4	12	Power supply for 48mhz USB clock . Connect to 3.3V supply.
VDDR	26	Power supply for 14.318mhz ISA clock . Connect to 3.3V supply.
VssC, VssR, Vss4, VssP	3, 15, 19, 28	Circuit Ground.

6. FREQUENCY SELECTION

SEL100/66#	CPUCLK_F, CPUCLK1	PCI
1	100 MHz	33.3 MHz
0	66.8 MHz	33.3 MHz

7. FUNCTIONAL DESCRIPTION

7.1 Power Mamagement Functions

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCOs to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE = 0, pins 10 and 11 are inputs (PCI_STOP#), (CPU_STOP#), when MODE = 1, these functions are not available. A particular clock could be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enabled.

The W83196S-14 may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPUCLK1	PCICLK1:4	CPUCLK_F& PCICLK_F	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING

7.2 2-Wire I^{2}C Control Interface

The clock generator is a slave I^{2}C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83196S-14 initializes with default register settings, and then it is optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I2C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I2C controller:

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when read back the data sequence is as follows:

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop

7.3 Serial Control Registers

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Register 0 to Register 2 are referred to the Winbond SDRAM buffer(W83178S/179J) drivers.

7.3.1 Register 3: CPU Frequency Select Register (1 = Enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	0	-	Reserved
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by SEL100/66# 1 = Selection by software I^2C - Bit 6:4 and Register 7 Bit0
2	0	-	Reserved
1-0	00	-	Bit1 Bit0 (See Function Table) 0 0 Normal 0 1 Test Mode 1 0 ±0.5% center type Spread Spectrum enabled 1 1 Tristate

(I) Default Frequency table selection by software via I^2C (When Register 7 Bit 0 = 0)

SSEL2	SSEL1	SSEL0	CPU, SDRAM (MHZ)	PCI (MHZ)	REF2X (MHZ)
0	0	0	68.5	34.25	14.318
0	0	1	75	37.5	14.318
0	1	0	83.3	41.6	14.318
0	1	1	66.8	33.4	14.318
1	0	0	103	34.25	14.318
1	0	1	112	37.3	14.318
1	1	0	133.3	44.43	14.318
1	1	1	100	33.3	14.318

(II) Default Frequency table selection by software via I^2C (When Register 7 Bit 0 = 1)

SSEL2	SSEL1	SSEL0	CPU, SDRAM (MHZ)	PCI (MHZ)	REF2X (MHZ)
0	0	0	124	41.3 (CPU/3)	14.318
0	0	1	150	37.5 (CPU/4)	14.318
0	1	0	140	35 (CPU/4)	14.318
0	1	1	133	33.3 (CPU/4)	14.318

FUNCTION TABLE

FUNCTION	OUTPUTS			
Description	CPU	PCI	REF2X	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	See table	See table	14.318	14.318

7.3.2 Register 4 : CPU , 48/24 MHz Clock Register (1 = Enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	0	-	Reserved
6	1	14	24/48 MHz (Active/Inactive)
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	1	21	CPUCLK1 (Active/Inactive)
1	0	-	Reserved
0	1	22	CPUCLK_F (Active/Inactive)

7.3.3 Register 5: PCI Clock Register (1 = Enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	4	PCICLK_F (Active/Inactive)
6	1	11	PCICLK6 (Active/Inactive)
5	1	10	PCICLK5 (Active/Inactive)
4	0	-	Reserved
3	1	8	PCICLK4 (Active/Inactive)
2	1	7	PCICLK3 (Active/Inactive)
1	1	6	PCICLK2 (Active/Inactive)
0	1	5	PCICLK1 (Active/Inactive)

7.3.4 Register 6: IOAPIC and REF2X Clock Register (1 = Enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	0	-	Reserved
6	0	-	Reserved
5	1	24	IOAPIC (Active/Inactive)
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1-0	1 1	27	Bit1 Bit0 REF2X 1 1 Drive strength 2X 1 0 Drive strength 1X 0 1 Drive strength 1X 0 0 Tri-state

7.3.5 Register 7: Additional Register

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	0	-	Frequency select bit for different CPU/PCI frequency table setting by Register3 bit4-bit6 (SSEL0–SSEL2)

8.0 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or V_{DD}).

PARAMETER	SYMBOL	RATING
Voltage on Any Pin with Respect to GND	V_{DD}, V_{IN}	-0.5V to +7.0V
Storage Temperature	T_{STG}	-65° C to +150° C
Ambient Temperature	T_B	-55° C to +125° C
Operating Temperature	T_A	0° C to +70° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 AC Characteristics

$V_{DD}R = V_{DD}Core = V_{DD}P = V_{DD}4 = 3.3V \pm 5\%$, $V_{DD}A = V_{DD}C = 2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU to PCI Offset	t_{OFF}	1		4	nS	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
Cycle to Cycle Jitter	t_{CCJ}			200	ps	
CPU Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	nS	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V_{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

8.3 DC Characteristics

$V_{DD}R = V_{DD}Core = V_{DD}P = V_{DD}4 = 3.3V \pm 5\%$, $V_{DD}A = V_{DD}C = 2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-25	µA	
Input High Current	I_{IH}			10	µA	
Output Low Voltage I_{OL} = 1 mA	V_{OL}			50	mV_{dc}	CPU_F, CPU1
Output High Voltage I_{OH} = -1 mA	V_{OH}	3.1			V_{dc}	CPU_F, CPU1
Output Low Current	I_{OL}	27	57	97	mA	CPU_F,CPI1
		20.5	53	139	mA	PCI_F,PCI1:6
		40	85	140	mA	IOAPIC
		50	74	152	mA	REF2X
		25	37	76	mA	48,24 MHz
Output High Current	I_{OH}	25	55	97	mA	CPU_F,CPI1
		31	55	189	mA	PCI_F,PCI1:6
		40	87	155	mA	IOAPIC
		54	88	188	mA	REF2X
		27	44	94	mA	48,24 MHz

8.4 Buffer Characteristics

8.4.1 Type 1 Buffer for CPUCLK_F and CPUCLK1

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	I_{OH} (min)	-27			mA	Vout = 1.0V
Pull-up Current Max.	I_{OH} (max)			-27	mA	Vout = 2.0V
Pull-down Current Min.	I_{OL} (min)				mA	Vout = 1.2V
Pull-down Current Max.	I_{OL} (max)			27	mA	Vout = 0.3V
Rise/Fall Time Min. Between 0.4V and 2.0V	T_{RF} (min)	0.4			nS	10 pF Load
Rise/Fall Time Max. Between 0.4V and 2.0V	T_{RF} (max)			1.6	nS	20 pF Load

8.4.2 Type 2 Buffer for IOAPIC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	I_{OH} (min)				mA	Vout = 1.4V
Pull-up Current Max.	I_{OH} (max)			-29	mA	Vout = 2.7V
Pull-down Current Min.	I_{OL} (min)				mA	Vout = 1.0V
Pull-down Current Max.	I_{OL} (max)			28	mA	Vout = 0.2V
Rise/Fall Time Min. Between 0.7V and 1.7V	T_{RF} (min)	0.4			nS	10 pF Load
Rise/Fall Time Max. Between 0.7V and 1.7V	T_{RF} (max)			1.8	nS	20 pF Load

8.4.3 Type 3 Buffer for REF2X, 24 MHz, 48 MHz

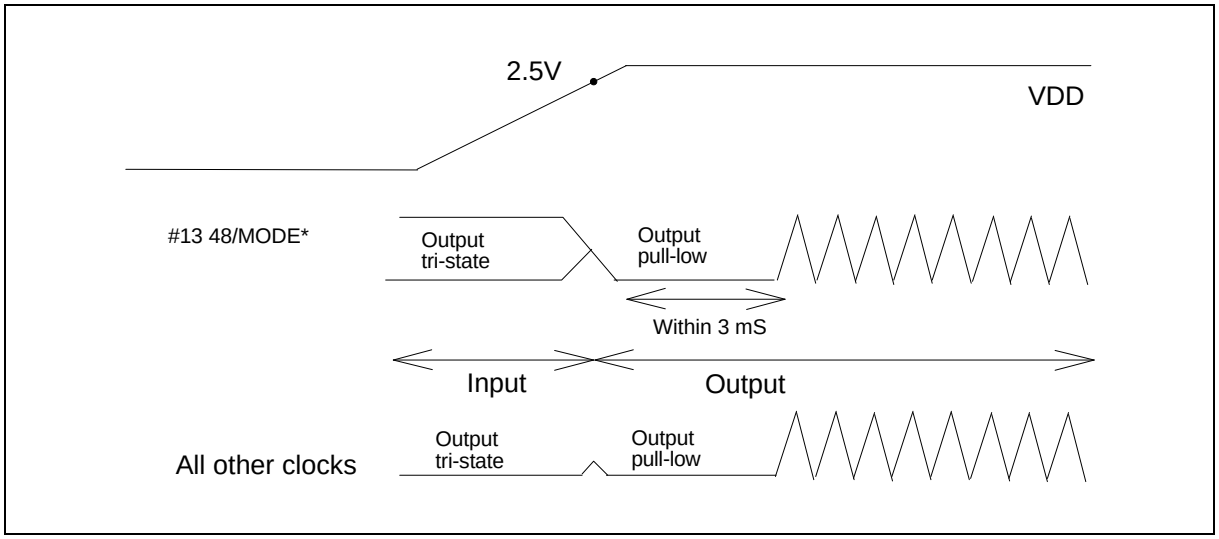
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	I_{OH} (min)	-29			mA	Vout = 1.0 V
Pull-up Current Max.	I_{OH} (max)			-23	mA	Vout = 3.135V
Pull-down Current Min.	I_{OL} (min)	29			mA	Vout = 1.95 V
Pull-down Current Max.	I_{OL} (max)				mA	Vout = 0.4 V
Rise/Fall Time Min. Between 0.8V and 2.0V	T_{RF} (min)	1.0			nS	10 pF Load
Rise/Fall Time Max. Between 0.8V and 2.0V	T_{RF} (max)			4.0	nS	20 pF Load

8.4.4 Type 5 Buffer for PCICLK (1:6,F)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	I_{OH} (min)	-33			mA	Vout = 1.0V
Pull-up Current Max.	I_{OH} (max)			-33	mA	Vout = 3.135V
Pull-down Current Min.	I_{OL} (min)	30			mA	Vout = 1.95V
Pull-down Current Max.	I_{OL} (max)			38	mA	Vout = 0.4V
Rise/Fall Time Min. Between 0.8V and 2.0V	T_{RF} (min)	0.5			nS	15 pF Load
Rise/Fall Time Max. Between 0.8V and 2.0V	T_{RF} (max)			2.0	nS	30 pF Load

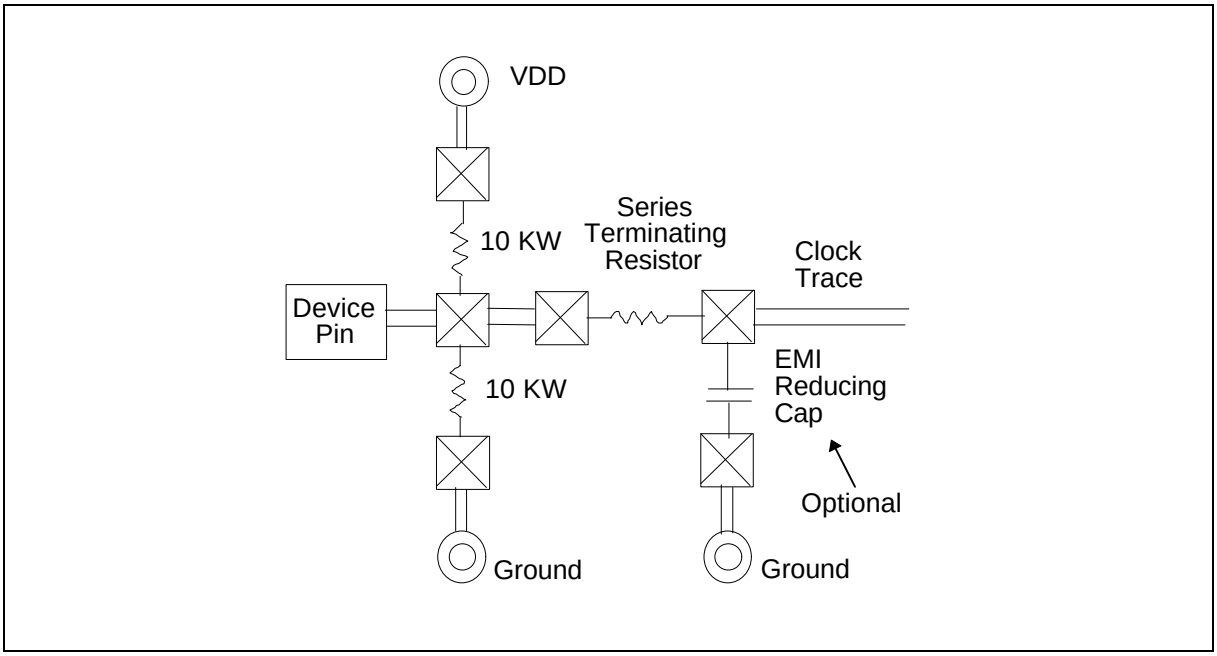
9. OPERATION OF DUAL FUCTION PINS

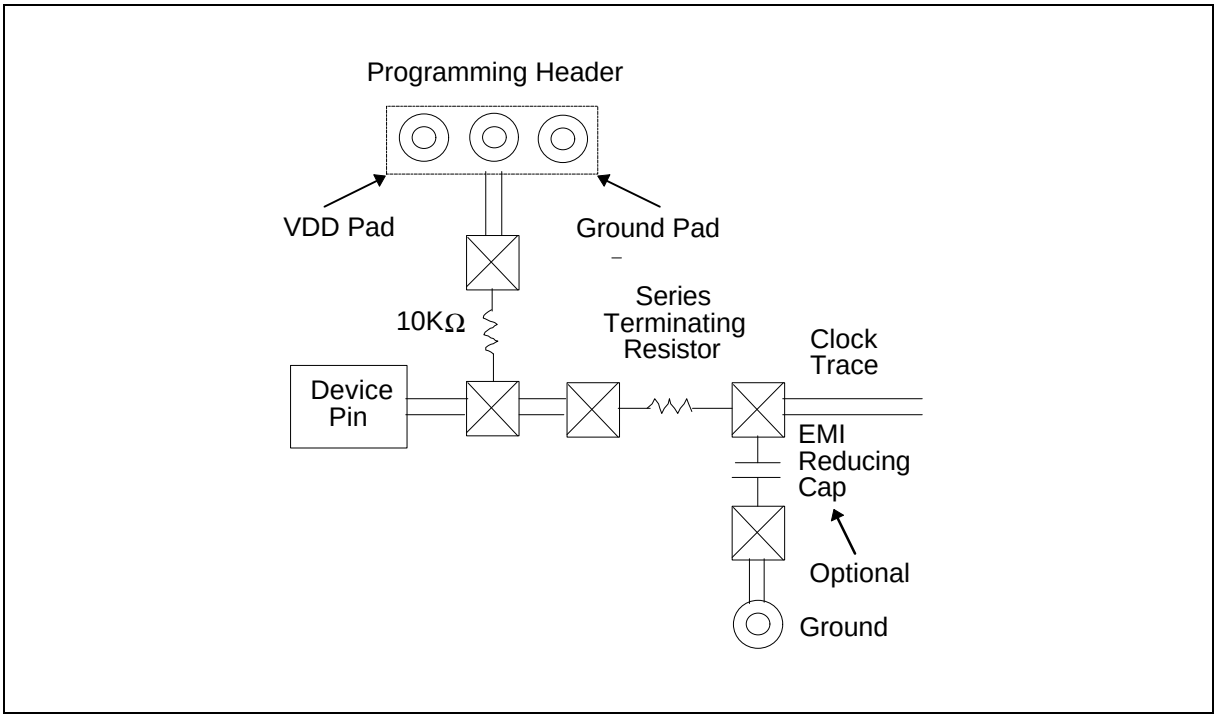
Pin13 is dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Figure 1), therefore, and are considered input select pins. When VDD reaches 2.5V, the logic level that is present on these pins are latched into their appropriate internal registers. Once the correct information are properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins are a large pull-up resistor (250 KΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 KΩ resistor is recommended to be connected to VDD if logic 1 is expected. The same 10 KΩ connection to ground if a logic 0 is desired. The 10 KΩ resistor should be place before the serious terminating resistor. Note that these logic will only be latched at initial power on.

If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitor has typical values ranging from 4.7 pF to 22 pF.

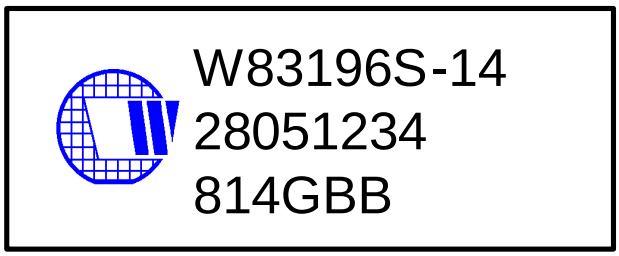

VDD
10 KW
Series
Terminating
Resistor
Clock
Trace
Device
Pin
EMI
Reducing
Cap
10 KW
Optional
Ground
Ground


Programming Header
VDD Pad
Ground Pad
10KΩ
Series
Terminating
Resistor
Clock
Trace
Device
Pin
EMI
Reducing
Cap
Optional
Ground

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83196S-14	28-pin SOP	Commercial, 0° C to +70° C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83196S-14

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

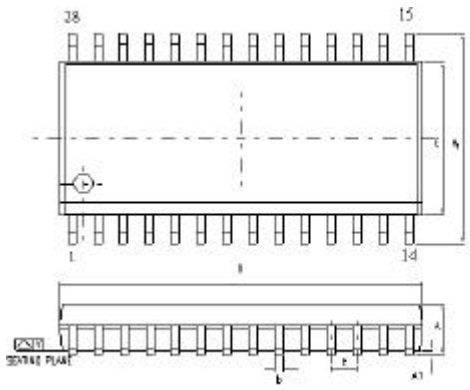
814: packages made in '98, week 14

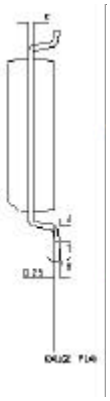
G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

12. PACKAGE DIMENSIONS

28-pin SOP





Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	17.70	18.10	0.697	0.713
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

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