



# 128K x 8 Static RAM

## Features

- **High speed**  
— $t_{AA} = 15 \text{ ns}$
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options**

## Functional Description

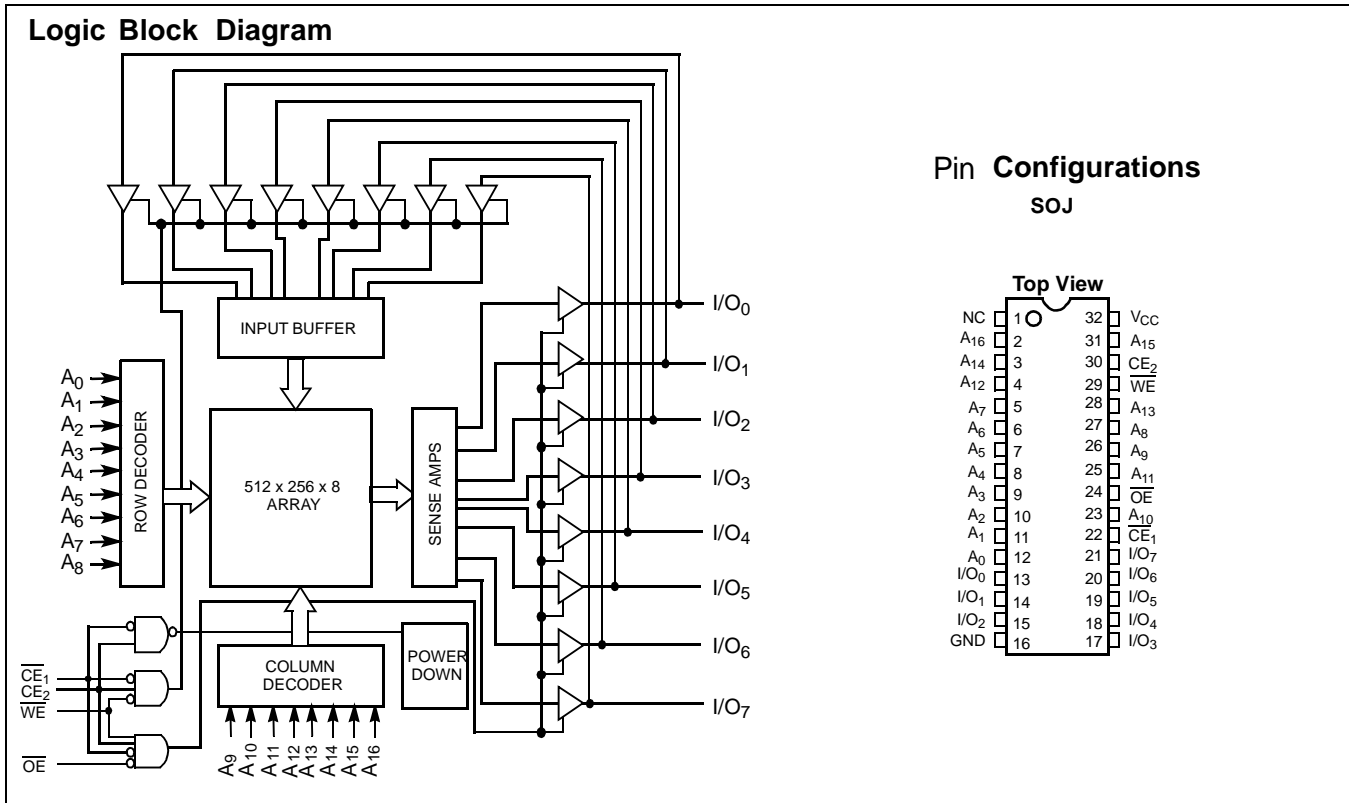
The WCF1008C3E and WCFS1008C9E are high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and Chip Enable

Two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable Two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The WCFS1008C3E is available in standard 300-mil-wide SOJ. The WCFS1008C9E is available in standard 400-mil-wide SOJ. The WCFS1008C3E and WCFS1008C9E are functionally equivalent in all other respects..



## Selection Guide

	WCFS1008C3E	WCFS1008C9E 15ns
Maximum Access Time (ns)		15
Maximum Operating Current (mA)		80
Maximum CMOS Standby Current (mA)		10



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	WCFS1008C3E WCFS1008C9E 15ns		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		80	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10	mA

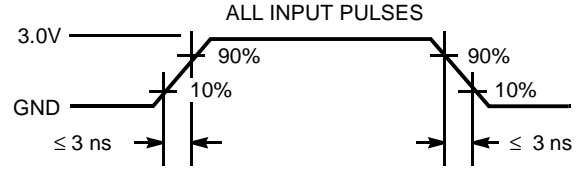
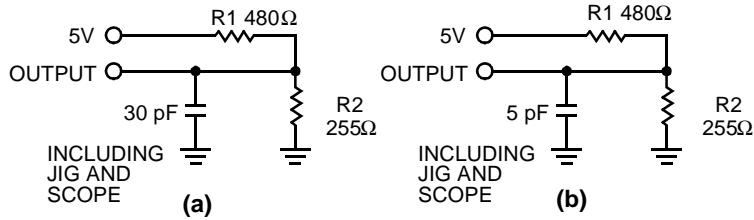
**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT  
 OUTPUT  $\text{---} \frac{167\Omega}{\text{---}} \text{---} 1.73\text{V}$

### Switching Characteristics<sup>[5]</sup> Over the Operating Range

Parameter	Description	WCFS1008C3E WCFS1008C9E-15		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	15		ns
$t_{AA}$	Address to Data Valid		15	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		7	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[7]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[6, 7]</sup>		7	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		15	ns
<b>WRITE CYCLE<sup>[8]</sup></b>				
$t_{WC}$	Write Cycle Time <sup>[9]</sup>	15		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	12		ns
$t_{AW}$	Address Set-Up to Write End	12		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		ns
$t_{SD}$	Data Set-Up to Write End	8		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		7	ns

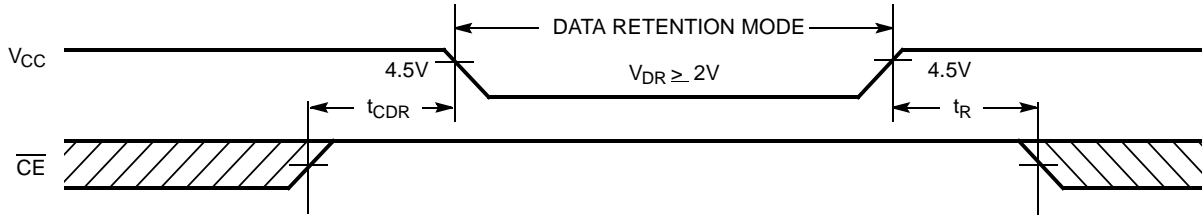
**Note:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range

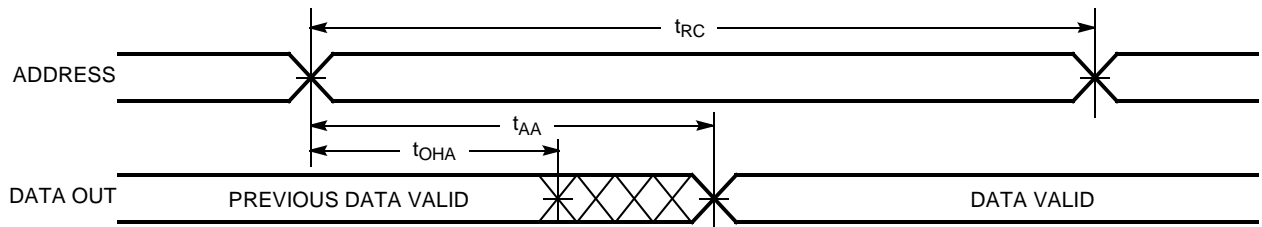
Parameter	Description	Conditions	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	No input may exceed $V_{CC} + 0.5V$	2.0		V
$t_{CDR}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$ , $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ ,	0		ns
$t_R$	Operation Recovery Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	200		$\mu s$

**Data Retention Waveform**

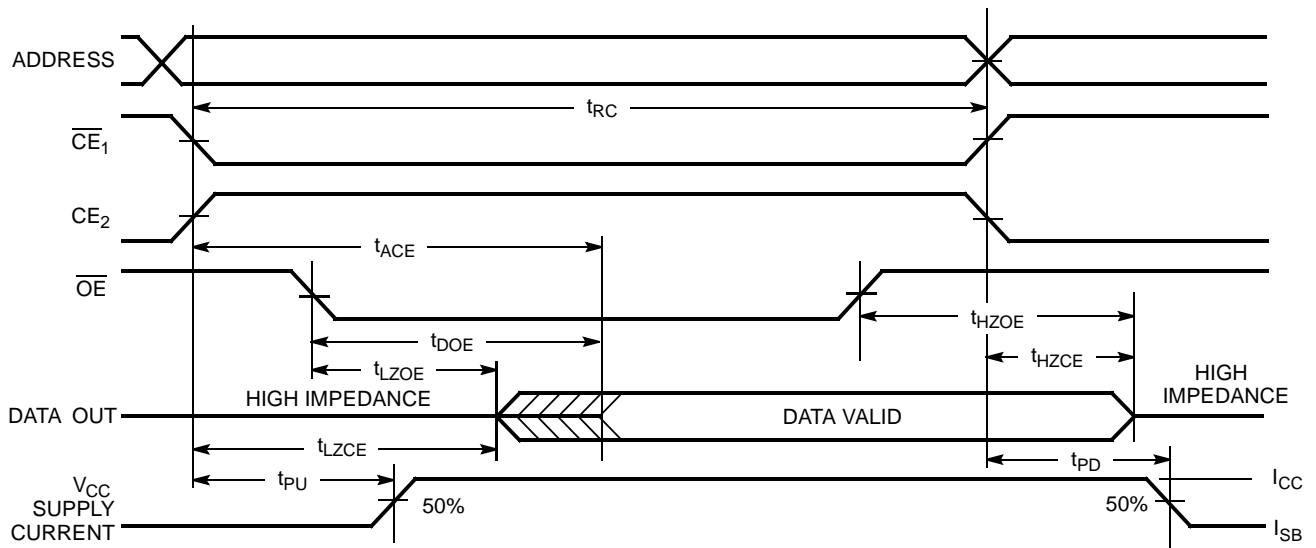


**Switching Waveforms**

**Read Cycle No. 1**<sup>[10, 11]</sup>



**Read Cycle No. 2 (OE Controlled)**<sup>[11, 12]</sup>

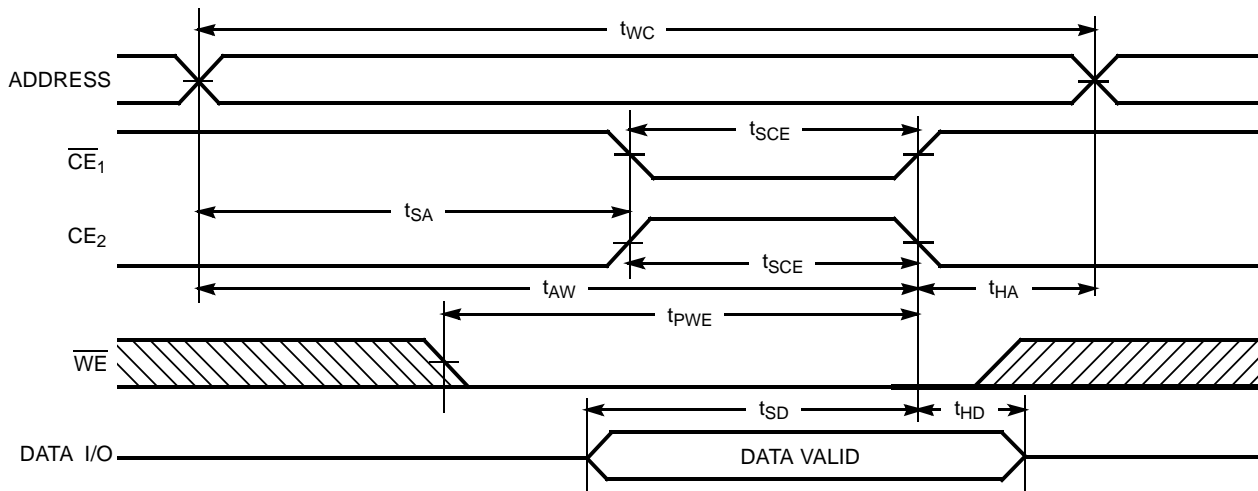


**Note:**

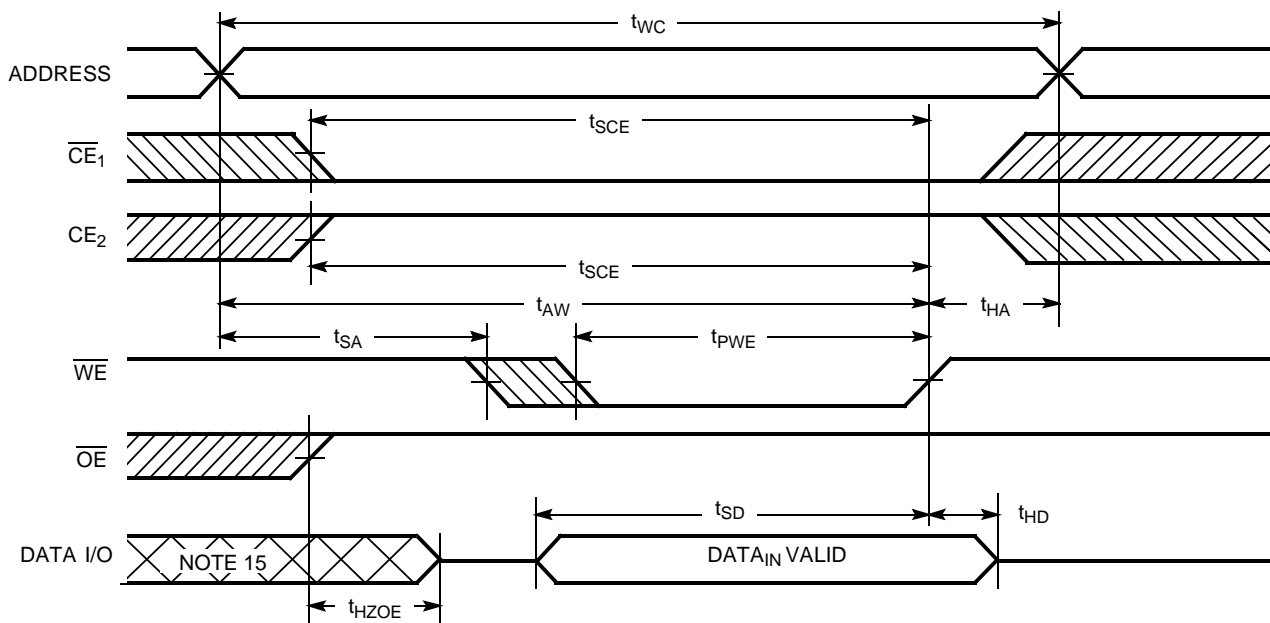
- 10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_L$ ,  $CE_2 = V_{IH}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms** (continued)

**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[10, 14]</sup>**



**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[10, 14]</sup>**

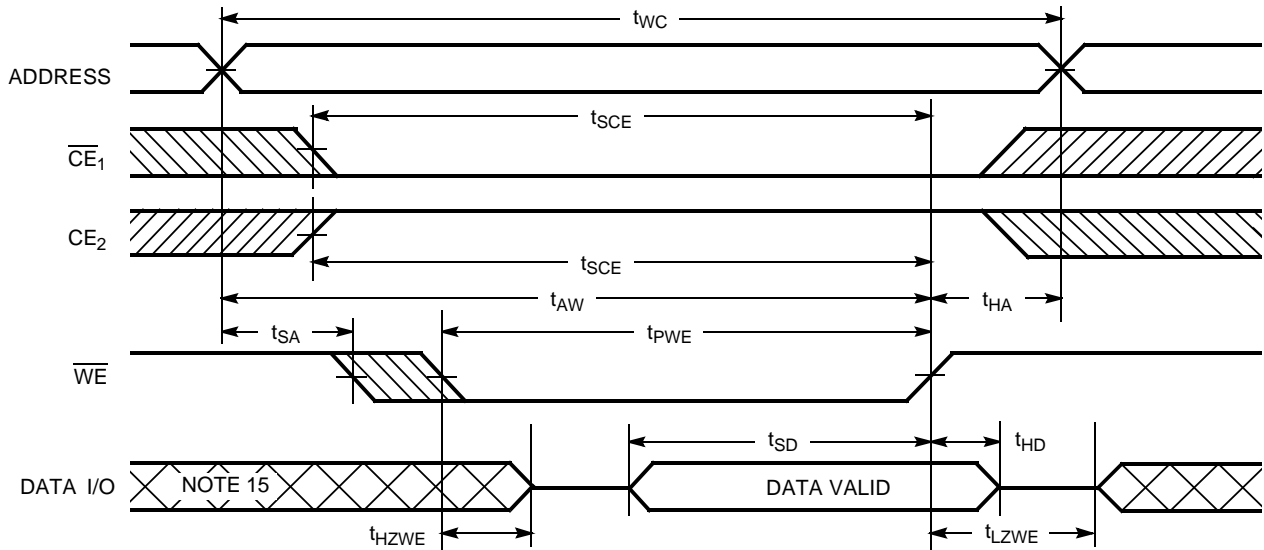


**Notes:**

- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>**



**Truth Table**

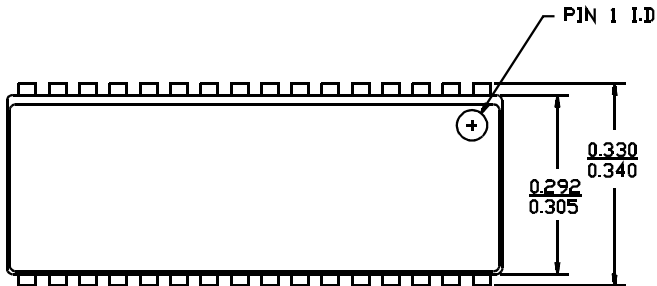
$CE_1$	$CE_2$	OE	WE	I/O <sub>0</sub> - I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

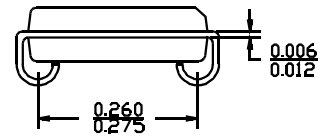
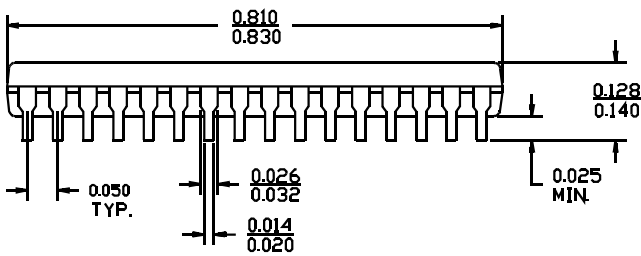
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	WCFS1008C3E-JC15	J	32-Lead (300-Mil) Molded SOJ	Commercial
	WCFS1008C9E-JC15	J	32-Lead (400-Mil) Molded SOJ	

Package Diagrams

32-Lead (300-Mil) Molded SOJ J

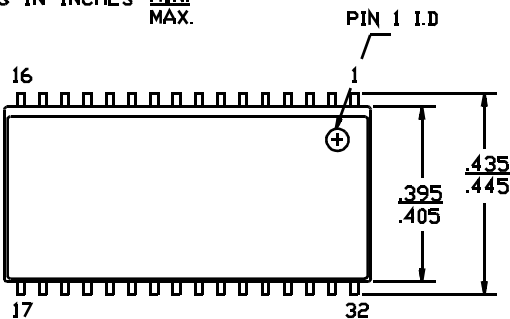


DIMENSIONS IN INCHES MIN.  
MAX.  
LEAD COPLANARITY 0.004 MAX.

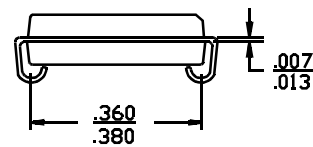
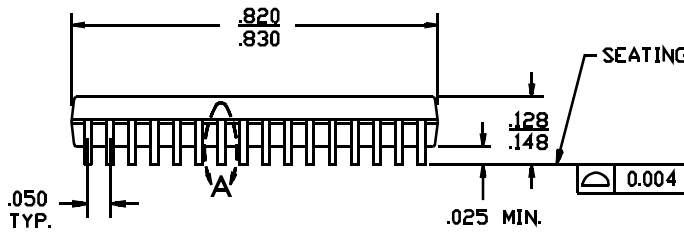
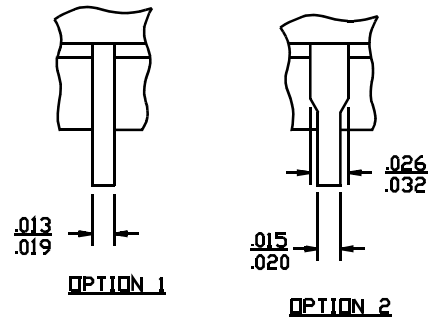


32-Lead (400-Mil) Molded SOJ J

DIMENSIONS IN INCHES MIN.  
MAX.



DETAIL A  
EXTERNAL LEAD DESIGN





<b>Document Title: WCFS1008C3E WCFS1008C9E 128K x 8 SRAM</b>			
<b>REV.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	4/12/02	XFL	NEW DATASHEET