DIMMDrive Solid State ATA Flash Module

FEATURES

- 144 Pin SO-DIMM, JEDEC package
- Plug-and-play solid state disk
- NAND Flash memory technology by SanDisk
- PC CARD ATA compatible - memory mapped or I/O operation
- 3.3 volt & 5.0 volt power supply operation
- 16MB - 768MB memory density
  - (1GB - Q3/02)
- Low Power Consumption
- ECC error correction
- Supports true IDE mode
- 8Kbyte data buffers
- Broad O/S support: DOS, Linux, Windows 3.X, Windows 95, Windows NT4.0/5.0, Windows CE, others
- Compatible with major processors: x86, Media GX, PowerPC, 68K, MIPS, SHx, StrongArm, others
- Full Hard Disk emulation and Boot capability
- Easy to use interface, JEDEC standard
- Supports power down commands and sleep modes
- Commercial temperature range 0C + 70C
- Industrial temperature range -40C +85C

MODULE APPLICATIONS

Embedded systems

Internet Access Devices

Set Top Boxes

WEB Browser

Routers, Networking

WEB phones, car PC, DVD, HPC

Point-of-sale

Medical and Telecom

Other applications requiring embedded or solid state storage

* This datasheet is preliminary, therefore all specifications are subject to change without notice.

DESCRIPTION

The DIMMDrive WED7GxxxATA33 is a high performance single chip flash disk module available in 144 Pin SO-DIMM package. The module is based on SanDisk NAND Flash technology and utilizes the 128Mb, 256Mb, 512Mb or 1Gb memory components to provide the maximum in module density.

The DIMMDrive WED7GxxxATA33 utilizes a SanDisk Flash ChipSet controller which is designed specifically for use as a Flash mass storage controller for the SanDisk memory devices. This interface allows a host computer to issue commands to read or write blocks of memory in the Flash memory array. The intelligence to manage the interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics are controlled by this device. Automatic power management and clock control is handled by the controller as well.

The DIMMDrive WED7GxxxATA33 module will have the same functionality and capabilities of an intelligent ATA (IDE) disk drive. An advantage of the on board Flash controller and it's ATA command set, is the ease of software development by the user. Once the device has been configured by the user, it appears to the host as a standard ATA disk drive. Additional ATA commands have been provided to enhance the system performance.

The on-board controller is a highly integrated solution and the controller is designed to handle all intelligent operations, even the rare cases when new defects arise and need to be mapped out or replaced by a spare. The hardware performs the complicated task of ECC detection and correction and will return good data to the host. The controller manages all defects and errors and makes the Flash memory appear as perfect memory to the host.

The DIMMDrive WED7GxxxATA33 module also provides a more cost effective solution to the traditional hard disk media. The module is perfect for applications requiring upgradeability to higher densities and for those applications with limited space availability and power consumption requirements.

Unlike standard IDE drives, no cables or extra space is required. The module has no moving parts providing significant reduction in power consumption and increasing reliability. Simply insert the module into a standard 144 Pin SO-DIMM socket and you then have a bootable flash disk.

The DIMMDrive WED7GxxxATA33 is available with memory densities of 16MB to 768MB today with 1GB density available in Q3/02.

MODULE PINOUT

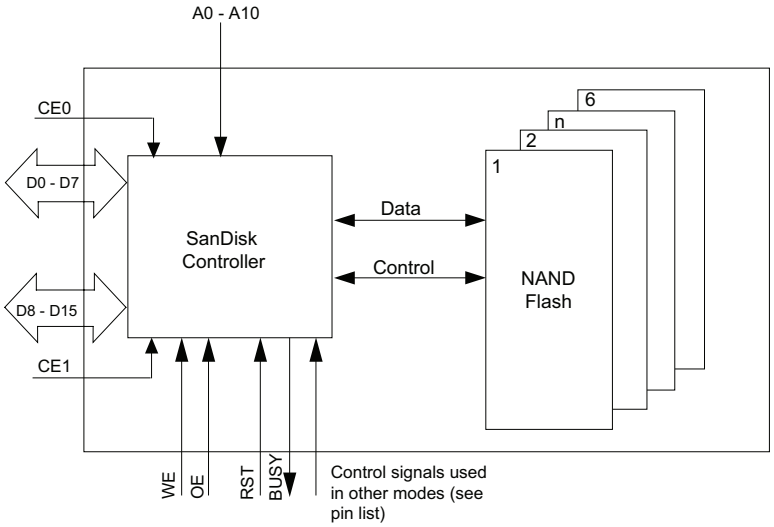
PIN	SIGNAL	NOTE	PIN	SIGNAL	NOTE	PIN	SIGNAL	NOTE	PIN	SIGNAL	NOTE
1	V_{SS}		37	DQ8	1	73	OE#		109	A0	2
2	V_{SS}		38	Reserved		74	IO16	3	110	NC	
3	DQ0		39	DQ9	1	75	V_{SS}		111	A10	4
4	Reserved		40	Reserved		76	V_{SS}		112	Reserved	
5	DQ1		41	DQ10	1	77	Reserved		113	V_{CC}	
6	Reserved		42	Reserved		78	Reserved		114	V_{CC}	
7	DQ2		43	DQ11	1	79	Reserved		115	Reserved	
8	Reserved		44	Reserved		80	Reserved		116	Reserved	
9	DQ3		45	V_{CC}		81	V_{CC}		117	Reserved	
10	Reserved		46	V_{CC}		82	V_{CC}		118	Reserved	
11	V_{CC}		47	DQ12	1	83	Reserved		119	V_{SS}	
12	V_{CC}		48	Reserved		84	Reserved		120	V_{SS}	
13	DQ4		49	DQ13	1	85	Reserved		121	Reserved	
14	Reserved		50	Reserved		86	Reserved		122	Reserved	
15	DQ5		51	DQ14	1	87	Reserved		123	Reserved	
16	Reserved		52	Reserved		88	Reserved		124	Reserved	
17	DQ6		53	DQ15	1	89	Reserved		125	Reserved	
18	Reserved		54	Reserved		90	Reserved		126	Reserved	
19	DQ7		55	V_{SS}		91	V_{SS}		127	Reserved	
20	Reserved		56	V_{SS}		92	V_{SS}		128	Reserved	
21	V_{SS}		57	Reserved		93	Reserved		129	V_{CC}	
22	V_{SS}		58	Reserved		94	Reserved		130	V_{CC}	
23	CE0#		59	Busy	4	95	Reserved		131	Reserved	
24	Reserved		60	NC		96	Reserved		132	Reserved	
25	CE1#	1	61	BVD1	3	97	Reserved		133	Reserved	
26	Reserved		62	BVD2	3	98	Reserved		134	Reserved	
27	V_{CC}		63	V_{CC}		99	Reserved		135	Reserved	
28	V_{CC}		64	V_{CC}		100	Reserved		136	Reserved	
29	A0		65	RST	4	101	V_{CC}		137	Reserved	
30	A3		66	IOWR	3	102	V_{CC}		138	Reserved	
31	A1		67	WE#		103	A6	2	139	V_{SS}	
32	A4	2	68	IORD	3	104	A7	2	140	V_{SS}	
33	A2		69	Reserved		105	A8	2	141	Reserved	
34	A5	2	70	REG	3	106	NC		142	Reserved	
35	V_{SS}		71	Reserved		107	V_{SS}		143	V_{CC}	
36	V_{SS}		72	INPACK	3	108	V_{SS}		144	V_{CC}	

Note: 1.) 16-Bit bus mode signals not used (floating) in 9-bit mode
CE1# signal in 16-bit only mode should be tied to CE0#
2.) Optional addresses, do not have to be connected for module use in Memory Mapped Mode
3.) Optional test signals not used in Memory Mapped Mode
4.) Busy, RST and A10 signals are optional in Memory Mapped Mode
NC - pins internally not connected

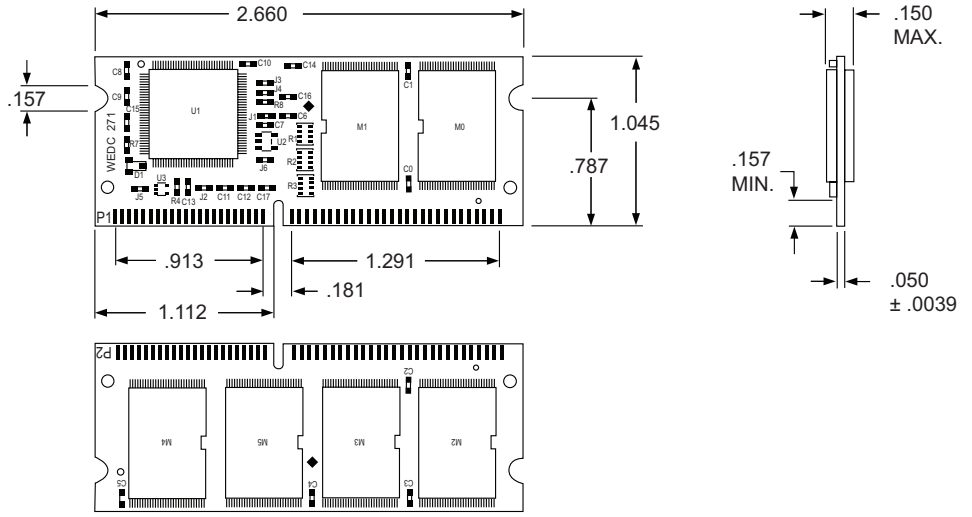
SIGNAL DESCRIPTION

Signal Name	Description
DQ0-DQ7, DQ8-DQ15	Data bus can either be 8-bits or 16-bits wide depending on selection of CE0# and CE1#
CE0#, CE1#	CE1# always selects the odd byte of the word. CE0# accesses the even or odd byte depending on A0 and CE1#. For 8-bit systems, CE0# is used and for 16-bit systems, both CE0# and CE1# are used. Both CE0# and CE1# should be decoded by the logic to determine the memory window.
OE#	This is an output enable strobe generated by the host interface. It is used to read data from the Flash ChipSet in Memory Mode and to read the CIS and configuration registers
WE#	The write enable pin is driven by the host and used for strobing data to the registers of the Flash ChipSet when the Flash ChipSet is configured in the memory interface mode. It is also used for writing the configuration registers.
A0-A10	A0-A3 selects the basic registers of the controller to communicate to the module. This requires 16 bytes of host address space. A0 is optional if CE0# and CE1# are combined to enable 16-bit wide register access.
Busy	The Busy signal is driven low when the product is accessing memory. When Busy is high, register access is allowed. After a data transfer command is issued, this signal is used to signify that the host can transfer data.
RST	When RST is high, the product is placed in a reset mode. This signal is only valid at power on.
BVD1	This signal is driven high since a battery is not used with this product
BVD2	This output line is always driven to a high state in Memory Mode since a batery is not required for this product
IOWR	This signal is not used in the memory mode.
IORD	This signal is not used in the memory mode.
REG	This signal is used during Memory Cycles to distinguish between common memory and register memory accesses. High for common memory, low for attribute memory.
INPACK	This signal is not used in the memory mode.
IO16	Optional test signals not used in the Memory Mapped Mode.
Reserved	Pins are reserved for future expansion and must be left floating.
V_{CC}	Power pins. All V_{CC} pins must be connected.
V_{SS}	Ground pins. All V_{SS} pins must be connected.
NC	No connect. Pin internally not connected.

BLOCK DIAGRAM



PACKAGE



ALL DIMENSIONS ARE IN INCHES