XC73144
144-Macrocell CMOS EPLD

Product Specifications

Features

- High-Performance EPLD
  - 7.5 ns pin-to-pin speed on all fast inputs
  - 100 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - Four Fast Function Blocks
  - Twelve High-Density Function Blocks
- 100% interconnect matrix
- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 MHz 16-bit accumulators
- 144 Macrocells with programmable I/O architecture
- Up to 132 inputs programmable as direct, latched, or registered
- All outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 160-pin plastic quad flat pack and 225-pin ball-grid-array packages
- 100% PCI compliant
- Programmable slew rate
- Programmable ground control

General Description

The XC73144 is a member of the Xilinx Dual-Block EPLD family. It consists of four Fast Function Blocks and twelve High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The sixteen Function Blocks in the XC73144 are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM and output pins.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

The XC73144 is designed in a 0.8 µ CMOS EPROM technology.

In addition, the XC73144 includes a programmable power management feature to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software (XEPLD) supports all members of XC7300 family. The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator automatically performs logic optimization, collapsing, mapping and routing without user intervention. After compiling the design, XEPLD translator produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques
- Converts netlist to fuse map in minutes using a 386/486 PC or workstation platform
- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages
- Timing simulation using Viewsim, OrCAD VST, Mentor, LMC and other tools compatible with the Xilinx Netlist Format (XNF)

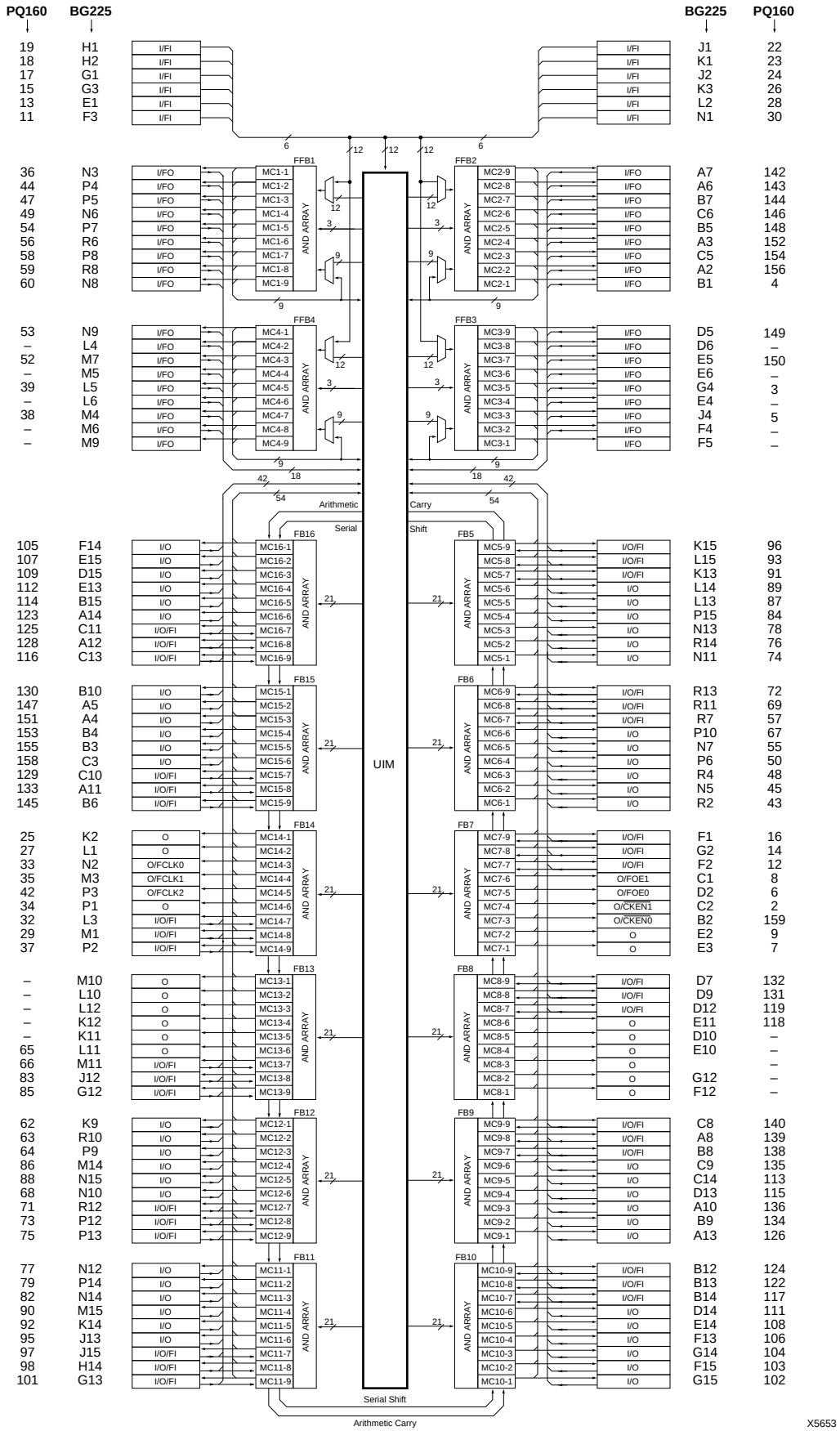


Figure 1. XC73144 Functional Block, Diagram

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND	Commercial	T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	T_A = -40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	T_A = -55°C to T_C = +125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50.0	ns

Power Management

The XC73144 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}(mA) = MC_{HP}\ (2.4) + MC_{LP}\ (2.1) + MC\ (0.015\ mA/MHz)\ f$$

Where:

- MC_{HP} = Macrocells in high-performance mode
- MC_{LP} = Macrocells in low-power mode
- MC = Total number of Macrocells used
- f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC73144 device, programmed as eight 16-bit counters and operating at the indicated clock frequency.

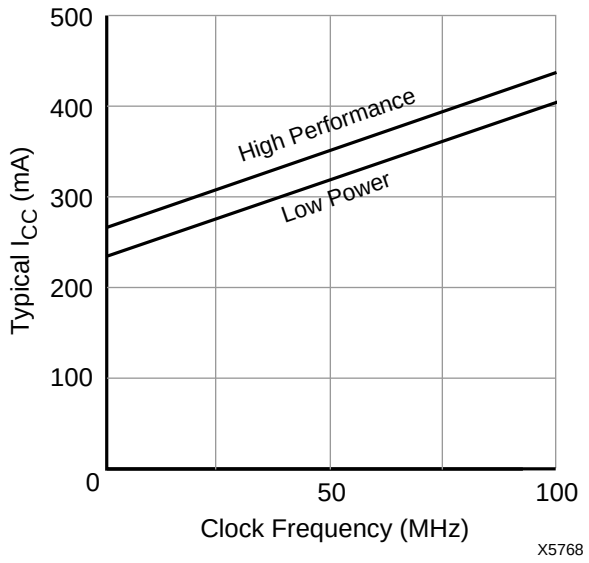


Figure 2. Typical I_{CC} vs Frequency for XC73144

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT} [1]	Output capacitance	V_O = GND f = 1.0 MHz		20.0	pF
I_{CC1} [2]	Supply Current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5 V f = 1.0 MHz @ 25°C	250 Typ		mA

Notes: 1. Sample tested
2. Measured with device programmed as eight 16-bit counters

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Slew Rate and Programmable Ground Control

Due to the large number of high current drivers available on the XC73144, two programmable signal management features have been included – slew rate control (SRC) and ground control (GC). Slew rate control is primarily for external system benefit, to reduce ringing and other coupling phenomenon. SRC permits designers to select either 1 V/ns or 1.5 V/ns slew rate on a pin-by-pin basis for any output or I/O signal. This can be done with PLUSASM or schematically, as needed. The defafult slew rate is 1 V/ns. To assign the pins with equations (PLUSASM), the designer needs to only declare them as follows:

FAST ON <signal name list>

This will assign the signals in the list to have a 1.5 V/ns slew rate. Omitting the signal name list will globally set all signals to be 1.5 V/ns. Specific signals therefore can be declared with 1 V/ns slew rate as follows:

FAST OFF <signal name list>

Schematic control of SRC is also straightforward. Again, the default is 1 V/ns, but to assign specific pins fast, the designer need only attach the “FAST” attribute to the I/O or output buffer or the corresponding pin.

Programmable ground control is useful for internal chip signal management. The output buffers of the Fast Function Blocks have an impedance of around 7 Ω when switching high to low, where the High Density Function Blocks impedance is around 14 Ω. Since this low impedance is negligible compared to the impedance of the pin inductance when output current transients occur, a reasonable ground connection can be made by driving unused output pins low and physically attaching them to external ground. The XC73144 architecture permits the automatic assignment of external ground signals to all Macrocells that are not declared as primary outputs or I/Os. Note that the logical function of the buried Macrocell is fully preserved, while its output driver is driving low and physically attached to ground. Should designers not wish to employ programmable ground control, they need only declare all such pins as primary I/Os whether they will be attached externally or not.

Fast Function Block (FFB) External AC Characteristics [3]

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1, 2]	105.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1, 2]		13.5		19.0		22.0		27.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	83.3		62.5		55.6		45.5		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	12.0		16.0		18.0		22.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		20.0		23.0		28.0	ns
t_{PD}	I/O to output valid [1, 2]		18.0		25.0		30.0		36.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Preliminary

Notes:
1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [2]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [2]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [2]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [2]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [4]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [4]		1.0		1.5		2.0		3.0	ns

Preliminary

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

4. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

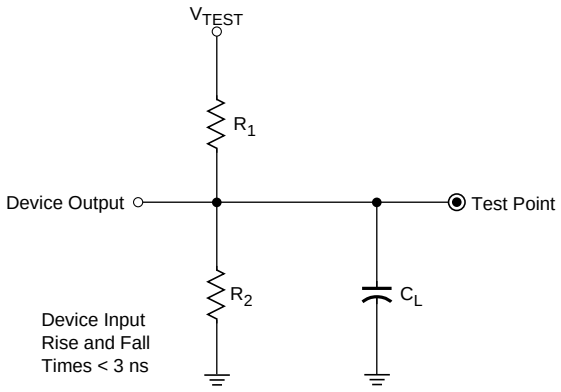
Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [2]	83.3		62.5		55.6		45.5		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns

Preliminary

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3. AC Load Circuit

XC73144 Pinouts

BG225	PQ160	Input	XC73144	Output
D3	1		V_{CCIO}	
E4	-	I/FO		MC3-4
F4	-	I/FO		MC3-2
C2	2	O/CKEN1		MC7-4
F5	-	I/FO		MC3-1
G4	3	I/FO		MC3-5
B1	4	I/FO		MC2-1
J4	5	I/FO		MC3-3
D2	6	O/FOE0		MC7-5
E3	7	O		MC7-1
C1	8	O/FOE1		MC7-6
E2	9	O		MC7-2
D1	10		V_{CCINT}/V_{PP}	
F3	11	I/FI		
F2	12	I/O/FI		MC7-7
E1	13	I/FI		
G2	14	I/O/FI		MC7-8
G3	15	I/FI		
F1	16	I/O/FI		MC7-9
G1	17	I/FI		
H2	18	I/FI		
H1	19	I/FI		
H3	20		**GND**	
J3	21	I/FI	MR	
K5	-		V_{CCIO}	
J1	22	I/FI		
K1	23	I/FI		
J2	24	I/FI		
K2	25	O		MC14-1
K3	26	I/FI		
L1	27	O		MC14-2
L2	28	I/FI		
M1	29	I/O/FI		MC14-8
N1	30	I/FI		
M2	31		**GND**	
L3	32	I/O/FI		MC14-7
N2	33	O/FCLK0		MC14-3
P1	34	O		MC14-6
M3	35	O/FCLK1		MC14-4
N3	36	I/FO		MC1-1
K4	-	I/FO		MC4-1
L4	-	I/FO		MC4-2
P2	37	I/O/FI		MC14-9
M4	38	I/FO		MC4-3
L5	39	I/FO		MC4-5
R1	40		**GND**	

BG225	PQ160	Input	XC73144	Output
N4	41		V_{CCIO}	
P3	42	O/FCLK2		MC14-5
R2	43	I/O		MC6-1
P4	44	I/FO		MC1-2
N5	45	I/O		MC6-2
R3	46		V_{CCINT}	
M5	-	I/FO		MC4-4
P5	47	I/FO		MC1-3
R4	48	I/O		MC6-3
L6	-	I/FO		MC4-6
M6	-	I/FO		MC4-8
N6	49	I/FO		MC1-4
P6	50	I/O		MC6-4
R5	51		**GND**	
M7	52	I/FO		MC4-7
M9	53	I/FO		MC4-9
P7	54	I/FO		MC1-5
N7	55	I/O		MC6-5
R6	56	I/FO		MC1-6
R7	57	I/O/FI		MC6-7
P8	58	I/FO		MC1-7
R8	59	I/FO		MC1-8
N8	60	I/FO		MC1-9
N9	61		V_{CCIO}	
M10	-	O		MC13-1
L10	-	O		MC13-2
R9	62	I/O		MC12-1
R10	63	I/O		MC12-2
P9	64	I/O		MC12-3
L11	65	O		MC13-6
M11	66	I/O/FI		MC13-7
M12	-		**GND**	
P10	67	I/O		MC6-6
N10	68	I/O		MC12-6
R11	69	I/O/FI		MC6-8
P11	70		**GND**	
R12	71	I/O/FI		MC12-7
R13	72	I/O/FI		MC6-9
P12	73	I/O/FI		MC12-8
N11	74	I/O		MC5-1
P13	75	I/O/FI		MC12-9
R14	76	I/O		MC5-2
N12	77	I/O		MC11-1
N13	78	I/O		MC5-3
P14	79	I/O		MC11-2
R15	80		**GND**	

XC73144 Pinouts (continued)

BG225	PQ160	Input	XC73144	Output
M13	81		V_{CCIO}	
L12	-	O		MC13-3
K12	-	O		MC13-4
N14	82	I/O		MC11-3
K11	-	O		MC13-5
J12	83	I/O/FI		MC13-8
P15	84	I/O		MC5-4
G12	85	I/O/FI		MC13-9
M14	86	I/O		MC12-4
L13	87	I/O		MC5-5
N15	88	I/O		MC12-5
L14	89	I/O		MC5-6
M15	90	I/O		MC11-4
K13	91	I/O/FI		MC5-7
K14	92	I/O		MC11-5
L15	93	I/O/FI		MC5-8
J14	94		V_{CCINT}	
J13	95	I/O		MC11-6
K15	96	I/O/FI		MC5-9
J15	97	I/O/FI		MC11-7
H14	98	I/O/FI		MC11-8
H15	99		**GND**	
H13	100		**GND**	
F11	-		V_{CCINT}	
G13	101	I/O		MC11-9
G15	102	I/O		MC10-1
F15	103	I/O		MC10-2
G14	104	I/O		MC10-3
F14	105	I/O		MC16-1
F13	106	I/O		MC10-4
E15	107	I/O		MC16-2
E14	108	I/O		MC10-5
D15	109	I/O		MC16-3
C15	110		**GND**	
D14	111	I/O		MC10-6
E13	112	I/O		MC16-4
C14	113	I/O		MC9-5
B15	114	I/O		MC16-5
D13	115	I/O		MC9-4
C13	116	I/OFI		MC16-9
F12	-	O		MC8-1
E12	-	O		MC8-2
B14	117	I/O/FI		MC10-7
E11	118	O		MC8-6
D12	119	I/O/FI		MC8-7
A15	120		**GND**	

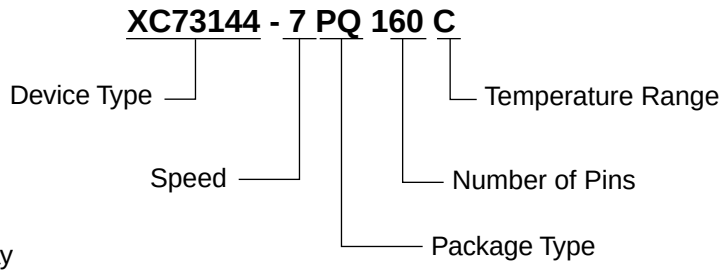
BG225	PQ160	Input	XC73144	Output
C12	121		V_{CCIO}	
B13	122	I/O/FI		MC10-8
A14	123	I/O		MC16-6
B12	124	I/O/FI		MC10-9
C11	125	I/O/FI		MC16-7
A13	126	I/O		MC9-1
D11	-			
B11	127		**GND**	
A12	128	I/O/FI		MC16-8
E10	-			MC8-4
D10	-			MC8-5
C10	129	I/O/FI		MC15-7
B10	130	I/O		MC15-1
D9	131	I/O/FI		MC8-8
D7	132	I/O/FI		MC8-9
A11	133	I/O/FI		MC15-8
B9	134	I/O		MC9-2
C9	135	I/O		MC9-6
A10	136	I/O		MC9-3
A9	137		**GND**	
B8	138	I/O/FI		MC9-7
A8	139	I/O/FI		MC9-8
C8	140	I/O/FI		MC9-9
C7	141		V_{CCIO}	
A7	142	I/FO		MC2-9
A6	143	I/FO		MC2-8
B7	144	I/FO		MC2-7
B6	145	I/O/FI		MC15-9
C6	146	I/FO		MC2-6
D6	-	I/FO		MC3-8
E6	-	I/FO		MC3-6
A5	147	I/O		MC15-2
B5	148	I/FO		MC2-5
D5	149	I/FO		MC3-9
E5	150	I/FO		MC3-7
A4	151	I/O		MC15-3
A3	152	I/FO		MC2-4
B4	153	I/O		MC15-4
C5	154	I/FO		MC2-3
D4	-		**GND**	
B3	155	I/O		MC15-5
A2	156	I/FO		MC2-2
C4	157		V_{CCINT}	
C3	158	I/O		MC15-6
B2	159	O/CKEN0		MC7-3
A1	160		**GND**	

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 2-1 through 2-10.

For a detailed description of the device timing, see pages 2-9, 2-10 and 2-50 through 2-52.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Speed Options

-15 15 ns pin-to-pin delay
-12 12 ns pin-to-pin delay
-10 10 ns pin-to-pin delay (commercial only)
-7 7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PQ160 160-Pin Plastic Quad Flat Pack
BG225 225-Pin Plastic Ball-Grid-Array

Temperature Options

C Commercial $0^{o}C$ to $70^{o}C$
I Industrial $-40^{o}C$ to $85^{o}C$

Component Availability

Pins		44			68		84		100	144	160	225	
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Ceramic BGA
Code		PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC73144	-15										CI	CI	CI
	-12										CI	CI	CI
	-10										C	C	C
	-7										C	C	C

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C

Parenthesis indicate future product plans

X5654