FEATURES

- Single 10/12-Bit 8 MSPS A/D Converter
- Serial or Parallel Programming Interface
- Triple Correlated Double Sampler
- Triple Programmable Gain Amplifier
- Triple-Channel, 2.5 MSPS CCD Color Scan Mode
- Single-Channel, 6 MSPS Monochrome Scan Mode CCD or CIS
- Differential or Single Ended Inputs
- CDS for CCD or S/H Mode for CIS
- Inverting or Non-Inverting Mode

- Internal/External Voltage Reference
- 3V or 5V Operation and I/O Compatibility
- Low Power CMOS: 500mW @ 5V
- 8-1 Analog Multiplexer

APPLICATIONS

- CCD or CIS Color Scanners
- Color and Gray Scale Flat-Bed Scanners
- Multifunction Products
- Film Scanners

GENERAL DESCRIPTION

The XRD9820/22 is a fully integrated, high-performance analog signal processor/digitizer specifically designed for use in 3-channel linear CCD and CIS imaging applications. Each channel of the XRD9820/22 includes a Correlated Double Sampler (CDS), Programmable Gain Amplifier (PGA) and channel offset adjustment. After gain and offset adjustment, the analog inputs are sequentially sampled and digitized by an accurate 10-Bit (XRD9820) or 12-Bit (XRD9822) A/D converter.

The XRD9820/22 also contain a high speed 8-1 analog multiplexer which can be used to monitor system parameters and perform system calibration.

The analog front-end can be configured for inverting/non-inverting input, CDS or sample-hold (S/H) mode, or AC/DC coupling, making the XRD9820/22 suitable for use in CCD, CIS and other data acquisition applications. The CDS mode of operation supports both line and pixel-clamp modes and can be used to achieve

significant reduction in system 1/f noise and CCD reset clock feed-through. In S/H mode the internal DC-restore voltage clamp can be enabled or disabled to support AC-coupled or DC inputs.

PGA gain and channel offsets can be updated on a line by line basis. Each channel can have a seperate offset and gain setting. The differential inputs reject common mode noise that can accumulate in a scanner system due to lamp switching and cabling.

Sampling mode, PGA gain, channel offset and input signal polarity can be programmed through the 8 most significant bits of a bi-directional data bus or through a serial interface. PGA gain (1-10) and channel offset (-300mV to 300mV) are programmable in 256 linear steps. The A/D Full-Scale Range (FSR) is programmable to 2V or 3V operation using the internal reference or can be set through the external reference pin.

ORDERING INFORMATION

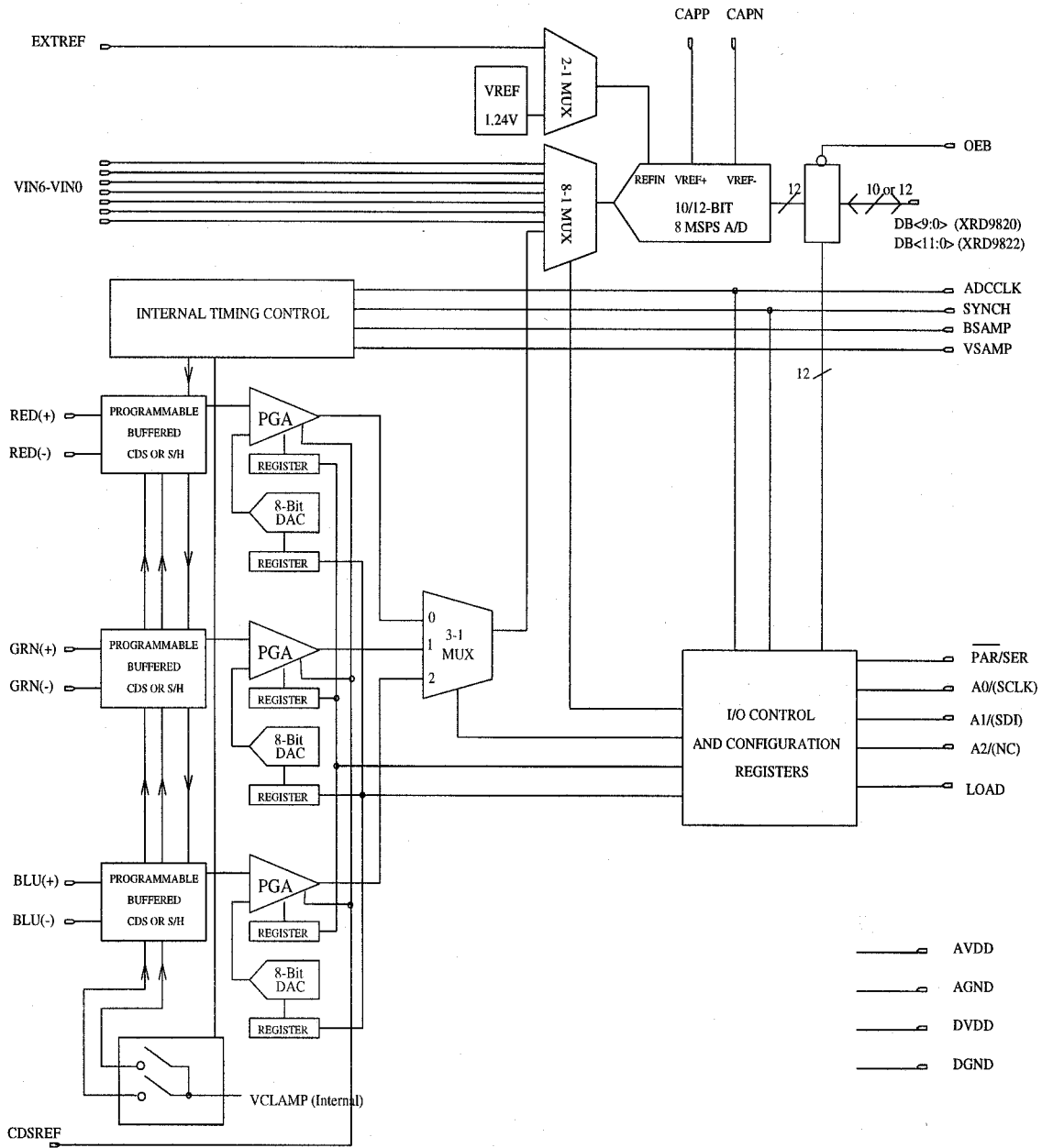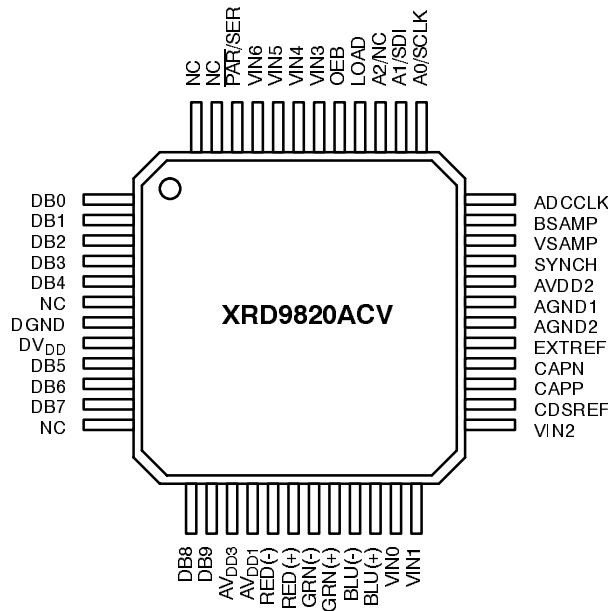| Part No.	Package	Operating Temperature Range
XRD9820ACV	48 Lead TQFP	0°C to +70°C
XRD9822ACV	48 Lead TQFP	0°C to +70°C

Figure 1. XRD9820/22 Functional Block Diagram

PIN CONFIGURATION

48 Lead TQFP (7 x 7 x 1.0 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	DB0	Data Output Bit 0
2	DB1	Data Output Bit 1
3	DB2	Data I/O Bit 2
4	DB3	Data I/O Bit 3
5	DB4	Data I/O Bit 4
6	NC	No Connect
7	DGND	Ground (Output Drivers and Internal Decode Logic)
8	DV_{DD}	Digital Power Supply (Output Drivers and Internal Decode Logic)
9	DB5	Data I/O Bit 5
10	DB6	Data I/O Bit 6
11	DB7	Data I/O Bit 7
12	NC	No Connect
13	DB8	Data I/O Bit 8
14	DB9	Data I/O Bit 9

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
15	AV_{DD3}	Analog Power Supply
16	AV_{DD1}	Analog Power Supply
17	RED(-)	Red Negative Analog Input
18	RED(+)	Red Positive Analog Input
19	GRN(-)	Green Negative Analog Input
20	GRN(+)	Green Positive Analog Input
21	BLU(-)	Blue Negative Analog Input
22	BLU(+)	Blue Positive Analog Input
23	VIN0	Multiplexer Input Channel 0
24	VIN1	Multiplexer Input Channel 1
25	VIN2	Multiplexer Input Channel 1
26	CDSREF	Decoupling Cap CDSREF
27	CAPP	Decoupling Cap for Positive Reference
28	CAPN	Decoupling Cap for Negative Reference
29	EXTREF	External A/D Reference
30	AGND2	Analog Ground (Substrate)
31	AGND1	Analog Ground (Substrate)
32	AV_{DD2}	Analog Power Supply
33	SYNCH	RGB Start of Line
34	VSAMP	Video Level Sampling Clock
35	BSAMP	Black Level Sampling Clock
36	ADCCLK	A/D Converter Clock
37	A0/SCLK	Register Address/ Serial Clock
38	A1/SDI	Register Address/Serial Data
39	A2/NC	Register Address/No Connect
40	LOAD	Register Write Enable
41	OEB	Active Low Output Enable
42	VIN3	Multiplexer Input Channel 3
43	VIN4	Multiplexer Input Channel 4
44	VIN5	Multiplexer Input Channel 5
45	VIN6	Multiplexer Input Channel 6
46	$\overline{PAR}$ / SER	Parallel/Serial Mode Select
47	NC	No Connect
48	NC	No Connect

ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD}=DV_{DD}=5.0V$, ADCCLK=6MHz, $T_A=25°C$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
A/D CONVERTER						
	Resolution					
R	XRD9820	10			BITS	
R	XRD9822	12			BITS	
Fc	Conversion Rate	6	8		MSPS	
DNL	Differential Non-Linearity	-1.0	+/-0.5	+1.0	LSB	
INL	Integral Non-Linearity		+/-2.0		LSB	
M	Monotonicity		Yes			Guaranteed
ZSE	Input Referred Offset		30		mV	
ZSD	Offset Drift		15		µV/°C	
FSE	Input Referred Gain Error		+/- 2		% FS	
FSD	Gain Error Drift		.003		% FS/°C	
	Input Voltage Range					
IVR	2V Full-Scale Range	0		2.0	V	PB5=0, Config Reg #1
IVR	3V Full-Scale Range	0		3.0	V	PB5=1, Config Reg #1
CDS - S/H SPECIFICATIONS						
	Input Voltage Range					
INVSR	Input Buffer Disabled (Note 1)	AGND		AV_{DD}	V	AC Coupled, PB1=0, Config Reg #1
INVSRB	Input Buffer Enabled	.5		$AV_{DD}-1$	V	DC Coupled, PB1=1, Config Reg #1
	Input Bias Current					
IB	Input Buffer Disabled (Note 2)		25µA		uA	PB1=0, Config Reg #1, Gain=1
IBB	Input Buffer Enabled			25	nA	$T_A=70°C$, PB1=1, Config Reg #1
Ron	Input Switch On -Resistance		85	150	Ω	Clamp Enabled
Roff	Input Switch Off -Resistance	100	1000		MΩ	Clamp Disabled
	Internal Voltage Clamp					
Vclamp	CCD Input (Inverting)		4		V	PB2=0 (Reg 1), Config Reg #1
Vclamp	S/H Input (Non-Inverting)		.5		V	PB2=1 (Reg 1), Config Reg #1
PGA SPECIFICATIONS						
GRAN	Gain Range	-1		-10	V/V	
GRES	Gain Resolution		-.035		V/V	8-Bit 256 Steps, Monotonic
OFFSET SPECIFICATIONS						
OFR	Offset Adjustment Range	-300		300	mV	
OFRES	Offset Adjustment Resolution		2.75		mV	8-Bit 256 Steps, Monotonic

Notes:

1   *ADC digitizing range = (A/D Full-Scale Range/PGA Gain)*

2   *Due to switch capacitor input.*

ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD}=DV_{DD}=5.0V$, ADCCLK=6MHz, $T_A=25°C$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
SYSTEM SPECIFICATIONS (Includes CDS, PGA and A/D)						
	Differential Non-Linearity					
DNL_{SMIN}	PGA Gain= -1		+/-0.5		LSB	
DNL_{SMAX}	PGA Gain= -10		+/-0.5		LSB	
	Integral Non-Linearity (XRD9810)					
INL_{SMIN}	PGA Gain= -1		+/-1.5		LSB	
INL_{SMAX}	PGA Gain = -10		+/-3.0		LSB	
	Integral Non-Linearity (XRD9812)					
INL_{SMIN}	PGA Gain= -1		+/-2.5		LSB	
INL_{SMAX}	PGA Gain = -10		+/-5.0		LSB	
	Input Referred Noise					
IRN_{SMIN}	PGA Gain = -1		500		μV rms	
IRN_{SMAX}	PGA Gain = -10		200		μV rms	
	Input Referred Offset					
IRO_{SMIN}	PGA Gain= -1		+/-25		mv	
IRO_{SMAX}	PGA Gain = -10		+/-15		mv	

ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD}=DV_{DD}=5.0V$, ADCCLK=6MHz, $T_A=25°C$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TIMING SPECIFICATIONS						
tcr3	3-Channel Conversion Period	400			ns	
tcr1	1-Channel Conversion Period	166			ns	
tpwb	BSAMP Pulse Width	30			ns	
tbvf	BSAMP falling edge to VSAMP falling edge.	70			ns	
tvbf	VSAMP falling edge to BSAMP falling edge.	70			ns	
tvfcr	VSAMP falling edge delay from rising ADCCLK. (All modes except 1 Channel S/H).	30			ns	
tvfcr	VSAMP falling edge delay from rising ADCCLK (1 Channel S/H)	70			ns	Config Reg #1, PB2=1, PB7=1
tpwv	VSAMP Pulse Width	30			ns	
VSAMP TIMING OPTION #1						
tvrcf	VSAMP rising edge delay from falling ADCCLK [1]	15			ns	tvrcr is not required Config Reg #1, PB0=0
VSAMP TIMING OPTION #2						
tvrcr	VSAMP rising edge delay from rising ADCCLK [1]	15			ns	tvrcf is not required Config Reg #1, PB0=1
taclk	ADCCLK Pulse Width	50			ns	
tcp1	ADCCLK Period (1 Ch. Mode)	166			ns	
tcp3	ADCCLK Period (3 Ch. Mode)	133			ns	
tstl	PGA Settling Time for accurate ADC Sampling	70			ns	
ts	SYNCH Rising, Falling Setup	15			ns	
th	SYNCH Rising, Falling Hold	15			ns	
tap	Aperture Delay		5		ns	
WRITE SPECIFICATIONS						
tas	Address Setup Time	15			ns	
tah	Address Hold Time	15			ns	
tds	Data Setup Time	15			ns	
tdh	Data Hold Time	15			ns	
tcss	Chip Select Setup Time	15			ns	
tcsh	Chip Select Hold Time	15			ns	
tpww	Write Pulse Width	25			ns	

Note:

[1] *VSAMP Timing Option #2 allows additional timing flexibility by allowing the rising edge of VSAMP to occur approximately one-half ADCCLK period earlier than Option #1. Option #2 is only available in 3-channel operation (PB4=0, PB3=0, configuration Register #1).*

ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD}=DV_{DD}=5.0V$, ADCCLK=6MHz, $T_A=25°C$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DATA READBACK SPECIFICATIONS						
taa (1)	Address Access Time		20		ns	
taoe (1)	Output Enable Access Time		20		ns	
toh	Output Data Hold from Address Change		5		ns	
ADC DIGITAL OUTPUT SPECIFICATIONS						
tod	Output Delay		20		ns	
tlz	3-State to Data Valid		8		ns	
thz	Output Enable High to 3-State Latency		8		ns	
lat	Multiplexer Input		6		ADCCLK	
lat	RGB Inputs		6		ADCCLK	
DIGITAL INPUTS						
V_{IH}	Input High Logic Level	80			% DV_{DD}	DV_{DD}=3-5V
V_{IL}	Input Low Logic Level			20	% DV_{DD}	DV_{DD}=3-5V
I_{IH}	High Level Input Current		5		µA	
I_{IL}	Low Level Input Current		5		µA	
C_{IN}	Input Capacitance		10		pF	
DIGITAL OUTPUTS (DV_{DD}=5V)						
V_{OH}	Output High Voltage	4.2			V	I_L=2ma
V_{OL}	Output Low Voltage			0.4	V	I_L=-2ma
C_{OUT}	Output Capacitance		10		pF	
DIGITAL OUTPUTS (DV_{DD}=3.3V)						
V_{OH}	Output High Voltage	2.8			V	I_L=2ma
V_{OL}	Output Low Voltage			0.3	V	I_L=-2ma
C_{OUT}	Output Capacitance		10		pF	
POWER SUPPLY						
AV_{DD}	Analog Power Supply	4.5	5.0	5.5	V	
DV_{DD}	Digital Power Supply	3.0	5.0	5.5	V	
IDDA	Analog Supply Current		90		mA	
IDDD	Digital Supply Current		10		mA	Digital Output CLoad=30pF, all pins.
PDoff	Sleep Mode Current		15		mA	

Note:

[1] *Start of valid data depends on which timing becomes effective last, taoe or taa.*

Function	A2	A1	A0	PB7-PB0 (Note 1)
Configuration Reg #1	0	0	0	See Configuration Register #1
Configuration Reg #2	0	0	1	See Configuration Register #2
Red Gain	0	1	0	8-Bit Gain
Green Gain	0	1	1	8-Bit Gain
Blue Gain	1	0	0	8-Bit Gain
Red Offset	1	0	1	8-Bit Offset
Green Offset	1	1	0	8-Bit Offset
Blue Offset	1	1	1	8-Bit Offset

Table 1. XRD9820/22 Register Overview

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Clamp Mode	Clamp Mode	A/D Full Scale Range	Color Select	Color Select	Signal Polarity	Buffer Enable	Vsam Timing

Table 2. Configuration Register #1 Bit Assignment (Note 1)

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
8:1 Mux Select	8:1 Mux Select	8:1 Mux Select	A/D Mux Select	Test Mode	A/D Ext Ref	Sleep Mode	Read Back

Table 3. Configuration Register #2 Bit Assignment (Note 1)

A2 A1 A0	PB7 PB6	PB5	PB4 PB3	PB2	PB1	PB0
Address	Clamp Mode	A/D FSR	Color Select	Input Signal Polarity	Input Buffer Enable	VSAMP Timing
0 0 0	0 0 - Pixel 0 1 - CDS Line 1 0 - No Clamp 1 1 - S/H Line	0 - 2V 1 - 3V	0 0 - RGB 0 1 - G & RB 1 0 - Green 1 1 - Bayer	0 - Inverted (CCD) 1 - Non-inverted (CIS)	0 - No Buffer (DC or AC Coupling w/Pixel Clamp). 1 - Enable Buffer (AC coupling and Line/No clamp)	0 - Timing #1 1 - Timing #2

Table 4. Configuration Register #1 Definition (Power Up State is 0h)

Note:

[1] Data PB7-PB0 corresponds to the 8 most significant bits of the data output bus. (See below)

A2 A1 A0	PB7 PB6 PB5	PB4	PB3	PB2	PB1	PB0
Address	8-1 Mux Select	A/D Mux Select	Test Mode Enable	A/D External Reference	Sleep Mode	Read-back Mode

0 0 1	0 0 0 - Channel 0
	0 0 1 - Channel 1
	0 1 0 - Channel 2
	0 1 1 - Channel 3
	1 0 0 - Channel 4
	1 0 1 - Channel 5
	1 1 0 - Channel 6
	If PB3=0,
	1 1 1 - Internal
	        Reference
	If PB3=1,
	1 1 1 - Register
	        Reset
		0 - A/D Input from PGA.
		1 - A/D input from 8-1 Mux.
			0 - Test Mode Disabled
			1 - Test Mode Enabled.
				0 - A/D uses internal reference.
				1 - A/D uses external reference.
					0 - All circuits active.
					1 - Low PowerMode.
						0 - (A/D digital output)
						
						1 - PB7- PB0 (A2:A0 select register data).

Table 5. Configuration Register #2 Definition (Power Up State is 0h)

A2 A1 A0	Function	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0 1 0	Red Gain	MSB							LSB
0 1 1	Green Gain	MSB							LSB
1 0 0	Blue Gain	MSB							LSB
1 0 1	Red Offset	MSB							LSB
1 1 0	Green Offset	MSB							LSB
1 1 1	Blue Offset	MSB							LSB

Table 6. Gain And Offset Registers

Note:

[1] *Data PB7-PB0 corresponds to the 8 most significant bits of the data output bus. (See below)*

Part #	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
XRD9820	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
XRD9822	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4

Table 7. Programming Bit to I/O Bit Correspondence

GENERAL

The XRD9820/22 contains all of the circuitry required to create a complete 3-channel signal processor /digitizer for use in CCD/CIS imaging system. Each channel includes a correlated double sampler, programmable gain amplifier and channel offset adjustment. The input stage can also be configured for use with inverting/non-inverting, AC or DC coupled signals. In order to maximize flexibility the specific operating mode is programmable through two configuration registers in serial or parallel mode. In addition the gain and offset of each channel can be independently programmed through separate gain and offset registers. In parallel mode configuration register data corresponds to the 8 most significant bits of the data bus (DB11-DB4 for the XRD9820, DB9-DB2 for the XRD9820). In serial mode, data is shifted through dual purpose pins (A0/SCLK) and (A1/SDI). Specific details for register writes are detailed below. After signal conditioning the three PGA outputs are digitized by a 10-bit (XRD9820) or 12-bit (XRD9822) A/D converter. The XRD9820/22 also has an on-board 8-1 analog multiplexer which can be used to digitize any signal which is within the input range of the A/D.

Writing Registers Data

The XRD9820/22 configuration registers can be written to in both parallel and serial modes. In serial mode (PAR=0), register data is written though the 3-pin serial interface consisting of SDI (serial data input), SCLK (serial shift clock) and LOAD (positive edge write enable). A write consists of pulling LOAD low, shifting in 3 bits of address (MSB first) and 8 bits of data (MSB first). Data is written on the rising edge of LOAD. The timing diagram for writing to registers is shown in the timing diagrams. In parallel mode (PAR=1) register data is accessed through the 3-bit address inputs A0-A2. In order to write data to a register the active low output enable (OEB) should first be set to logic one in order to tristate the output data bus. The most significant 8-Bits on the data bus are written to the register input on the rising edge of LOAD. The timing diagram for writing to registers is shown in the timing diagrams.

Configuration Register #1

The bit assignment and definition for this register is detailed in the Configuration Register #1 Definition Table. The primary purpose of this register is to configure the analog input blocks for CCD or S/H operation.

Clamp Mode

The clamp mode setting determines the conditions when the internal clamp is enabled. (see Table 1). The pixel and CCD line-clamp modes are used to DC-restore AC coupled CCD input signals to the PGA common-mode input voltage while using correlated double sampling. S/H Line mode should be used to DC-restore AC coupled inputs which do not utilize correlated double sampling and have only one control input (VSAMP). No-Clamp mode should be used for DC coupled S/H inputs or AC coupled signals which have been externally DC-restored to the proper common-mode input voltage of the XRD9820/22.

Pixel Mode (CCD with CDS)

The input clamp is active each pixel period with a pulse-width determined by the black level sampling input (BSAMP). The position of BSAMP can be optimized to eliminate the effects of the CCD reset pulse. Since the input capacitor is recharged to the clamp voltage on each pixel, common-mode droop errors are eliminated.

CCD Line Mode (CCD with CDS)

The input clamp is enabled only at the beginning of the line by gating BSAMP with $\overline{SYNCH}$. Gating with $\overline{SYNCH}$ maintains the ability to position the clamp pulse (BSAMP) away from the CCD reset for varying $\overline{SYNCH}$ position and width. Since the input capacitor is clamped only at the beginning of each line a larger input capacitor is required to satisfy the common-mode input requirements of the analog front-end. (See Coupling Capacitor Requirements). The input buffer should be enabled in this mode (PB1=1, Register #1).

S/H Line Mode (S/H with AC Coupling)

The S/H Line mode clamp is used to DC-restore AC coupled inputs which do not utilize CDS. VSAMP is used to sample and hold the input signal and $\overline{SYNCH}$ performs the clamp function. This differs from the CDS line and pixel modes which use BSAMP to clamp to the reference

level and VSAMP to hold the video input. The input buffer should be enabled in this mode (PB1=1, Register #1).

No-Clamp Mode (S/H with DC Input)

Used for DC coupled inputs or AC coupled inputs that have been externally clamped to the proper common-mode input voltage of the XRD9820/22. Pixel clamp is the default clamp mode.

Clamp Mode	PB7	PB6	Clamp Enable
Pixel	0	0	BSAMP
CDS Line	0	1	$BSAMP \cdot \overline{SYNCH}$
No Clamp	1	0	Disabled
S/H Line	1	1	$\overline{SYNCH}$

Table 8. Clamp Enable Definition
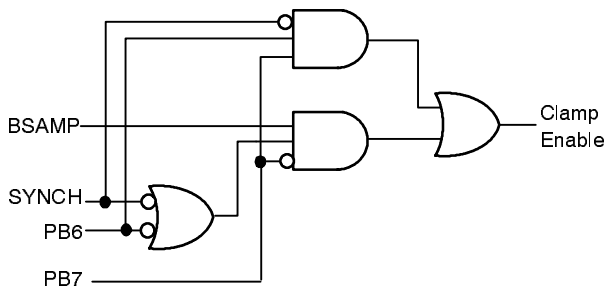
Figure 2.

A/D Full-Scale Range

This bit sets the Full-Scale Range (FSR) of the A/D converter to 2V or 3V.

Color Select

The color input corresponds to the signal input to be digitized by the A/D converter. If set to RGB (default) the A/D input is sequentially cycled through the red, green and blue channels. The red channel input is synchronized by sampling the SYNCH signal on the rising edge of

ADCCLK. If set to the green color the A/D multiplexer will not sequence and the A/D converter input will be continually connected to the green input (if 8-1 multiplexer is not selected, See Configuration Register #2, PB4).

Signal Polarity

This bit configures the analog inputs for positive or negative transitioning inputs. This is required to provide the correct signal polarity to the A/D input and to set the correct input clamp level. The default configuration is set to inverting mode (CCD input).

Input Buffer Enable

This bit enables the input buffer to the PGA amplifier and is required only for AC coupled inputs operating in CDS Line or S/H Line clamp modes. Since this input buffer reduces the input voltage range it's use is not recommended under DC or pixel-mode operation. The default setting is no buffer.

VSAMP Timing

This allows the user to select one of two VSAMP timing controls. Timing Option #2 allows the rising edge of VSAMP to occur approximately one-half ADCCLK earlier than Option #1. This does not affect internal timing and is provided only to allow additional flexibility in the external timing control. Timing Option #2 is available only in the 3-channel mode of operation. (See timing diagram).

Configuration Register #2

The bit assignment and definition for this register is detailed in the Configuration Register #2 Definition Table. The primary purpose of this register is to control the XRD9820/22 8-1 multiplexer inputs and A/D reference. A diagnostic read-back mode allows gain, offset and configuration data to be output as the high-byte on the digital output bus. Additional bits are used to enable a low-power sleep state and manufacturing test mode.

8-1 Multiplexer Select

The three most significant bits (PB7-PB5) are used in conjunction with PB4 to control the input to the A/D converter. Bits PB7-PB5 are decoded (See Configuration Register #2 Definition) to select one of the eight multiplexer channels.

A/D Multiplexer Select

Setting this bit to 0 (default) connects the A/D converter input to the PGA outputs (see Color Select of Configuration Register #1). Setting this bit to 1 connects the A/D input to the 8-1 multiplexer output defined by the 8-1 Multiplexer Select (see above).

Test Mode

This is a reserved bit for testing and must be set to 0 in all writes to Configuration Register 2.

A/D External Reference

Setting this bit to one allows use of an external reference to set the Full Scale Range of the A/D converter. The FSR is equal to 1.6 times the reference voltage.

Sleep Mode

Setting this bit to 1 forces the circuit into a low power standby mode. Configuration, offset and gain registers remain unchanged in sleep mode and the data output bus maintains a low impedance state.

Read Back Mode

This is a special diagnostic mode which can aid in the debugging of new system designs. Setting this bit to 1 allows all configuration, gain and offset register contents to be output on the data output bus (explained below).

Reading Register Data

In read-back mode the A/D output is bypassed and register data is placed on the 8 most significant bits of the data output bus. In parallel address mode (SER=0), register data is accessed by the A0-A2 address inputs. Register readback is dependent only on the state of configuration register 2, PB0. Read timing is shown in the timing diagrams.

In Serial addressing mode (SER=1), readback mode is enabled by setting PB0 in Configuration Register #2 equal to 1. Once readback mode has been enabled the LOAD pin must remain high to allow register addressing through the serial interface. In order to read a specific register shift in 3 bits of address data (MSB first), followed 8 dummy data bits. Register data will be valid after the 11th data bit is shifted in. In order to exit readback mode write configuration register #2, PB0=0.

Important:

The entire byte of register #2 is written when entering or exiting readback mode.

PGA Gain Settings

The gain for each color input is individually programmable from 1 to 10 in 256 linear steps.

$$PGA\ Gain = \left(\frac{Code}{256}\right) \cdot 9.0\ + 1.0$$

where Code represents the decimal contents of the binary 8-bit gain setting register.

Channel Offset Adjustment

The offset correction for each channel is programmable from -300mV to +300mV via an 8-Bit sign-magnitude DAC.

$$Channel\ Offset = PB7 \cdot \left[\frac{(Code)}{128}\right] \cdot 300mV$$

PB7= 1 equals -1

PB7= 0 equals +1

Code = (PB6:PB0) decimal content of the binary 8-bit offset register.

Theory of Operation (Correlated Double Sampling)

Correlated double sampling is a technique used to level shift and acquire CCD output signals whose information is equal to the difference between consecutive reference (black) and signal (video) samples. The CDS process consists of three steps:

1) Sampling and holding the reference black level.

2) Sampling the video level.

3) Subtracting the two samples to extract the video information.

Once the video information has been extracted it can be processed further through amplification and/or offset adjustment. Since system noise is also stored and subtracted during the CDS process, signals with bandwidths less than half the sampling frequency will be substantially attenuated. In order to reject higher frequency power supply noise which is not attenuated near the sampling frequency the XRD9820/22 utilizes a fully differential input structure. Since the CDS process uses AC coupled inputs the coupling capacitor must be charged to the common-mode range of the analog

front-end. This can be accomplished by clamping the coupling capacitor to the internal clamp voltage when the CCD is at a reference level. This clamp may occur during each pixel (Pixel Clamp), or at the beginning of each line (CDS Line Clamp). If CDS Line Clamp mode is used the input buffer (configuration register #1, PB1) must be enabled to eliminate the effects of input bias current. If Pixel mode is selected the input buffer is not required or recommended.

3-Channel CDS Mode

This mode allows simultaneous CDS of the red, green and blue inputs . Black-level sampling occurs on each pixel and is equal to the width of the BSAMP sampling input. The black level is held on the falling edge of BSAMP and the PGA will immediately begin to track the signal input until the falling edge of VSAMP. Two VSAMP timing modes are supported to allow additional flexibility in the VSAMP pulse width (see timing diagrams). At the end of the video sampling phase the difference between the reference and video levels is inverted, amplified and offset depending on the contents of the PGA gain and offset registers. The RGB channels are then sequentially converted by a high speed A/D converter. A/D converter data appears on the data output bus after TBD ADCCLK cycles . Channel synchronization occurs when the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The Red channel is always digitized first following synchronization and will be selected as long as the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The power up default mode is for CDS sampling a CCD input (Pixel Clamp, Inverting input, no input buffer).

1-Channel CDS Mode

The 1-Channel CDS mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode describe previously. To select a single channel input the color bits of configuration register 1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. In single color mode the SYNCH signal has no effect on synchronization but still affects clamping. (See Table 1). If the configuration is toggled from single color to 3-channel mode RGB scanning will not occur until the circuit is resynchronized with the SYNCH pulse.

3-Channel CIS/Sample and Hold Mode

The XRD9820/22 also supports operation for Contact Image Sensor (CIS) and S/H applications. Channel synchronization occurs when the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The Red channel is always digitized first following synchronization and will be selected as long as the rising edge of ADCCLK samples a logic 0 on the SYNCH input. For DC-coupled inputs the reference clamp and input buffer should be disabled and input polarity should be set to 1 (non-inverting). In this mode of operation the BSAMP input is connected to AGND and input sampling occurs on the falling edge of VSAMP.

When using AC coupled inputs the coupling capacitor must be clamped to the required common-mode input voltage when the signal source output is at a reference level. This can be accomplished by enabling the S/H Line clamp mode in configuration register 1 and clamping the input capacitor to the internal clamp voltage at the beginning of each line via the SYNCH input. The required width of the SYNCH signal is dependent on the value of the coupling capacitor, XRD9820/22 clamp resistance, source output resistance and desired accuracy. This is explained further in Coupling Capacitor Requirements. If AC coupling is used the input buffer (configuration register 1) must be enabled to eliminate input-bias current errors inherent to the sampling process. The input buffer is not required or recommended in DC coupled applications.

1-Channel CIS/ Sample and Hold Mode

The 1-Channel CIS S/H mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode with the exception that VSAMP timing option #2 is not supported. To select a single channel input the color bits of configuration register 1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. In single color mode the SYNCH signal has no effect on synchronization but still affects clamping. (See clamp mode). If the configuration is toggled from single color to 3-channel mode, RGB scanning will not occur until the circuit is resynchronized with the SYNCH pulse.

Power Supplies and Digital I/O

The XRD9820/22 utilizes separate analog and digital power supplies. All digital I/O pins are 3V/5V compatible and allow easy interfacing to external digital ASICs. For

single supply systems the analog and digital supply pins can be separately connected and bypassed to reduce noise coupling from digital to analog circuits.

Coupling Capacitor Requirements

The size of the external coupling capacitors depends on a number of items including the clamp mode, pixel rate, channel gain, black-level variation and system accuracy requirements. The major limitation for each clamp mode is shown below.

	CDS Mode	S/H Mode
Pixel Clamp (Buffer Disabled)	• Black level pixel-pixel variation • Initial charging	Not Applicable
Line Clamp (Buffer Enabled)	• Initial charging • Capacitor droop (common-mode range)	• Initial Charging • Capacitor droop (accuracy error)

Table 9. Coupling Capacitor Limitation

Maximum Capacitance (CDS Pixel Mode)

Limitation #1

Since the black-level is clamped during each pixel period the input bias current contributes an insignificant amount of droop during one pixel period. However, pixel-pixel variations in the black level may appear as errors . For a worst case gain of -10, 2V A/D FSR and 10-bit accuracy one lsb of error corresponds to 200uV input-referred. Assuming 2mV of pixel-pixel variation in the black level the maximum coupling capacitor can be determined as a function of the clamping period and internal clamp resistance.

$$C_{max} = \frac{tpwb}{(Rc + Rs) \cdot ln\left(\frac{2mV}{200\ \mu V}\right)}$$

where tpwb=clamp pulse width (BSAMP)

    Rc=Clamp resistance

    Rs=Signal source-resistance

For typical values of tpwb=100ns, Rc=100Ω, Rs=500Ω, $C_{MAX} \le 72pF$.

Limitation #2

The maximum input capacitance may also be limited by the time allowed to charge the input capacitor to the difference between the black level and clamp levels. The capacitor value can be related to the number of clamp pulses allowed before the capacitor voltage settles to within the desired accuracy.

$$C_{max} = \frac{tpwb \cdot N}{(Rc + Rs) \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where *tpwb= clamp pulse width (BSAMP)*

    N= number of pixels allowed to settle

    Rc=clamp resistance

    Rs=Signal source-resistance

    Vr= black level

    Vc=XRD9810 clamp voltage

    Vε=error voltage

Assuming that Vr=5V, Vc=4V, Vε=200uV, Rc=100Ω, Rs=500Ω, tpwb=100ns and N=10 the maximum allowable input capacitor is $\le$ 196pF. In this case the input capacitance is limited by pixel-pixel changes in the black level (first calculation).

Minimum Capacitance (CDS Pixel Mode)

The minimum coupling capacitance is limited by parasitic effects including pin and board capacitance. A minimum value of 68pF is recommended.

Maximum Capacitance (CDS Line Mode)

Since the coupling capacitor is charged only at the beginning of each line and not clamped at each pixel, the pixel-pixel variation in the black level has no effect on the capacitor size. The maximum size will be limited by the number of clamp pulses, clamp pulse-width and number of lines allowed to charge to a given accuracy.

$$C_{max} = \frac{N \cdot L \cdot tpwb}{(Rc + Rs) \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where tpwb= clamp pulse width (BSAMP)

> *N= number of clamp pulses at beginning of each line.*
>
> *L = number of lines to clamp to desired accuracy.*
>
> *Rc=clamp resistance*
>
> *Rs=Signal source-resistance*
>
> *Vr= black level*
>
> *Vc=XRD 9810 clamp voltage*
>
> *Vε=error voltage*

Assuming that Vr=5V, Vc=4V, Vε=200uV, Rc=100Ω, Rs=500Ω, tpwb=100ns N=10, L=2 the maximum allowable input capacitor is equal to 392pF. If it is desired to settle within one line (L=1) for a given capacitor value, the number of clamp pulses or the clamp pulse-width must be increased using the above equation.

Minimum Capacitance (CDS Line Mode)

In general the minimum value coupling capacitance is limited by the amount of droop which can occur before the input voltage range of the input amplifier is exceeded. The input capacitor droop is related to the input bias current by:

$$Vdroop = \frac{Ibias \cdot n \cdot T}{C}$$

where I_{bias} =input bias current

> *n=number of pixels per line*
>
> *T=pixel period*

If the minimum input voltage is allowed to equal the 0V input voltage of the XRD9810, the maximum allowable droop will be equal to the clamp level minus the difference between the black and video levels. For example if Vc=4V, and the CCD video output is -2V relative to the black level the maximum allowable droop is equal to 2V.

Using the previous equation and assuming T=500ns, n=3000

$$C \, min = \frac{10 \, nA \cdot 3000 \cdot 500 \, ns}{2V} = 7.5pF$$

$$Vdroop = \frac{Ibias \cdot T}{2 \cdot C \, min}$$

Note:

> *These are the absolute minimum capacitor requirements. As stated for pixel-mode a minimum value of 68pF is recommended.*

Minimum Capacitance (S/H Line Mode)

Unlike Line or Pixel CDS modes voltage droop across a line appears as an absolute error and is the dominant factor in determining the minimum coupling capacitor size.

$$C \, min = \frac{Ibias \cdot n \cdot T}{V\varepsilon}$$

where I_{bias}=input bias current

> *n=number of pixels per line*
>
> *T=pixel period*

Assuming n=3000, T=500nS, I=10nA and Vε=200uV the minimum required capacitor is 75nF.

Maximum Capacitance (S/H Line Mode)

The maximum capacitance is determined by the amount of time allowed to charge the coupling capacitor. In order to minimize the charging time the maximum capacitor can be set to the minimum value as previously calculated. In this case the time required to charge the capacitor is:

$$t = (Rs + Rc) \cdot C \, min \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)$$

where t= clamp pulse -width ($\overline{SYNCH}$)

> *Rc=clamp resistance*
>
> *Rs=Signal source-resistance*
>
> *Vr= Input reference level*
>
> *Vc=XRD9810 clamp voltage*
>
> *Vε=error voltage*
>
> *Cmin = coupling capacitor*

Assuming that Vr=.5 Vc=0V, Vε=200uV, Rc=100Ω, Rs=500Ω and C=75nF, the minimum clamp period is equal to 352μS.
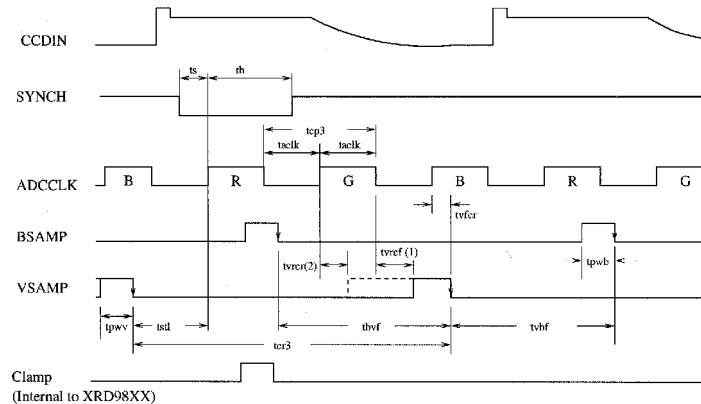
3 Channel CDS Mode - Pixel Clamp

Configuration Register #1 Pixel Clamp (PB7=0, PB6=0)
RGB (PB4=0, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Disabled (PB1=0)
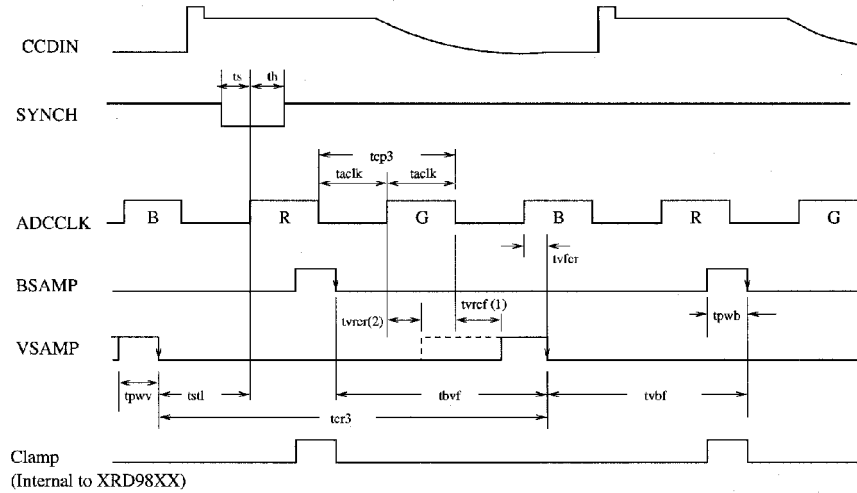
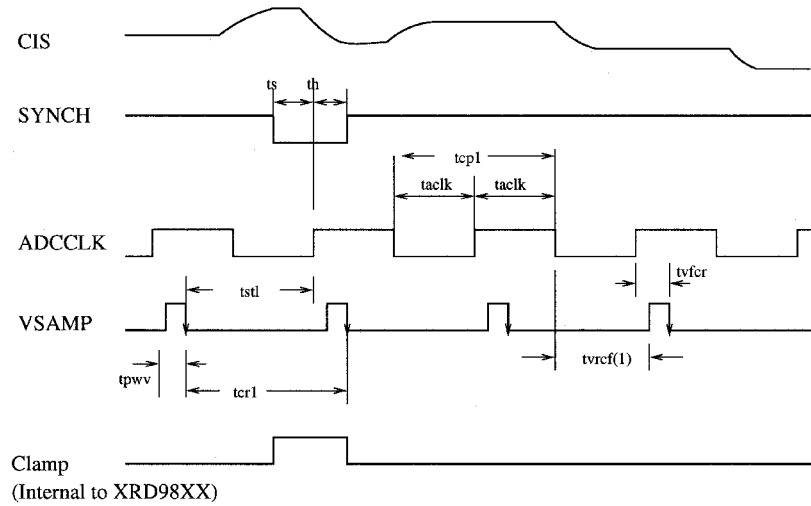| CDS Mode Event Table	
Event	**Action**
↑BSAMP	Connect CDS Inputs and Track Black Level
↓BSAMP	Hold Black Level and Track Video Level
VSAMP * ADCCLK	Reset PGA (Vsamp and ADCCLK both must be high for AMW of 30ns)
↓VSAMP	Hold Video Level

3 Channel CDS Mode - Line Clamp

Configuration Register #1 CDS Line (PB7=0, PB6=1)
RGB (PB4=0, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Enabled (PB1=1)

Notes: (1) VSAMP Timing option #1 uses tvrcf. (tvrcr is not required).
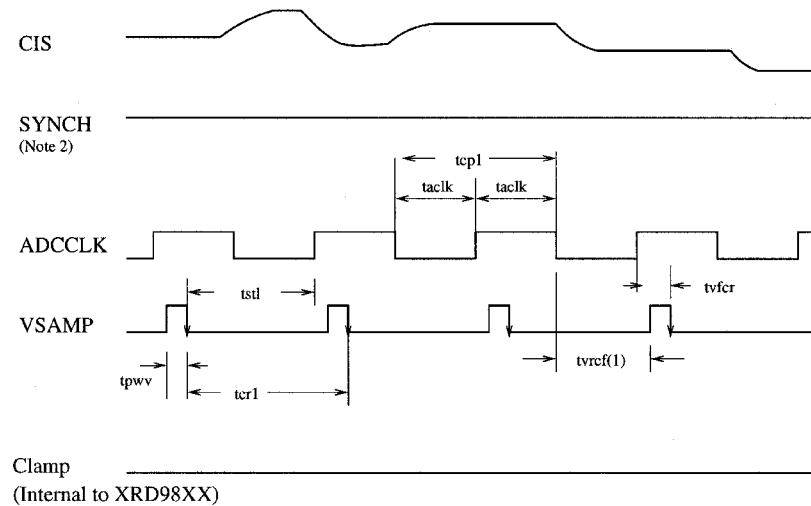(2) VSAMP Timing option #2 uses tvrcr. (tvrcf is not required).

1 Channel CDS Mode - Pixel Clamp

Configuration Register#1 Pixel Clamp (PB7=0, PB6=0)
Green Channel (PB4=1, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Disabled (PB1=0)

CCDIN

SYNCH
(Note 2)

ADCCLK

BSAMP

VSAMP

Clamp
(Internal to XRD98XX)
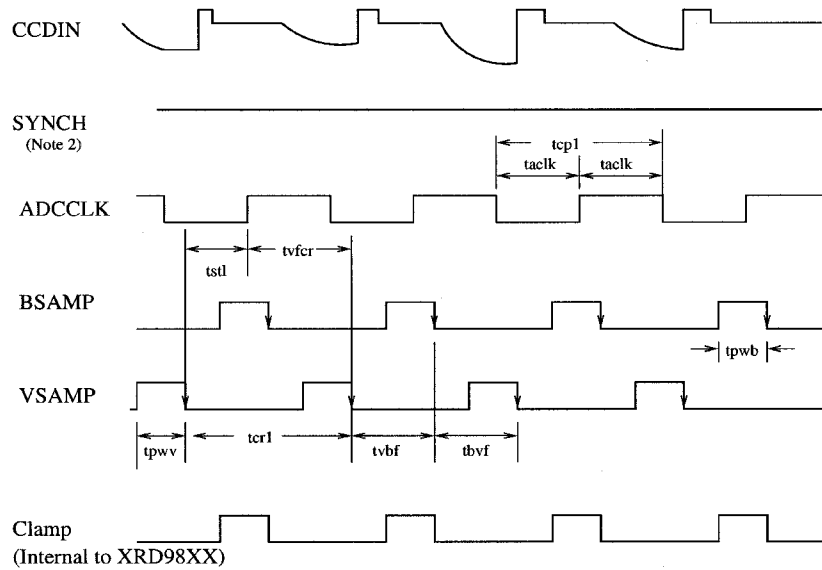
1 Channel CDS Mode - CDS Line Clamp

Configuration Register#1 CDS Line Clamp (PB7=0, PB6=1)
Green Channel (PB4=1, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Enabled (PB1=1)
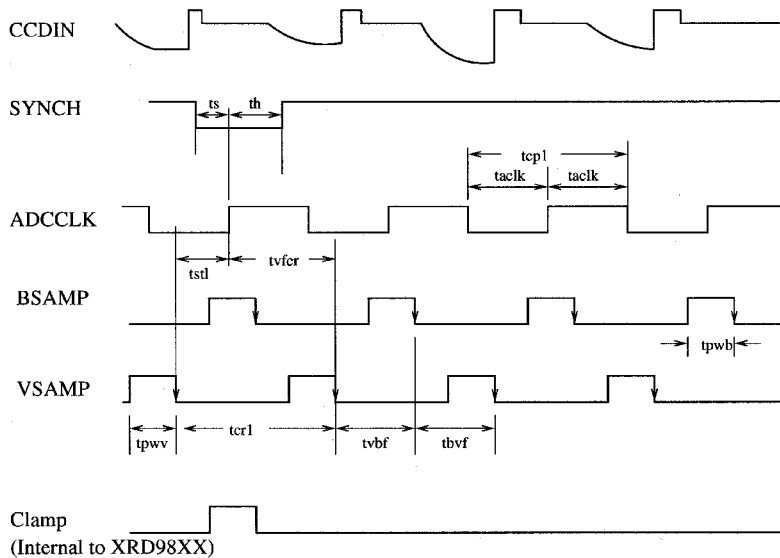
CCDIN

SYNCH

ADCCLK

BSAMP

VSAMP

Clamp
(Internal to XRD98XX)

Notes: (1) Only VSAMP timing option #1 is supported in 1-Channel mode.
 (2) Force SYNCH to logic 1 in 1-Channel Pixel-Clamp Mode

3 Channel S/H Mode - Line Clamp (AC Coupled)

Configuration Register#1   S/H Line Clamp (PB7=1, PB6=1)
RGB (PB4=0, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Enabled (PB1=1)
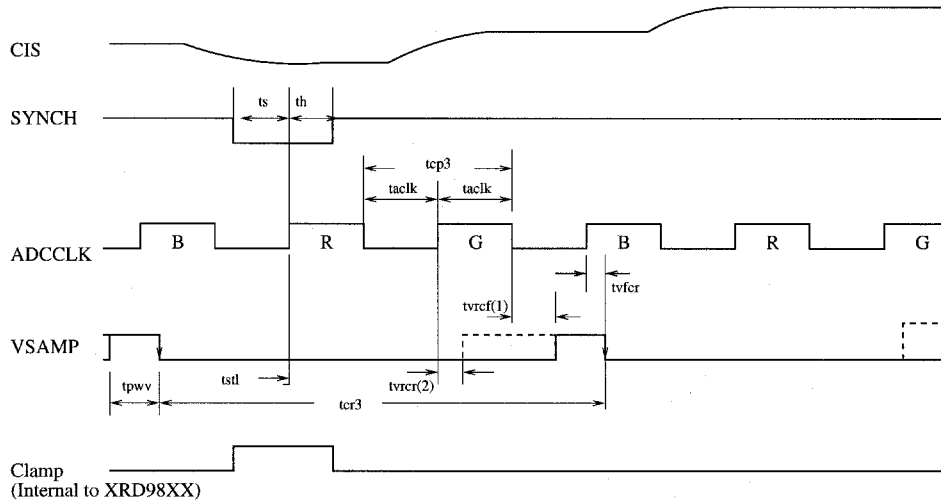
3 Channel S/H Mode -No Clamp (DC Coupled)

Configuration Register#1   No Clamp (PB7=1, PB6=0)
RGB (PB4=0, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Disabled (PB1=0)
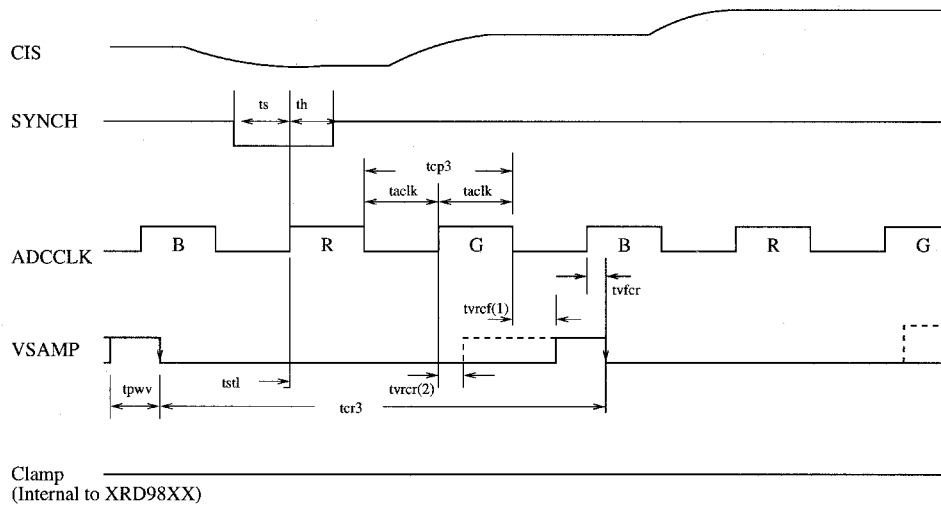
Notes: (1) VSAMP Timing option #1 uses tvrcf. (tvrcr is not required).
(2) VSAMP Timing option#2 uses tvrcr. (tvrcf is not required).

1 Channel S/H Mode - Line Clamp (AC Coupled)

Configuration Register #1 S/H Line (PB7=1, PB6=1)
Green Channel(PB4=1, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Enabled (PB1=1)

CIS

SYNCH

ts   th

ADCCLK

tcp1

taclk   taclk

VSAMP

tstl

tvfcr

tpwv

tcr1

tvrcf(1)

Clamp
(Internal to XRD98XX)

1 Channel S/H Mode - No Clamp (DC Coupled)

Configuration Register #1 S/H Line (PB7=1, PB6=1)
Green Channel(PB4=1, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Disabled (PB1=0)

CIS

SYNCH
(Note 2)

ADCCLK

tcp1

taclk   taclk

VSAMP

tstl

tvfcr

tpwv

tcr1

tvrcf(1)

Clamp
(Internal to XRD98XX)

Notes:(1) Only VSAMP timing option #1 is supported in 1-Channel mode.
(2) Force SYNCH to logic 1 in 1-Channel No-Clamp Mode

Parallel Mode
Write Timing
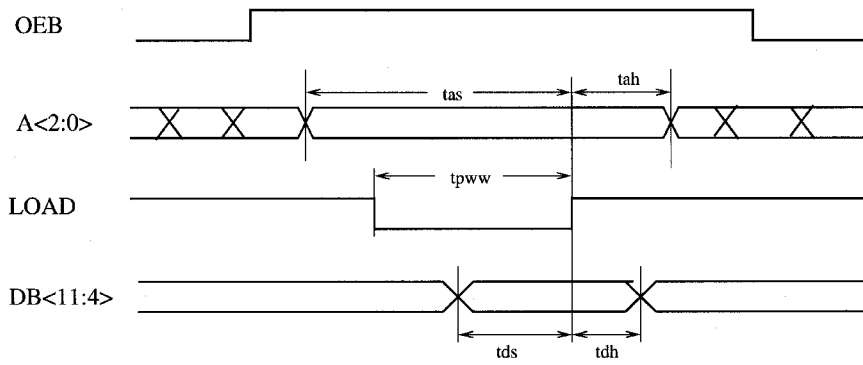
Read-Back Mode Timing
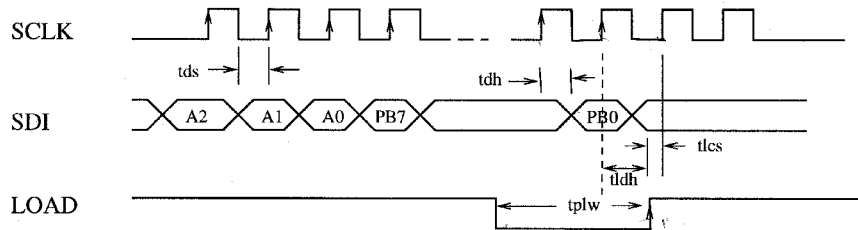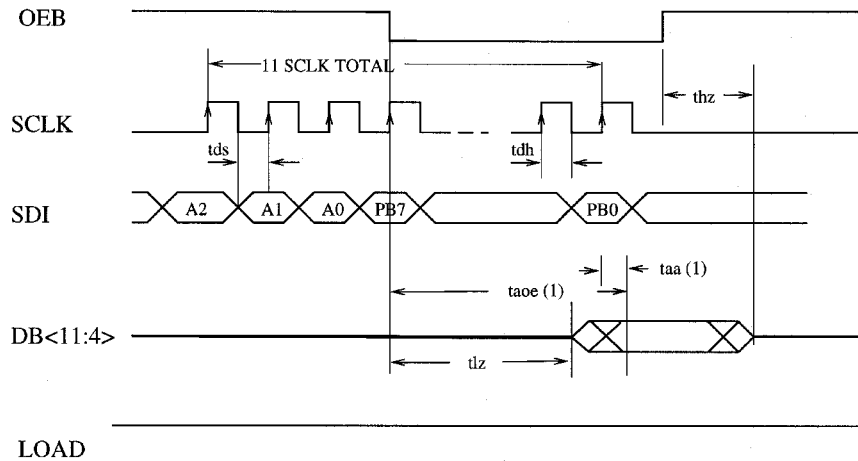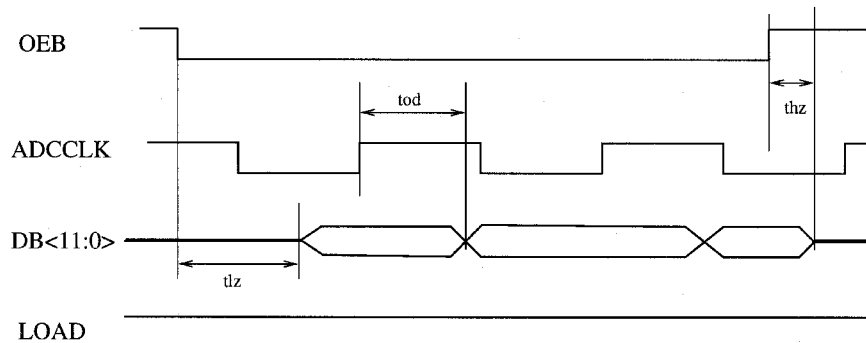(Readback Mode Enabled, PB0=1, Register #2)
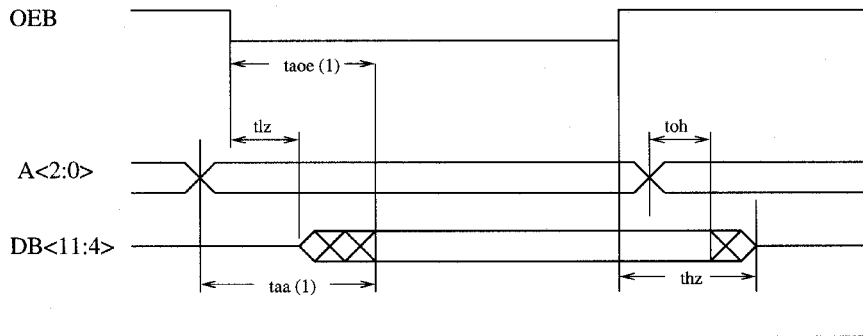
Note 1. Start of valid data depends on whcih timing becomes effective last taoe or taa.

ADC Digital Output Timing
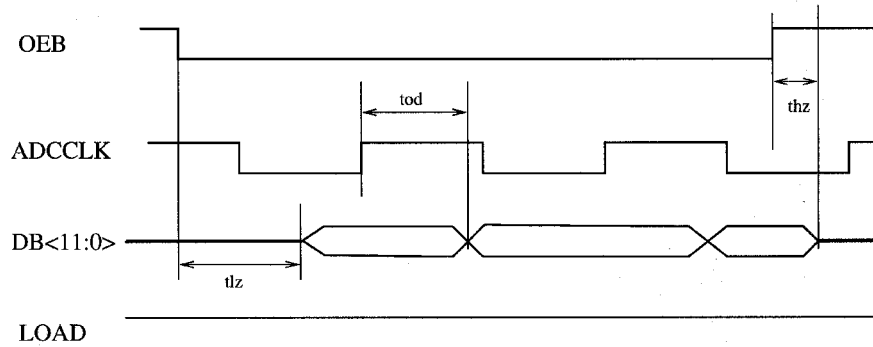
Write Timing

Read-Back Mode Timing
(Readback Mode Enabled, PB0=1, Register #2)

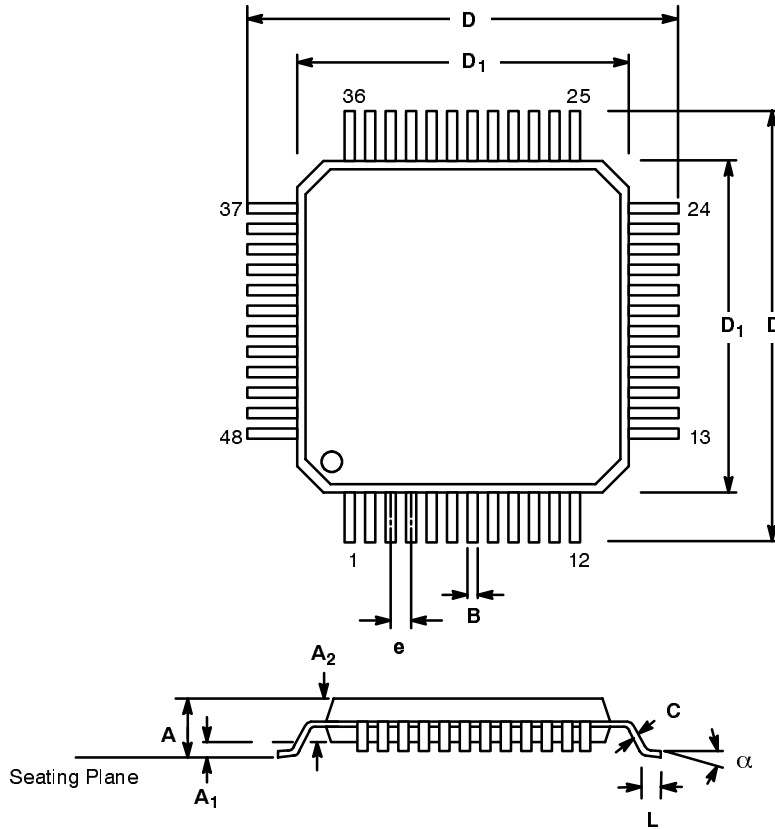Note 1. Start of valid data depends on whcih timing becomes effective last taoe or taa.

ADC Digital Output Timing

48 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.0 mm, TQFP)

Rev. 1.00

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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