



**Genesys Logic, Inc.**

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**GL860**

**USB 2.0 PC Camera Controller**

**Datasheet Revision 1.01**

**Jan. 04, 2006**



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## Revision History

Revision	Date	Description
0.10	04/29/2004	First draft release
0.20	05/25/2004	<ol style="list-style-type: none"> <li>1. Added Pin List and Pin Description in Chapter 3.</li> <li>2. Changed Features contents in Chapter 2.</li> <li>3. Changed CCD/CMOS Sensor interface function description in Chapter 4.</li> </ol>
0.30	06/25/2004	Changed mass contents.
0.40	07/26/2004	<ol style="list-style-type: none"> <li>1. Removed 32-pin QFN package.</li> <li>2. Changed 64-pin name.</li> <li>3. Added 100-pin PQFP package</li> </ol>
0.90	11/10/2004	First draft release
1.00	09/27/2005	<ol style="list-style-type: none"> <li>1. Modify pin list and description.</li> <li>2. Added and modify sensor register.</li> <li>3. Remove pin 64 pin list and pin decription.</li> <li>4. Remove features "Complies with USB Video Class specification rev. 1.0".</li> </ol>
1.01	01/04/2006	<ol style="list-style-type: none"> <li>1. Add 48 pin assignment.</li> <li>2. Add 48 pin Descriptions</li> <li>3. Add Application circuit</li> </ol>

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### CHAPTER 1 GENERAL DESCRIPTION

The GL860 is a high performance USB 2.0 controller for PC Camera application. With the Genesys Logic's highly recognized self-developed USB high-speed transceiver, GL860 provides up to 480Mbps bandwidth for fulfilling the mass bandwidth demand of video transferring. GL860 also support USB isochronous mode to provide certain bandwidth to insure user can get satisfied usage experience on video application even running high bandwidth consumption devices concurrently.

The GL860 integrates a highly flexible sensor interface to make it easily adopted with variety sensors in which include most popular CCD sensor module and CMOS sensors. The GL860's low power consumption, low operation temperature characteristic also make it is easy to implement a high quality PC Camera without worry about the noise signals of sensors to affect by high performance USB controller.

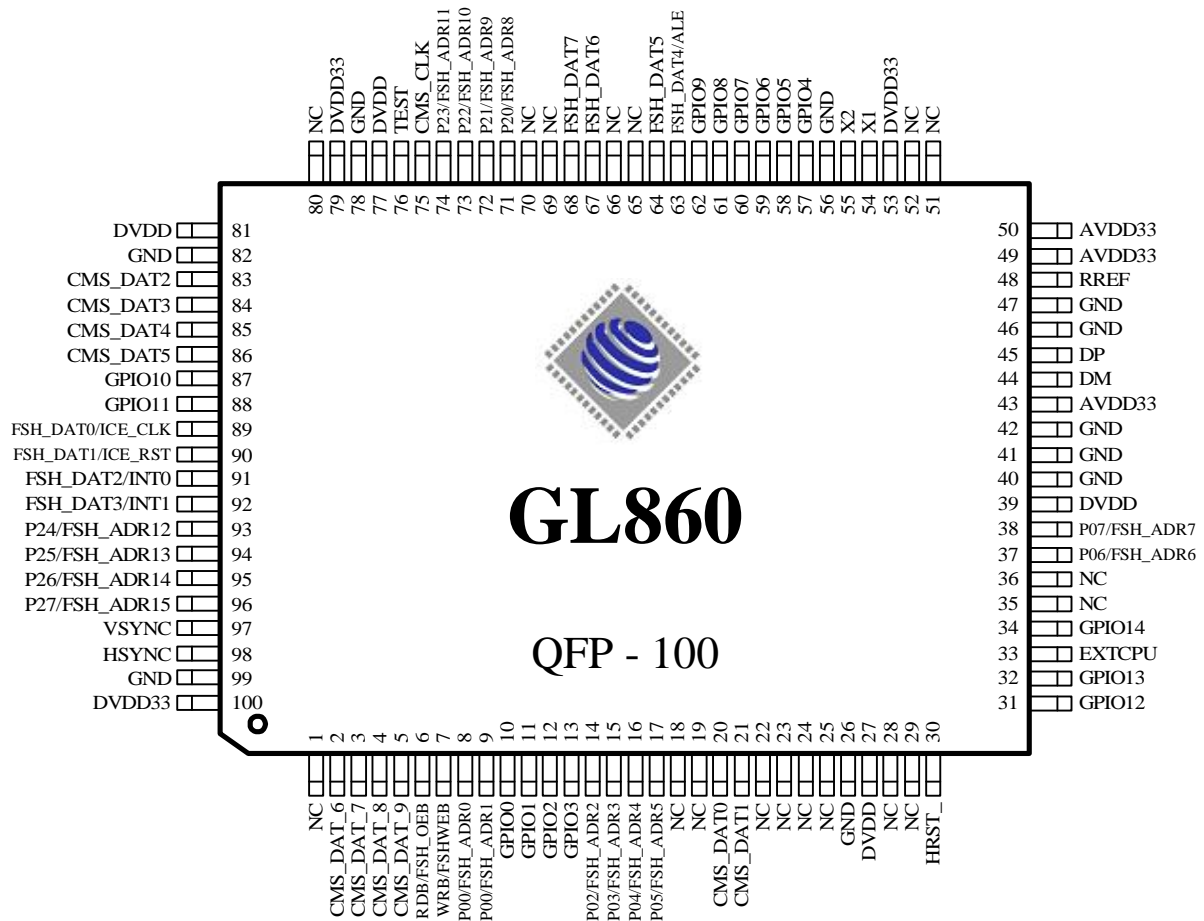


## CHAPTER 2 FEATURES

- I USB specification compliance
  - Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Complies with 12Mbps Universal Serial Bus specification rev. 2.0..
  - Support USB 2.0 Isochronous Video pipe to 24MB/s.
- I Sensor interface
  - Programmable interface for popular general CCD module/CMOS sensor
- I Non-processing video streaming (USB High-speed connection)
- I Support 4 USB endpoints
  - Endpoint 0: Control PIPE.
  - Endpoint 1: Isochronous/Bulk data in (configurable).
  - Endpoint 2: Interrupt OUT.
  - Endpoint 3: Interrupt IN.
- I Embedded 8052 micro-controller
  - Operate @ 15 MHz clock.
  - 8K ROM.
- I Support firmware stored in external FLASH memory for development of customer's firmware
- I Support USB remote wakeup.
- I Maximum 15 GPIO ports.
- I 3.3V/1.8V operation.
- I 3.3V to 1.8V regulator is built-in.
- I Capability to support on-line download program
- I Available in 100-pin QFP and 48-pin LQFP/QFN/LQFN package.

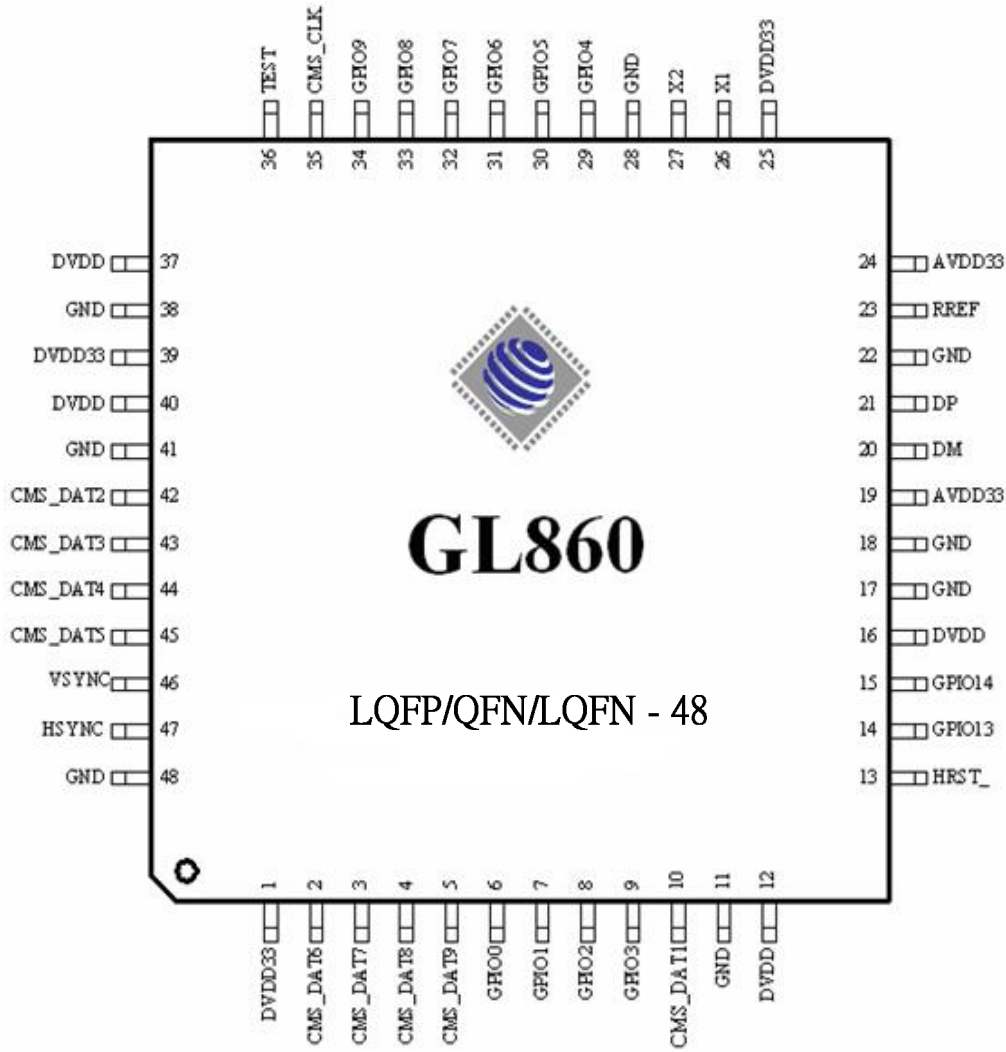
## CHAPTER 3 PIN ASSIGNMENT

### 3.1 Pinout



**Figure 3.1 - 100 Pin QFP Pinout Diagram**





**Figure 3.2 - 48 Pin LQFP/QFN/LQFN Pinout Diagram**



### 3.2 Pin List

Three type packages:

#### Case 1

- | 100 pin
- | w/ICE and flash memory
- | 10 bit sensor interface
- | 15 GPIO pins
- | QFP package

#### Case 2

- | 48 pin
- | 8 bit sensor interface
- | 12 GPIO pins
- | LQFP/QFN/LQFN package

**Table 3.1 - 100-Pin QFP Pin List**

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	NC	-	26	GND	P	51	NC	-	76	TEST	I
2	CMS_DAT6	I	27	DVDD	P	52	NC	-	77	DVDD	P
3	CMS_DAT7	I	28	NC	-	53	DVDD33	P	78	GND	P
4	CMS_DAT8	I	29	NC	-	54	X1	I	79	DVDD33	P
5	CMS_DAT9	I	30	HRST_	I	55	X2	I/O	80	NC	P
6	FSH_OEB	I	31	GPIO12	I/O	56	GND	P	81	DVDD	P
7	FSH_WEB	I	32	GPIO13	I/O	57	GPIO4	I/O	82	GND	P
8	FSH_ADR0	I/O	33	EXTCPU	I	58	GPIO5	I/O	83	CMS_DAT2	I
9	FSH_ADR1	I/O	34	GPIO14	I/O	59	GPIO6	I/O	84	CMS_DAT3	I
10	GPIO0	I/O	35	NC	-	60	GPIO7	I/O	85	CMS_DAT4	I
11	GPIO1	I/O	36	NC	-	61	GPIO8	I/O	86	CMS_DAT5	I
12	GPIO2	I/O	37	FSH_ADR6	I/O	62	GPIO9	I/O	87	GPIO10	I/O
13	GPIO3	I/O	38	FSH_ADR7	I/O	63	FSH_DAT4	I/O	88	GPIO11	I/O
14	FSH_ADR2	I/O	39	DVDD	P	64	FSH_DAT5	I/O	89	FSH_DAT0	I/O
15	FSH_ADR3	I/O	40	GND	P	65	NC	-	90	FSH_DAT1	I/O
16	FSH_ADR4	I/O	41	GND	P	66	NC	-	91	FSH_DAT2	I/O
17	FSH_ADR5	I/O	42	GND	P	67	FSH_DAT6	I/O	92	FSH_DAT3	I/O
18	NC	-	43	AVDD33	P	68	FSH_DAT7	I/O	93	FSH_ADR12	I/O
19	NC	-	44	DM	I/O	69	NC	-	94	FSH_ADR13	I/O
20	CMS_DAT0	I	45	DP	I/O	70	NC	-	95	FSH_ADR14	I/O
21	CMS_DAT1	I	46	GND	P	71	FSH_ADR8	I/O	96	FSH_ADR15	I/O
22	NC	-	47	GND	P	72	FSH_ADR9	I/O	97	VSYNC	I
23	NC	-	48	RREF	A	73	FSH_ADR10	I/O	98	HSYNC	I
24	NC	-	49	AVDD33	P	74	FSH_ADR11	I/O	99	GND	P
25	NC	-	50	AVDD33	P	75	CMS_CLK	I/O	100	DVDD33	P

**Table 3.2 - 48-Pin LQFP/QFN/LQFN Pin List**

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DVDD33	P	13	HRST_	I	25	DVDD33	P	37	DVDD	P
2	CMS_DAT6	I	14	GPIO13	I/O	26	X1	I	38	GND	P
3	CMS_DAT7	I	15	GPIO14	I/O	27	X2	I/O	39	DVDD33	P
4	CMS_DAT8	I	16	DVDD	P	28	GND	P	40	DVDD	P
5	CMS_DAT9	I	17	GND	P	29	GPIO4	I/O	41	GND	P
6	GPIO0	I/O	18	GND	P	30	GPIO5	I/O	42	CMS_DAT2	I
7	GPIO1	I/O	19	AVDD33	P	31	GPIO6	I/O	43	CMS_DAT3	I
8	GPIO2	I/O	20	DM	I/O	32	GPIO7	I/O	44	CMS_DAT4	I
9	GPIO3	I/O	21	DP	I/O	33	GPIO8	I/O	45	CMS_DAT5	I
10	CMS_DAT1	I/O	22	GND	P	34	GPIO9	I/O	46	VSYNC	I/O
11	GND	P	23	RREF	A	35	CMS_CLK	I/O	47	HSYNC	I/O
12	DVDD	P	24	AVDD33	P	36	TEST	I	48	GND	P

### 3.3 Pin Descriptions

**Table 3.3 - 100-Pin QFP Pin Descriptions**

Pin Name	Pin#	Type	Description
DVDD	27,39,77,81	P	1.8V core power
CMS_DAT0~9	20,21,83~86, 2~5	I	Sensor data bit 0~9
FSH_OEB	6	I	Read strobe of Output enable for flash memory. Low active
FSH_WEB	7	I	Write strobe of Write enable for flash memory. Low active
FSH_ADR0~15	8,9,14~17, 37,38,71~74, , 93~96	I/O	Port 0 and Port 2 for Address of flash memory
GPIO0~14	10~13,57~62, 87,88,31,32,34	I/O (pd)	GPIO pins bit 0~14
GND	26,40,41,42, 46,47,56,78, 82,99	P	Ground
HRST_	30	I (pu)	Hardware reset, low active
EXTCPU	33	I	Use external CPU mode for firmware development.
AVDD33	43,49,50	P	3.3V analog power
DM	44	I/O	USB D-
DP	45	I/O	USB D+
RREF	48	A	Reference R
DVDD33	53,79,100	P	3.3V power
X1	54	I	12M crystal in
X2	55	I/O	12M crystal out
FSH_DAT0~7	89,90,91,92, 63,64,67,68	I/O	Data bus of flash memory
CMS_CLK	75	I/O	Sensor clock
TEST	76	I (pd)	Test mode
VSYNC	97	I/O	Sensor Vsync
HSYNC	98	I/O	Sensor Hsync
NC	1,18,19,22~25, 28,29,35,36, 51,52,65,66, 69,70,80	-	No connection

**Table 3.4 - 48-Pin LQFP/QFN/LQFN Pin Descriptions**

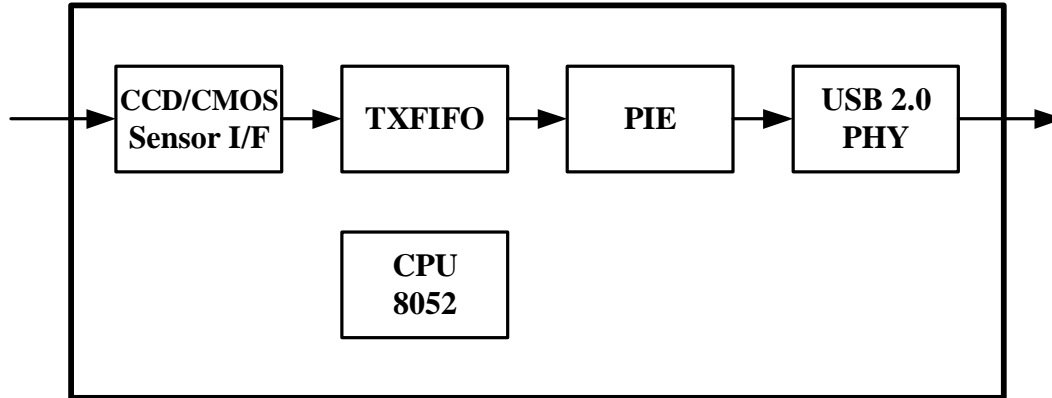
Pin Name	Pin#	Type	Description
DVDD	12,16,37,40	P	1.8V power for crystal
CMS_DAT1~9	10,42~45,2~5	I	Sensor data bit 1~9
GPIO0~9,13,14	6~9,29~34, 14,15	I/O (pd)	GPIO pins bit 0~9,13,14
GND	11,17,18,22, 28,38,41,48	P	Ground
DVDD33	1,25,39	P	3.3V core power
HRST	13	I (pu)	Hardware reset, low active
AVDD33	19,24	P	3.3V analog power
DM	20	I/O	USB D-
DP	21	I/O	USB D+
RREF	23	A	Reference R
X1	26	I	12M crystal in
X2	27	I/O	12M crystal out
CMS_CLK	35	I/O	Sensor clock
TEST	36	I (pd)	Test mode
VSYNC	46	I/O	Sensor Vsync
HSYNC	47	I/O	Sensor Hsync
NC	10	-	No connection

**Notation:**

<b>Type</b>	<b>O</b>	Output
	<b>I</b>	Input
	<b>B</b>	Bi-directional
	<b>B/I</b>	Bi-directional, default input
	<b>B/O</b>	Bi-directional, default output
	<b>P</b>	Power / Ground
	<b>A</b>	Analog
	<b>pu</b>	Internal pull up
	<b>pd</b>	Internal pull down
	<b>odpu</b>	Open drain with internal pull up

## CHAPTER 4 FUNCTIONAL DESCRIPTION

### 4.1 Function Block



**Figure 4.1 - Block Diagram**

#### I CCD Module/CMOS Sensor Interface

GL860 can link with popular CMOS sensor on market for PC camera application. GL860 can be configured by different sensor requirement. If sensor is acting as master, GL860 can accept HSYNC/VSYNC from sensor. If GL860 is configured as a master HSYNC/VSYNC will be provided by GL860 to sensor. GL860 keep the most flexibility to fit most of the sensors. The detail of configuration needs to refer to GL860 Application Note. For most sensors no matter of YUV format or RGB format, they can be easily transferred image data to PC by GL860.

#### I TXFIFO

GL860 build in 6K byte internal buffer for USB high bandwidth application. This 6K internal buffer can be used as transmitted buffer of isochronous pipe or bulk pipe. In USB specification, the highest bandwidth of isochronous pipe is 24M byte/second, that can be easily derived to maximum frame rate depending on configuration. For example, frame rate can be easily achieved to 30 frames per second if image size is 640 x 480 if raw data output and sensor clock is 15M.

#### I PIE

PIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with CPU to play the role of the chip's kernel. The main functions of PIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB1.1, bit stuffing/de-stuffing is implemented in UTMI, not in PIE.

#### I USB 2.0 PHY (UTMI )

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB2.0 test modes, and serial/parallel conversion.

#### I CPU

CPU is the micro-processor unit of GL860. It is an 8-bit 8052 processor with 8K ROM and 256 bytes RAM. It operates at 15Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition,  $\mu$ C can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of chip. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.



### 4.2 Operation Mode

For customized firmware, flash memory can use as external program memory of CPU. This is for customer to develop their firmware. This is only available for 100-pin package type.

#### 4.2.1 with Flash Memory

- | Only available in 100-pin QFP package
- | Force EXTCPU = 0
- | GPIO9 pull down
- | GPIO13/GPIO14 used as serial bus to configure sensor

#### 4.2.2 without Flash Memory

- | If 100 pin, set EXTCPU = 0
- | GPIO9 pull down
- | GPIO13/GPIO14 are used as serial bus to configure sensor



## CHAPTER 5 ELECTRICAL CHARACTERISTICS

### 5.1 Maximum Ratings

**Table 5.1 - Maximum Ratings**

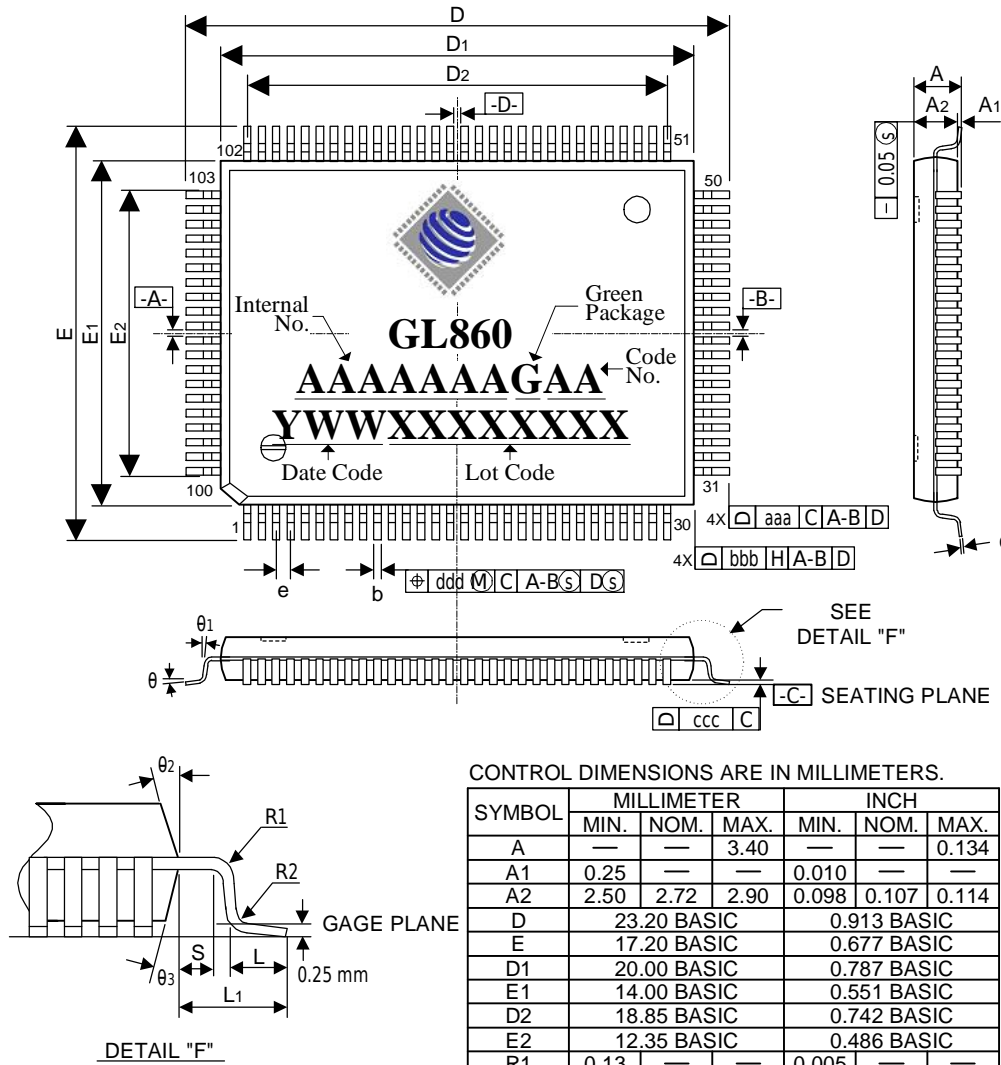
Symbol	Parameter	Min.	Max.	Unit
V <sub>IN</sub>	3.3V Input Voltage	3.0	3.6	V
T <sub>A</sub>	Ambient Temperature under bias	0	+100	°C
F <sub>OSC</sub>	Frequency	12 MHz ± 500ppm		

### 5.2 DC Characteristics

**Table 5.2 - DC Characteristics Except USB Signals**

Symbol	Parameter	Min.	Typ.	Max.	Unit
P <sub>D</sub>	Power Dissipation	-	-	-	mA
V <sub>DD</sub>	Power Supply Voltage	3	3.3	3.6	V
V <sub>IL</sub>	LOW level input voltage	-	-	0.9	V
V <sub>IH</sub>	HIGH level input voltage	2.0	-	-	V
V <sub>TLH</sub>	LOW to HIGH threshold voltage	1.36	1.48	1.62	V
V <sub>THL</sub>	HIGH to LOW threshold voltage	1.36	1.48	1.62	V
V <sub>OL</sub>	LOW level output voltage when I <sub>OL</sub> =8mA	-	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage when I <sub>OH</sub> =8mA	2.4	-	-	V
I <sub>OLK</sub>	Leakage current for pads with internal pull up or pull down resistor	-	-	-	μA
R <sub>DN</sub>	Pad internal pull down resistor	-	-	-	Ω
R <sub>UP</sub>	Pad internal pull up resistor	-	-	-	Ω

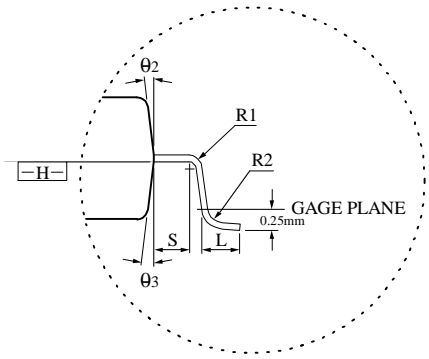
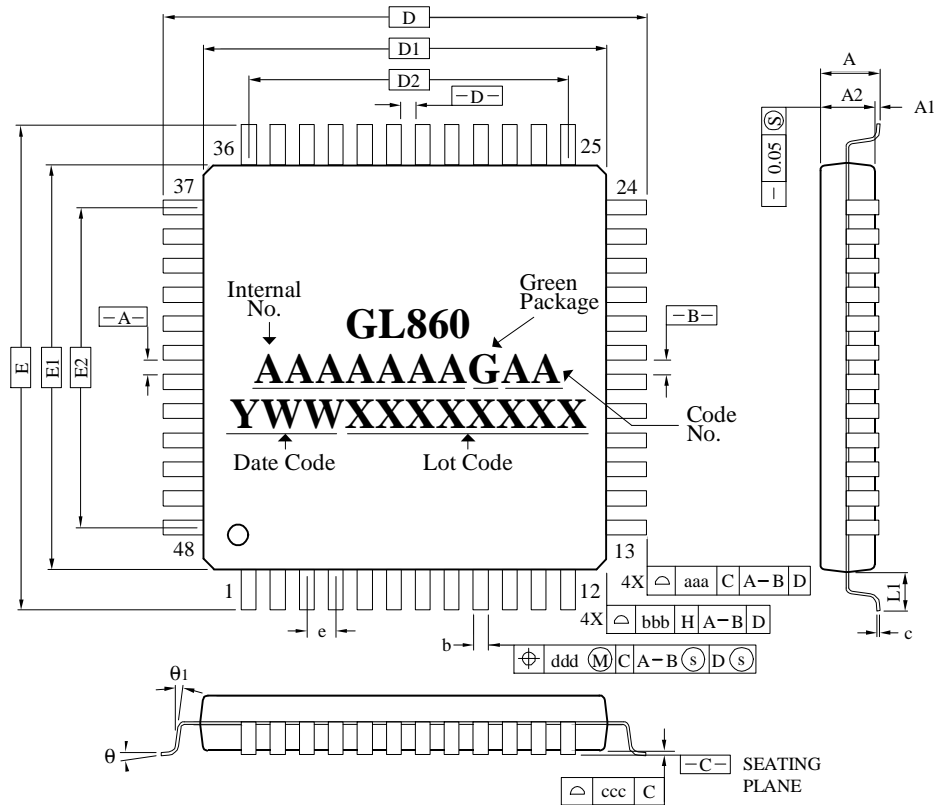
## CHAPTER 6 PACKAGE DIMENSION



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 6.1 - GL860 100 Pin QFP Package



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

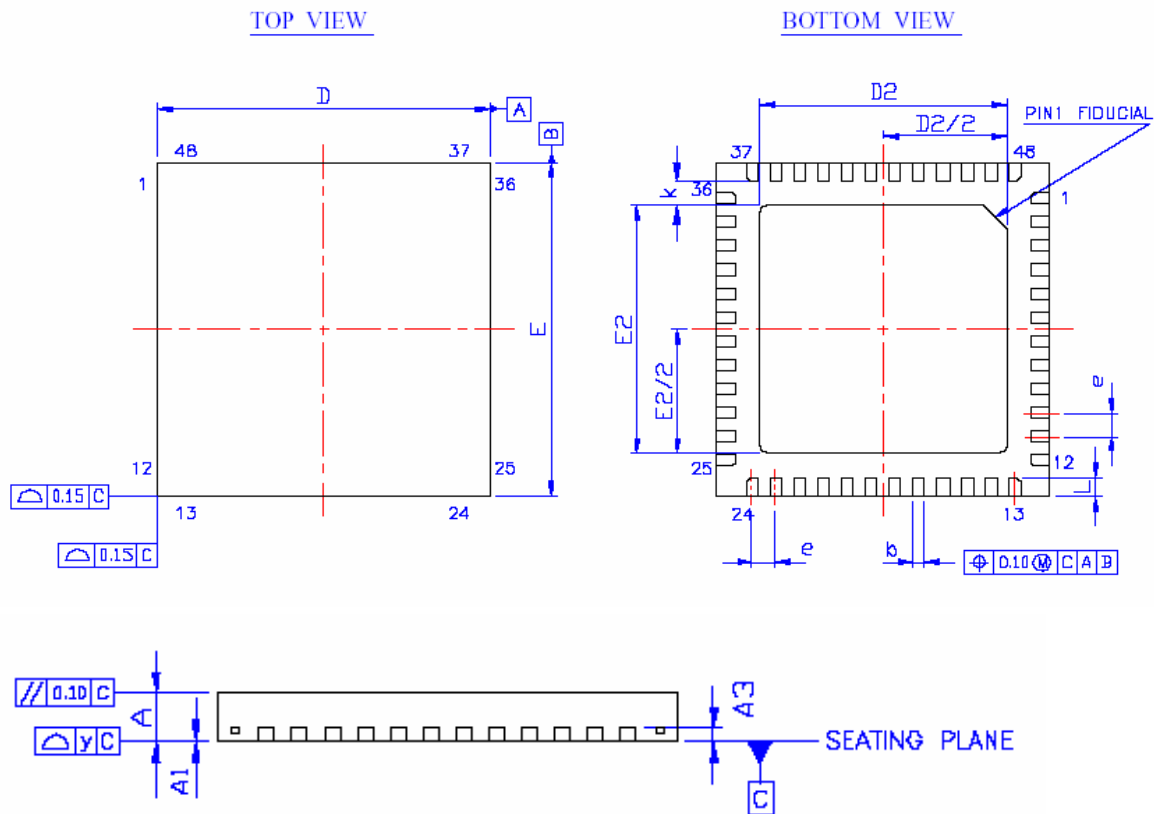
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20		0.008			
bbb	0.20		0.008			
ccc	0.08		0.003			
ddd	0.08		0.003			

Figure 6.2 - GL860 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.20 (8) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	7.00 (276) BSC		
E	7.00 (276) BSC		
D2	5.10 (201)	5.20 (205)	5.30 (209)
E2	5.10 (201)	5.20 (205)	5.30 (209)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	---	0.08 (3)
k	0.20 (8)	---	---

NOTE: 1. REFER TO JEDEC MO-220  
2. ALL DIMENSIONS IN MILLIMETERS.



**Figure 6.3 - GL860 48 Pin QFN Package**

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.13 (5) REF		
b	0.19 (7)	0.25 (10)	0.30 (12)
D	7.00 (276) BSC		
E	7.00 (276) BSC		
D2	5.10 (201)	5.20 (205)	5.30 (209)
E2	5.10 (201)	5.20 (205)	5.30 (209)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.20 (8)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

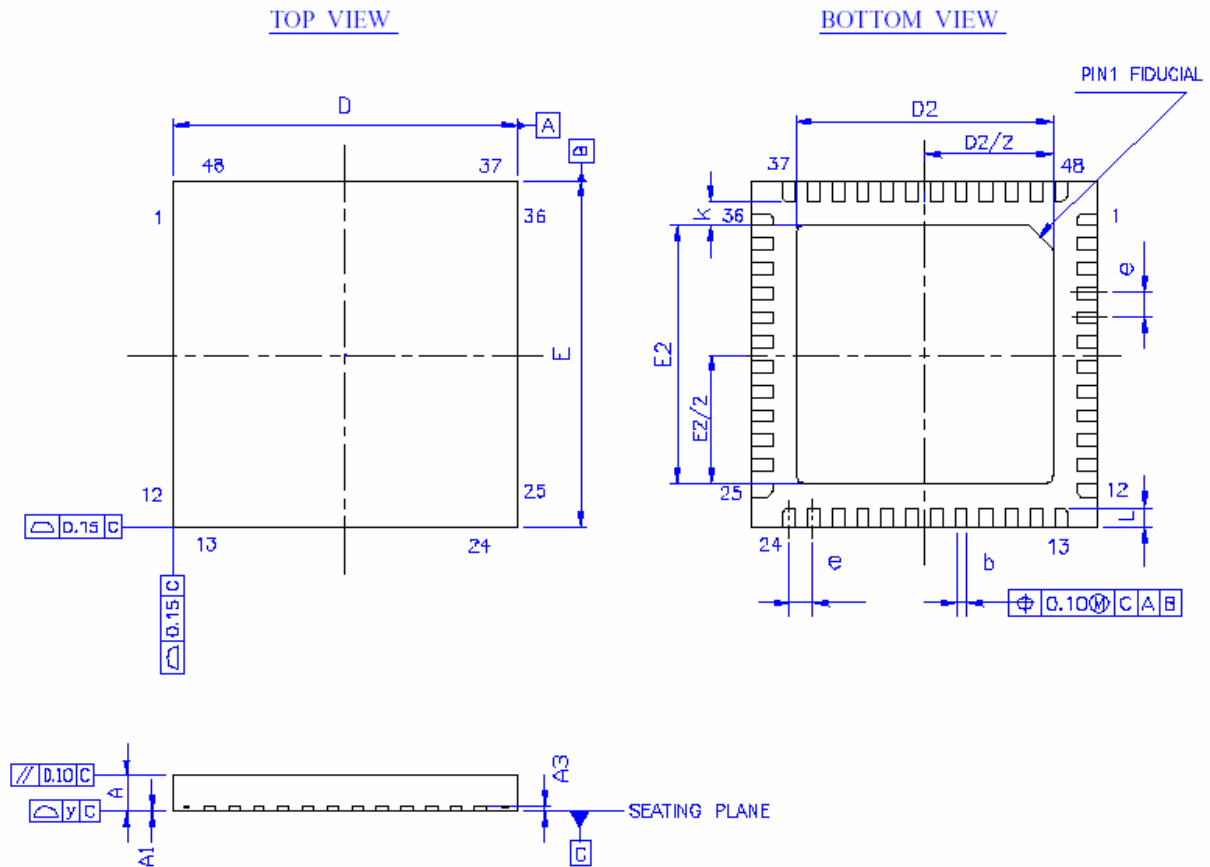


Figure 6.4 - GL860 48 Pin LQFN Package

## CHAPTER 7 ORDERING INFORMATION

Table 7.1 - Ordering Information

Part Number	Package	Status
GL860	100-pin QFP	
GL860	48-pin LQFP/QFN/LQFN	

## Appendix A. Application circuit

The schematic below represents a very basic example to the controller and is subject to variations depending on application intentions.

