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TECHNICAL SPECIFICATION

MODEL NO. : P64AN2AP04

Customer's Confirmation

Date _____

By _____

PVI's Confirmation

Confirmed By _____

Prepared By _____

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Date : Apr. 14,1999

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TECHNICAL SPECIFICATION

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1. Application

This technical specification applies to 6.4" color TFT-LCD module, P64AN2. The applications of the panel are car TV, portable TV, multimedia applications and others AV system.

2. Features

- . Compatible with NTSC and PAL system
- . Pixel in stripe configuration
- . Slim and compact
- . High Brightness
- . Optimum Viewing Direction : 6 o'clock
- . Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	6.4 (diagonal)	inch
Display Format	960x234	dot
Active Area	130.6 (H)x97.3 (V)	mm
Dot Pitch	0.136 (H)x0.416 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	156.3 (W)x119.8 (H)x14.3 (D)	mm
Weight	280	g

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4. Mechanical Drawing of TFT-LCD Module

5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No	Symbol	I/O	Description	Remark
1	$\overline{\text{HSY}}$	I/O	Horizontal Sync. Input / Output	Note 5-1
2	FRP	O	Video Polarity Alternating Signal	
3	CSY	I	Composite Sync. Signal	Note 5-1
4	V _{GH}	I	Supply Voltage for Gate Driver (Hi level)	Note 5-3
5	V _{GL}	I	Supply Voltage for Gate Driver (Low level)	Note 5-4
6	V _B	I	Video Signal (Blue)	
7	V _R	I	Video Signal (Red)	
8	V _G	I	Video Signal (Green)	
9	GND	I	Ground	
10	V _{DD}	I	Supply voltage for Controller	Note 5-5
11	V _{SH}	I	Supply voltage for source driver	Note 5-6
12	GND	I	Ground	
13	CKC	I	Control pin for select I/O signal	Note 5-1, 5-2
14	$\overline{\text{VSY}}$	I/O	Vertical Sync. Input/ Output	Note 5-1
15	PSI	O	Synchronize Pulse for Decoder	Note 5-7
16	PSC	O	Synchronize Pulse for DC-DC Converter	Note 5-8
17	VIY	I	Vertical Sync. Input Pin for reset Vertical Counter	
18	UD	I	UP/DOWN Control	Note 5-10
19	RL	I	Right/Left Shift Control	Note 5-9
20	NP	I	NTSC/PAL Input	Note 5-11

Note 5-1 : Pin 13 (CKC) can select the function for Pin 1 ($\overline{\text{HSY}}$), Pin 3 (CSY), and Pin 14 ($\overline{\text{VSY}}$).

Pin 13 (CKC)	Pin 1 ($\overline{\text{HSY}}$)	Pin 3 (CSY)	Pin 14 ($\overline{\text{VSY}}$)
Hi	$\overline{\text{HSY}}$ Output	CSY Input	$\overline{\text{VSY}}$ Output
Low	External H-Sync. Input	External Clock Input	External V-Sync. Input

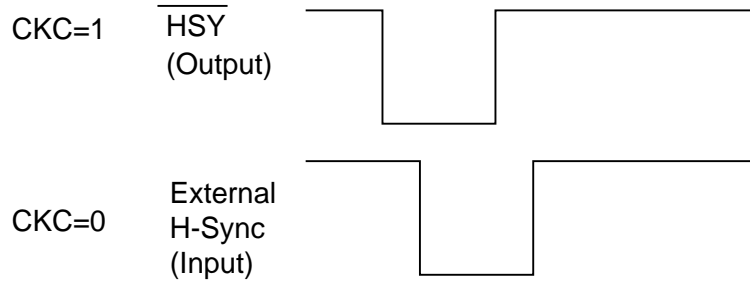
Note 5-1-1: External H-Sync and External V-Sync input pulse can be high going or low going.

Note 5-1-2: The pulse width of external H-Sync input is $4.7\mu\text{s} \pm 2\mu\text{s}$.

The pulse width of external V-Sync input is 2H~4H.

Note 5-1-3: The pulse length of external input V-Sync of NTSC system is 262H±4H and PAL system is 312H±4H.

Note 5-1-4: The timing chart of $\overline{\text{HSY}}$ and external H-Sync input:



Note 5-1-5: If there is any question about CKC=0, please contact PVI.

Note 5-2 : If CKC=1, the phase lock loop (PLL) is adopted in the LCD module.
 If CKC=0, the phase lock loop (PLL) is not adopted in the LCD module.
 If CKC=0, the external clock input frequency of Pin 3 is 18.9 MHz.

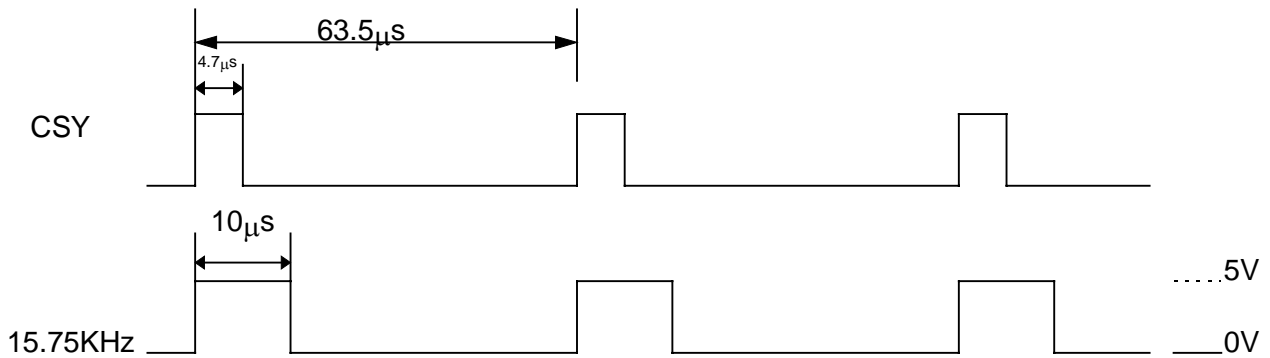
Note 5-3 : V_{GH} TYP. = +20V

Note 5-4 : V_{GL} TYP. = -5V

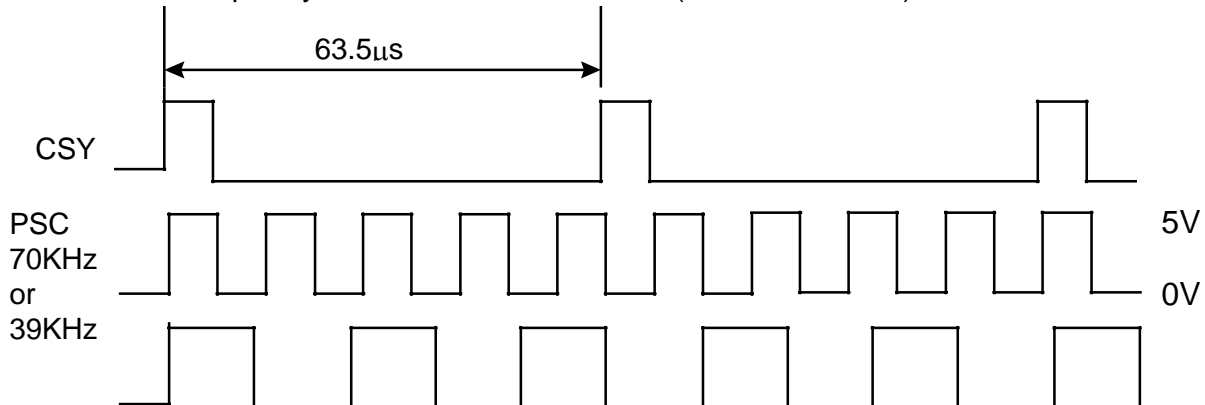
Note 5-5 : V_{DD} TYP. = +5V

Note 5-6 : V_{SH} TYP. = +14V

Note 5-7 : The frequency of PSI is 15.75KHz.



Note 5-8 : The frequency of PSC is 70KHz or 39KHz(Default is 70KHz).



Note 5-9 : Default Hi (+5V) for shift Right; Input Low (0V) for inverse (shift Left).

Note 5-10: Default Hi (+5V) for DOWN; Low (0V) for UP.

Note 5-11 : NTSC=Hi(+5V),PAL=LOW(0V)

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5-2) Backlight driving

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 5-12

Note 5-12 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

5-3) Input / Output Connector

A) LCD Module Connector

FFC Up Connector

16 Pins or 20 Pins

Pitch : 1.0 mm

B) Backlight Connector

JST BHR-03VS-1

Pin No. : 3

Pitch : 4 mm

6. Absolute Maximum Ratings:

GND = 0 V , Ta = 25

Parameter	Symbol	MIN.	MAX.	Unit	Remark	
Supply Voltage for Source Driver	V_{SH}	-0.5	+16	V		
Supply Voltage for Gate Driver	H Level	V_{GH}	-0.3	+26.5	V	
	L Level	V_{GL}	-7	20	V	
Supply voltage for controller	V_{DD}	-0.3	+6.5	V		
DC bias voltage of common electrode	V_{com}	+2	+6	V		
Analog input signals	V_B, V_R, V_G	0	12	V		
Digital input signals		-0.5	5.5	V	Note 6-1	
Digital output signals		-0.5	5.5	V	Note 6-2	
Storage Temperature		-30	+80			
Operation Temperature		-10	+60			

Note 6-1 : \overline{HSY} , \overline{CSY} , $\overline{VS_Y}$, CKC,

Note 6-2 : \overline{HSY} , $\overline{VS_Y}$, PSI, PSC

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

A) Driving for TFT-LCD Panel

GND = 0V , Ta = 25

Parameter	Symbol	MIN.	TYP	MAX.	Unit	Remark	
Supply voltage for source driver	V_{SH}	+13.5	+14	+14.5	V		
Supply voltage for gate driver	H Level	V_{GH}	+19	+20	+24	V	
	L level	V_{GL}	-5.5	-5	-4	V	
Supply voltage for controller	V_{DD}	+4.7	+5	+5.3	V		
Analog input voltage	Amplitude	V_B, V_R, V_G	+2	-	+12	V	
	DC component		+4	+6	+8	V	
Digital input voltage	H level		+2.4	-	+5	V	Note 7-1
	L level		-0.3	-	+0.8	V	
Digital output voltage	H level		+2.4	+4	+5	V	Note 7-2
	L level		0	-	+0.5	V	

Note 7-1 : \overline{HSY} , CSY , \overline{VSY} , CKC

Note 7-2 : \overline{HSY} , \overline{VSY} , PSI , PSC

B) Driving for backlight

Ta= 25

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	480	520	560	Vrms	$I_L=6mA$
Lamp current	I_L	4	6	8	mA	
Lamp frequency	P_L	20		60	KHz	Note 7-3
Kick-off voltage	V_s			1500	Vrms	

Note 7-3 : The wave form of lamp driving voltage should be as closed to a perfect SIN wave as possible.

7-2) Power Consumption

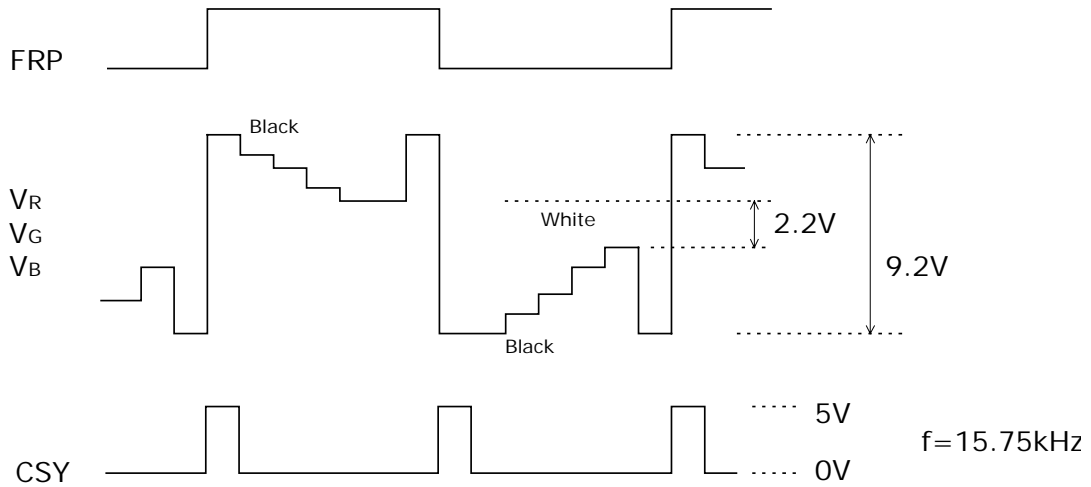
Ta= 25

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	$V_{GH} = +20V$	6	9	mA	
Supply current for Gate Driver (Low level)	I_{GL}	$V_{GL} = -5V$	5	10	mA	
Supply current for Source Driver	I_{SH}	$V_{EE} = +14V$	12	15	mA	
Supply current for controller	I_{DD}	$V_{DD} = +5V$	22	30	mA	
LCD Panel Power Consumption			0.45		W	Note 7-4
Backlight Lamp Power Consumption			3.12		W	Note 7-5

Note 7-4 : The power consumption for backlight is not included.

Note 7-5 : Backlight lamp power consumption is calculated by $I_L \times V_L$.

7-3) Input / Output signal timing chart



Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output Pulse	Width	T_{HO}	4.2	4.7	5.2	μs	
	Phase Difference	T_{HP}	0	2		μs	
	Rising Time	T_{HR}	-	-	0.5	μs	
	Falling Time	T_{HF}	-	-	0.5	μs	
Vertical Sync. Output Pulse	Width	T_{VO}	-	4H	-	μs	H=1/15.75KHZ
	Phase Difference	T_{VPO}	-	1H	-	μs	odd field
	Phase Difference	T_{VPE}	-	1.5H	-	μs	even field
	Rising Time	T_{VR}	-	-	2	μs	
	Frequency	f_{FRP}	7.67	7.87	8.07	KHz	
Polarity Alternating Signal	Delay time	T_{FD}	-	-	4	μs	
	Falling Time	T_{VF}	-	-	2	μs	

7-4) Display Time Range

A) When sync. signal of NTSC system is applied.

a) Horizontally

12.6 ~ 63.39 μ s.

b) Vertical

19 ~ 253 H

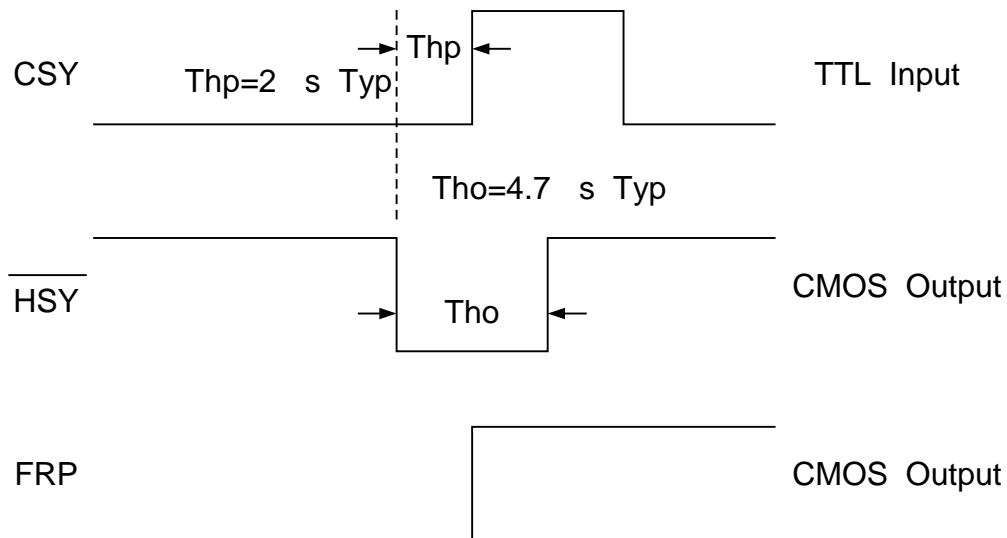
B) When sync. signal of PAL system is applied.

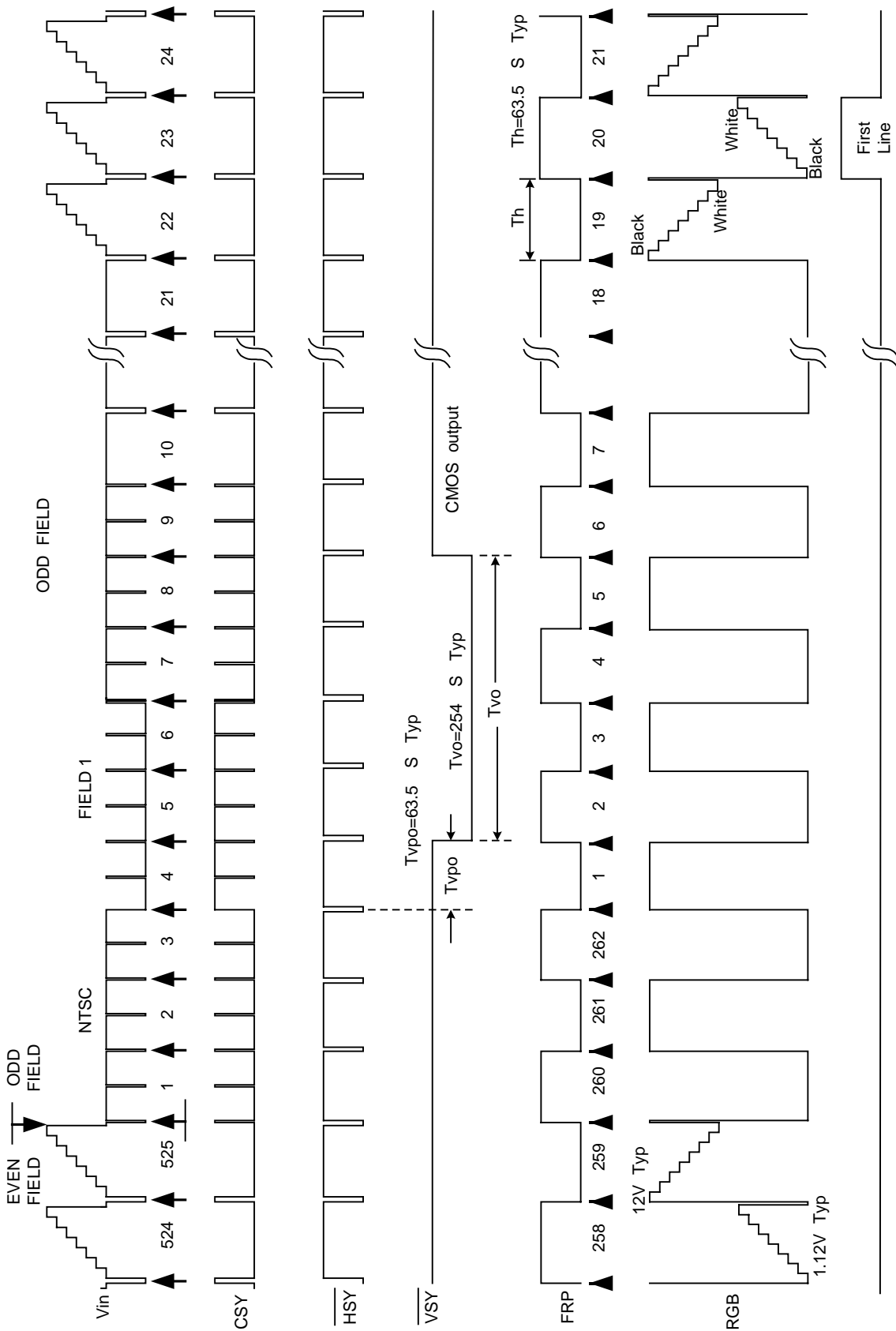
a) Horizontally

13.0 ~ 63.8 μ s .

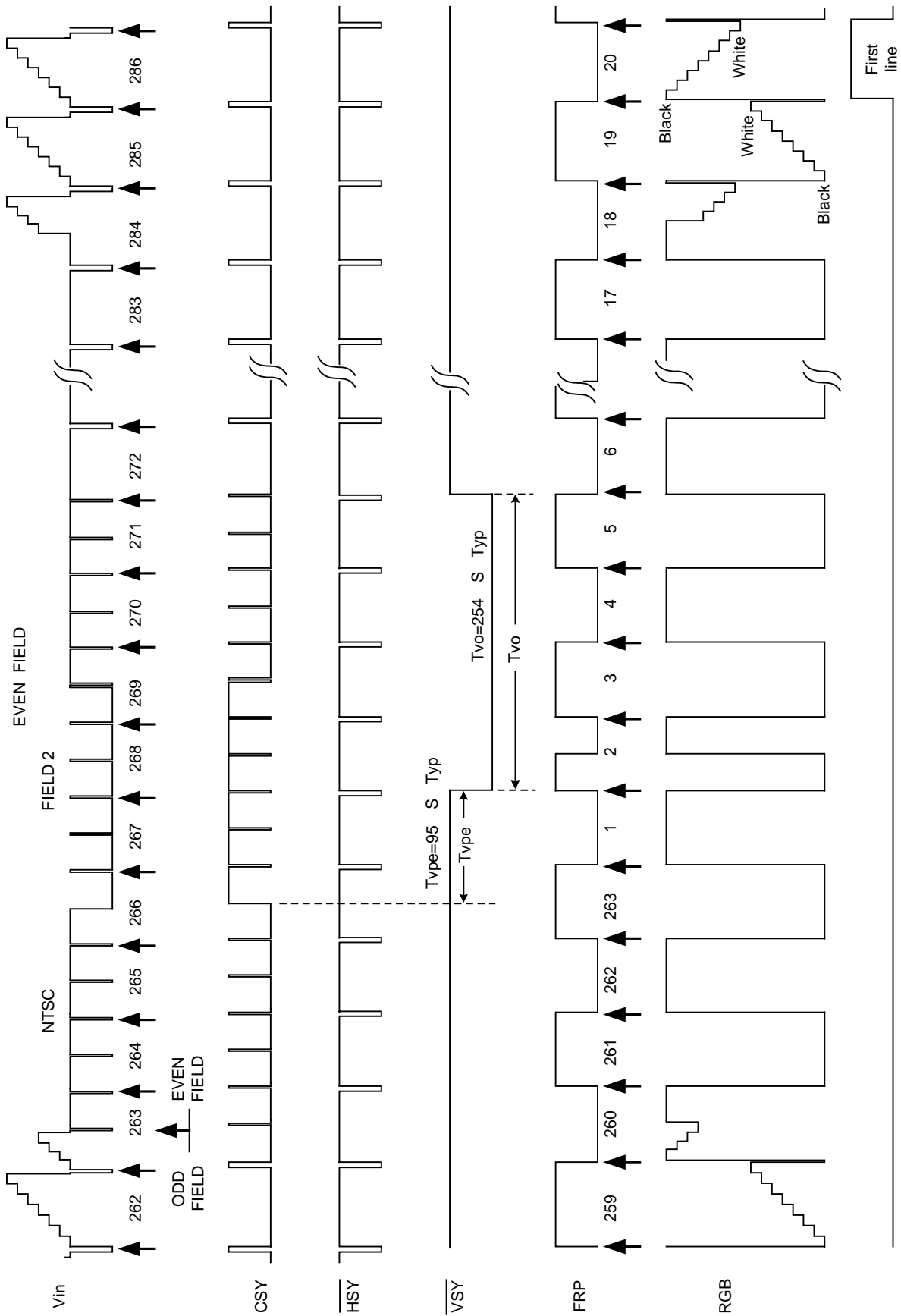
b) Vertical

26 ~ 298 H





Timing chart of I/O and RGB signal



Timing chart of I/O and RGB signal

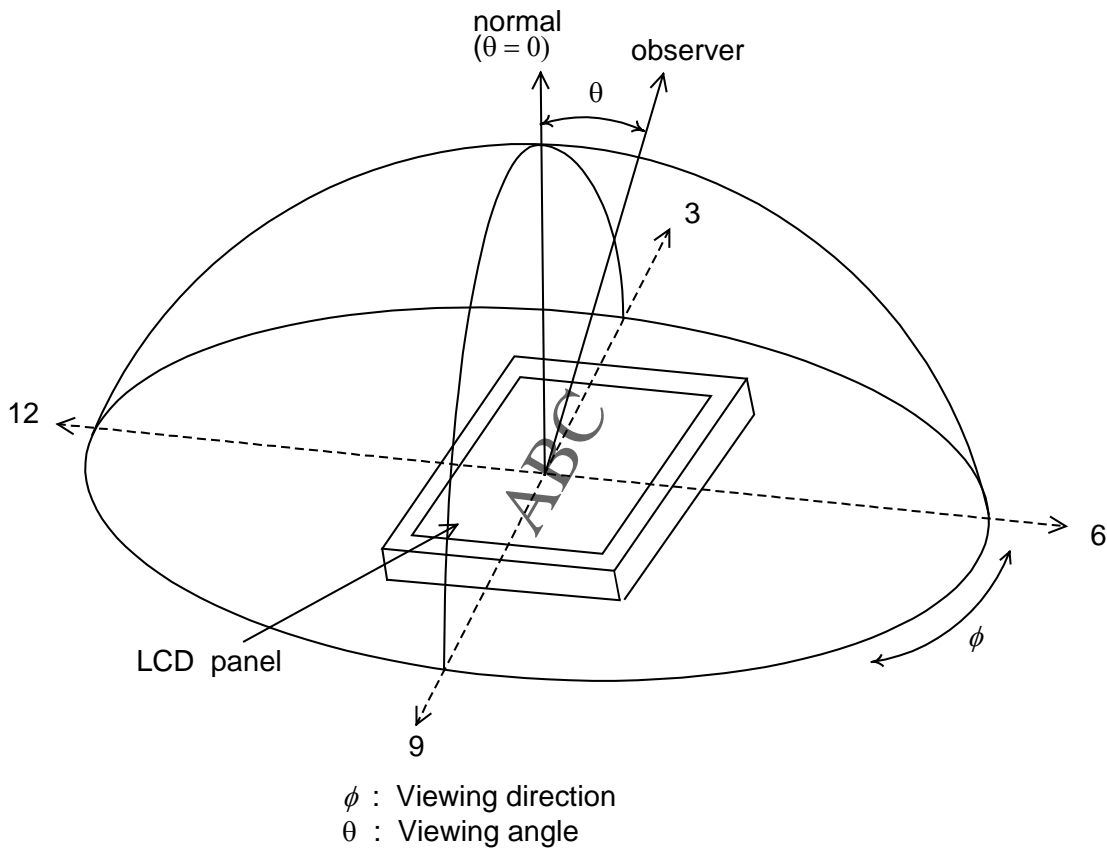
8.Optical Characteristics

8-1) Specification:

Ta = 25

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
Viewing Angle	Horizontal	CR 10	±45	±55		deg	Note 8-1	
	Vertical		(to 12 o'clock)	10	15		deg	Note 8-1
			(to 6 o'clock)	30	35		deg	Note 8-1
Contrast Ratio	CR		80	120			Note 8-2	
Response time	Rise	Tr	=0°			30	ms	Note 8-4
	Fall	Tf				50	ms	
Reflectance Ratio	R			6.0		%		
Brightness			250	300		cd/m ²	Note 8-3	
White Chromaticity	x		0.245	0.295	0.345		Note 8-3	
	y		0.307	0.357	0.407			
Lamp Life Time	+25		10,000			hr		

Note 8-1: The definitions of viewing angles



Note 8-2 : $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

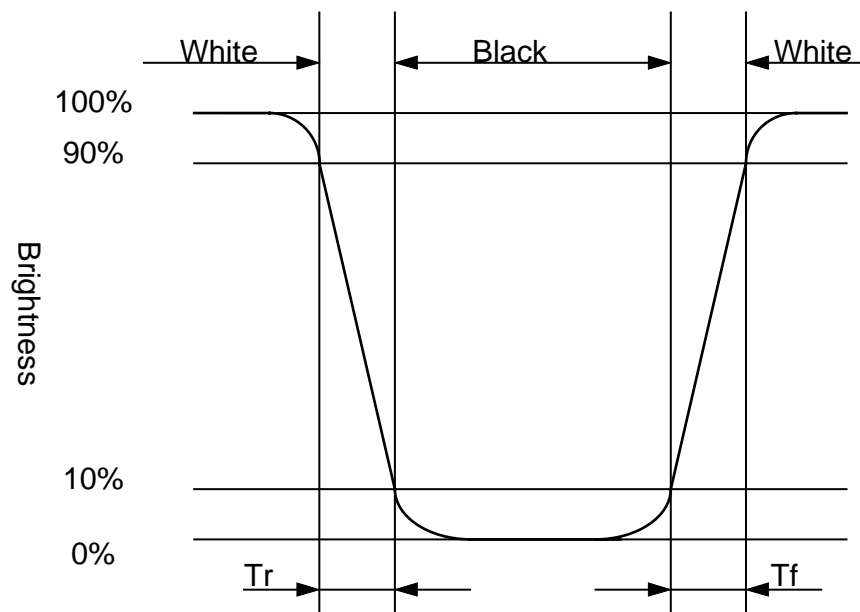
(Testing configuration see 8-2)

Contrast Ratio is measured in optimum common electrode voltage.

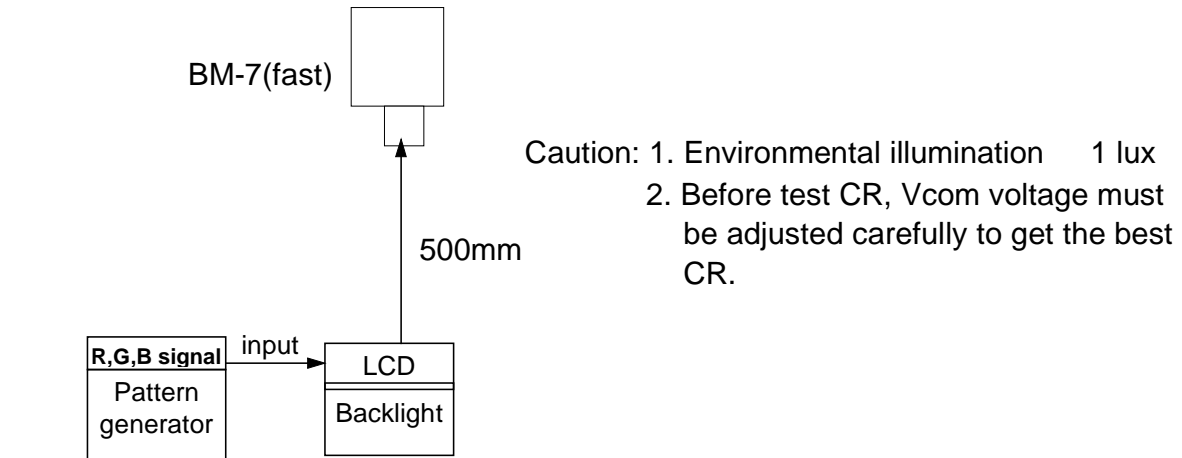
Note 8-3 : Topcon BM-7(fast) luminance meter 2°field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 6mA

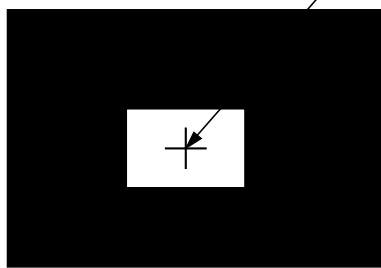
Note 8-4: The definition of response time:



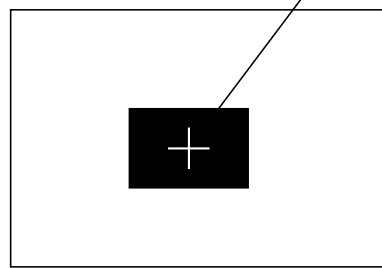
8-2) Testing configuration



- LCD Display Testing Point
- Testing Point

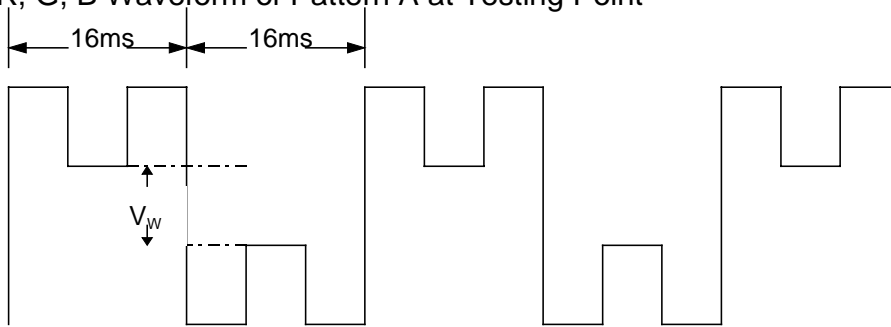


Pattern A



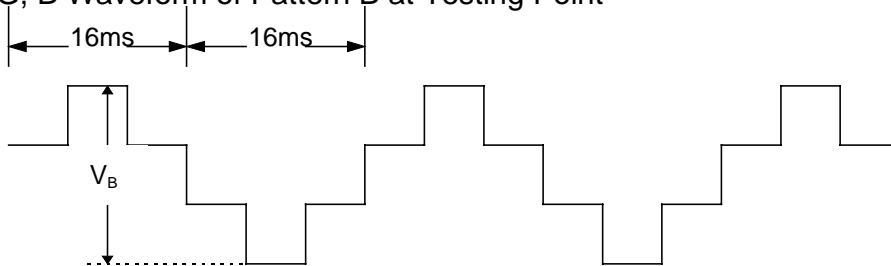
Pattern B

- R, G, B Waveform of Pattern A at Testing Point



$V_w = 2.2V \pm 0.2V$

- G, B Waveform of Pattern B at Testing Point



$V_b = 9.2V \pm 0.2V$

9. Reliability Test

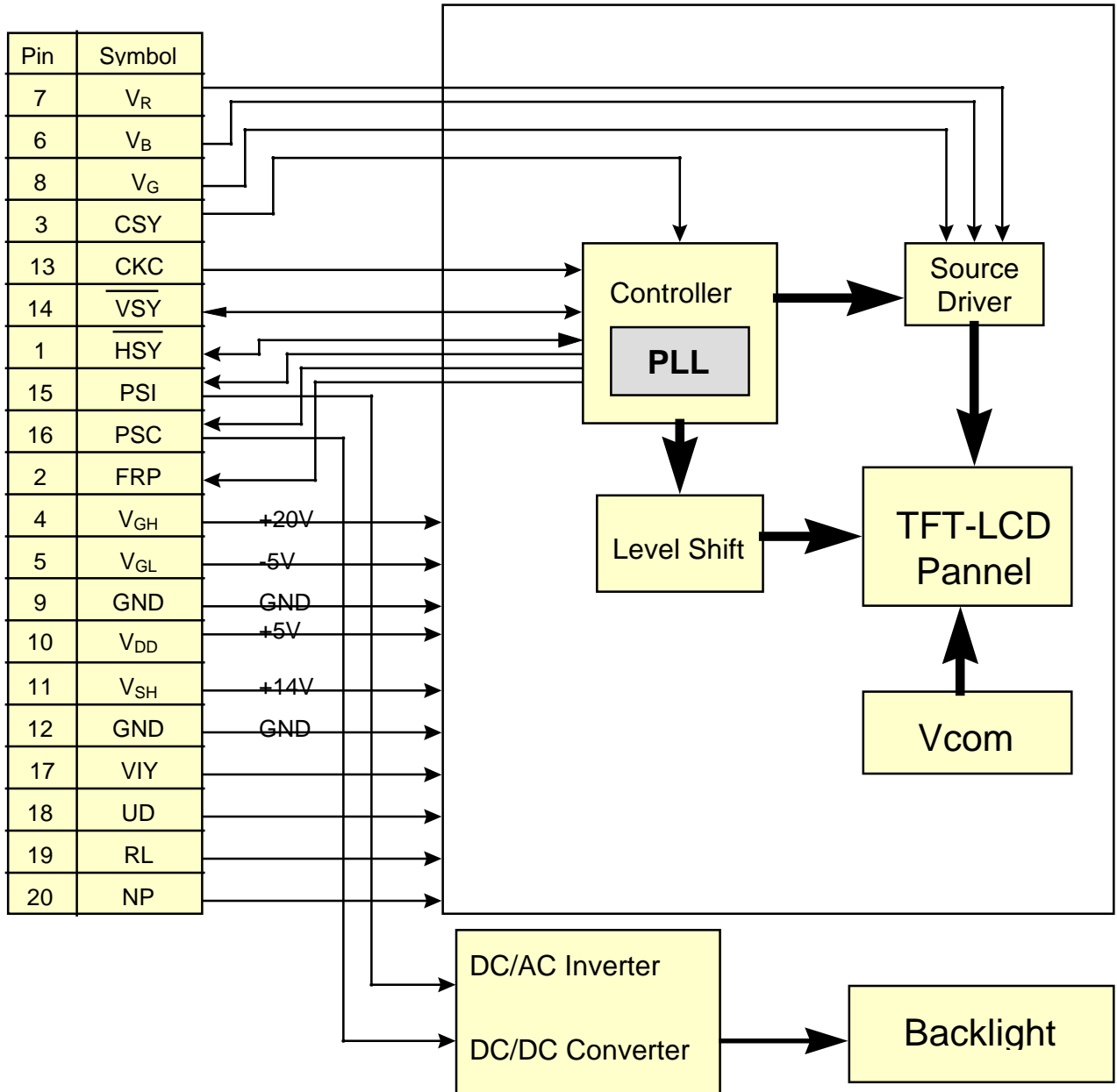
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 , 240 hrs
2	Low Temperature Storage Test	Ta = -30 , 240 hrs
3	High Temperature Operation Test	Ta = +60 , 240 hrs
4	Low Temperature Operation Test	Ta = -10 , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60 , 95%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25 +25 +70 , 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.5 mm Sweep time: 11 mins Test period: 2 hrs for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test	150pF, 330 10 times/point, 9 points/panel face

Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

10. Block Diagram



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11. Packing

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Revision History

Rev.	Issued Date	Revised Contents
1	Apr. 14,1999	NEW