Z16C32 SL1660 ONLY

IUSC™ INTEGRATED UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The IUSC (Integrated Universal Serial Controller) is a single-channel multple protocol data communications device with on-chip dual-channel DMA. The integration of a high-speed serial communications channel with a high performance DMA facilitates higher data throughput than is possible with discrete serial/DMA chip combinations. The buffer chaining capabilities combined with features like character counters, frame status block and buffer termination at the end of the frame facilitate sophisticated buffer management that can significantly reduce CPU overhead.

The IUSC is software configurable to satisfy a wide variety of serial communications applications. Offered at 20 Mbit/sec, its fast data transfer rate and multiple protocol support make it ideal for applications in todays dynamic environment of changing specifications and ever increasing speed. The many programmable features allow the user to tune the device response to meet system requirements and adapt to future changes with software instead of redesigning hardware.

The on-chip DMA channels allow high-speed data transfers for both the receiver and the transmitter. The device supports automatic status transfer through DMA and allows device initialization under DMA control. Each DMA channel can transfer data words in as little as three 50 ns clock cycles and can generate addresses compatible with 32-, 24- or 16-bit memory ranges. The DMA channels may operate in any of four modes: single buffer, pipelined, array-chained, or linked-list. The array-chained and linked-list modes reduce the problems with segmentation and re-assembly of messages in systems. To prevent the DMA from holding bus mastership too long, mastership time may be limited by counting the absolute number of clock cycles, the number of bus transactions, or both.

The CPU bus interface is designed for use with any conventional multiplexed or non-multiplexed bus. The device contains a variety of sophisticated internal functions including two baud rate generators, a digital phase-locked loop,

character counters, and 32-byte FIFOs for both the receiver and transmitter.

The IUSC handles asynchronous formats, synchronous byte-oriented formats (e.g., BISYNC), and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The IUSC can generate, and check CRC in any synchronous mode and is programmed to check data integrity in various modes. Access to the CRC value allows system software to resend or manipulate it as needed in various applications. The IUSC also has facilities for modem controls. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

Interrupts are supported by a daisy-chain hierarchy within the serial channel and between the serial channel and the DMA.

Support tools are available to aid the designer in efficiently programming the IUSC. The Technical Manual describes in detail all features presented in this Product Specification and gives programming sequence hints. The EPM™ manual (Electronic Programmers Manual) is an MS-DOS, disk-based programming initialization tool, used in conjunction with the Technical Manual. Also, there are assorted application notes and development boards to assist the designer in hardware/software development.

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).
Power connections follow conventional descriptions below:

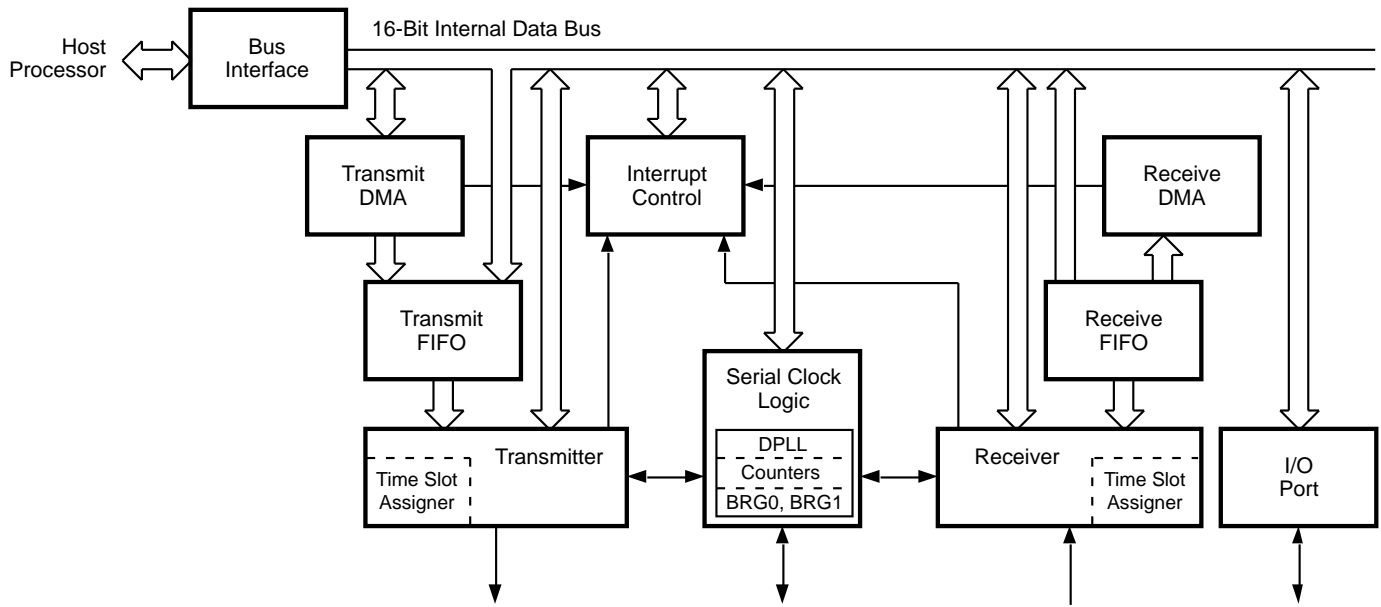| Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

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Figure 1. IUSC Block Diagram

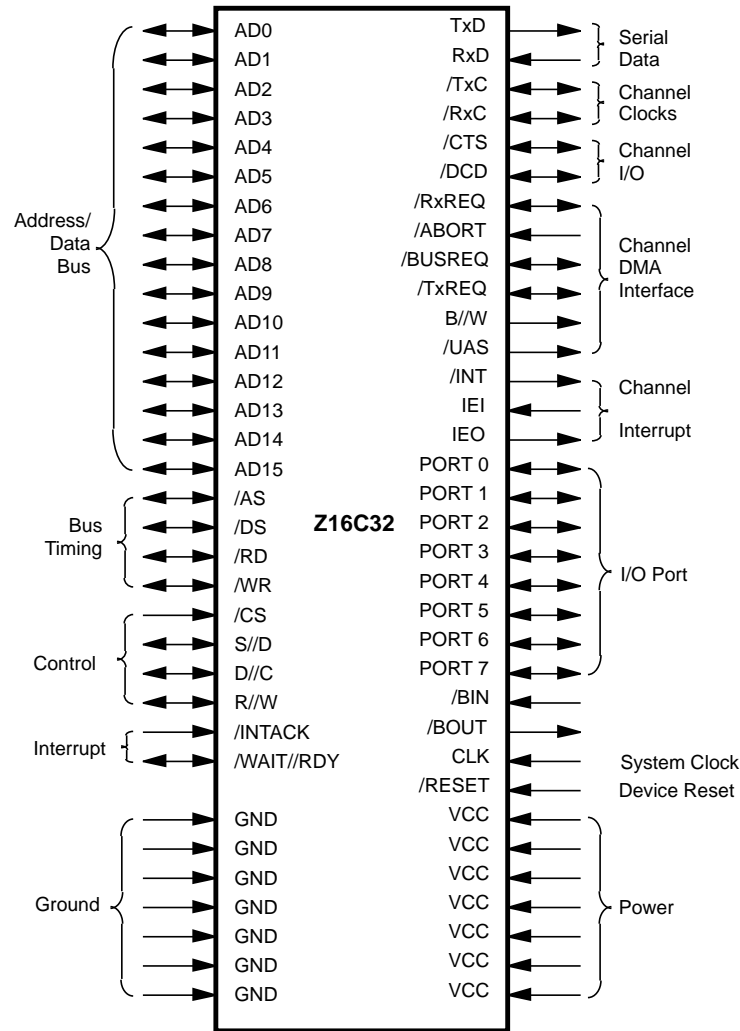**Figure 2. PLCC 68-Pin Assignments**

Figure 3. QFP 80-Pin Assignments

		Z16C32		
	AD0		TxD	Serial
	AD1		RxD	Data
	AD2		/TxC	Channel
	AD3		/RxC	Clocks
	AD4		/CTS	Channel
	AD5		/DCD	I/O
Address/	AD6		/RxREQ	
Data	AD7		/ABORT	Channel
Bus	AD8		/BUSREQ	DMA
	AD9		/TxREQ	Interface
	AD10		B//W	
	AD11		/UAS	
	AD12		/INT	Channel
	AD13		IEI	
	AD14		IEO	Interrupt
	AD15		PORT 0	
	/AS		PORT 1	
Bus	/DS		PORT 2	
Timing	/RD		PORT 3	
	/WR		PORT 4	I/O Port
	/CS		PORT 5	
Control	S//D		PORT 6	
	D//C		PORT 7	
	R//W		/BIN	
Interrupt	/INTACK		/BOUT	
	/WAIT//RDY		CLK	System Clock
			/RESET	Device Reset
	GND		VCC	
	GND		VCC	
	GND		VCC	
Ground	GND		VCC	Power
	GND		VCC	
	GND		VCC	
	GND		VCC	

Figure 4. Functional Diagram

ABSOLUTE MAXIMUM RATINGS

SYM	Description	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	+70	V
T_{STG}	Storage Temp	65°	+150°	C
T_A	Operating Ambient Temp	0	+70	C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Standard Test Load). Standard conditions are as follows:

■ $+4.5$ V $< V_{CC} <$ $+5.5$ V

■ GND = 0 V

■ T_A as specified in Ordering Information

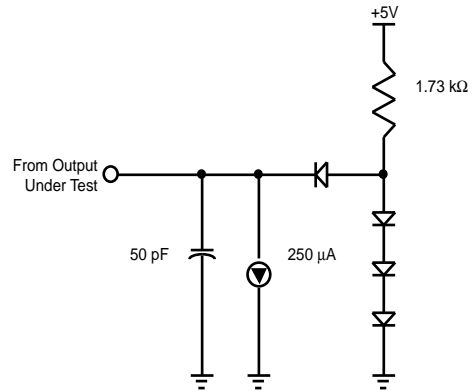**Figure 5. Standard Test Load**

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to ground.
C_{OUT}	Output Capacitance		15	pF	
$C_{I/O}$	Bidirectional Capacitance		20	pF	

Note: f = 1 MHz, over specified temperature range.

MISCELLANEOUS

Transistor Count - 100,000

TEMPERATURE RANGE

Standard: 0°C to +70°C

P R E L I M I N A R Y CP97HHS0100

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} Min	$T_A = 0°C$ to $+70°C$ Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		$V_{CC} +0.3$	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	$I_{OH}= −1.6mA$
V_{OH2}	Output High Voltage	$V_{CC}−0.8$			V	$I_{OH}= −250 \mu A$
V_{OL}	Output Low Voltage			0.4	V	$I_{OL}= +2.0 mA$
I_{IL}	Input Leakage			+10.00	μA	$0.4 < V_{IN} < +2.4V$
I_{OL}	Output Leakage			+10.00	μA	$0.4 < V_{OUT} < +2.4V$
I_{CC1}	V_{CC} Supply Current		7	50	mA	$V_{CC}=5V$ $V_{IH}=4.8V$ $V_{IL} = 0.2V$

Note: $V_{CC} = 5V \pm 10\%$ unless otherwise specified, over specified temperature range.
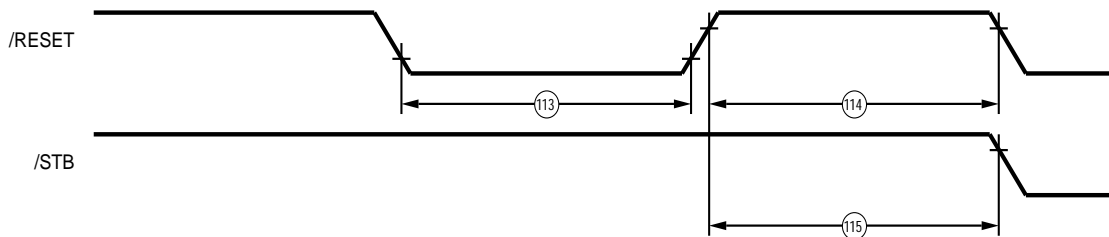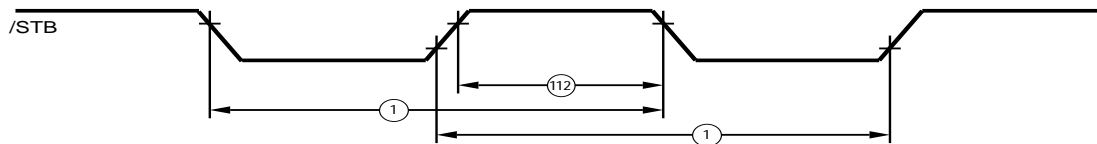
AC CHARACTERISTICS

Timing Diagrams

Figure 6. Reset Timing

Note: /STB is any of the following: /DS, /RD, /WD or Pulsed /INTACK.

Figure 7. Bus Cycle Timing
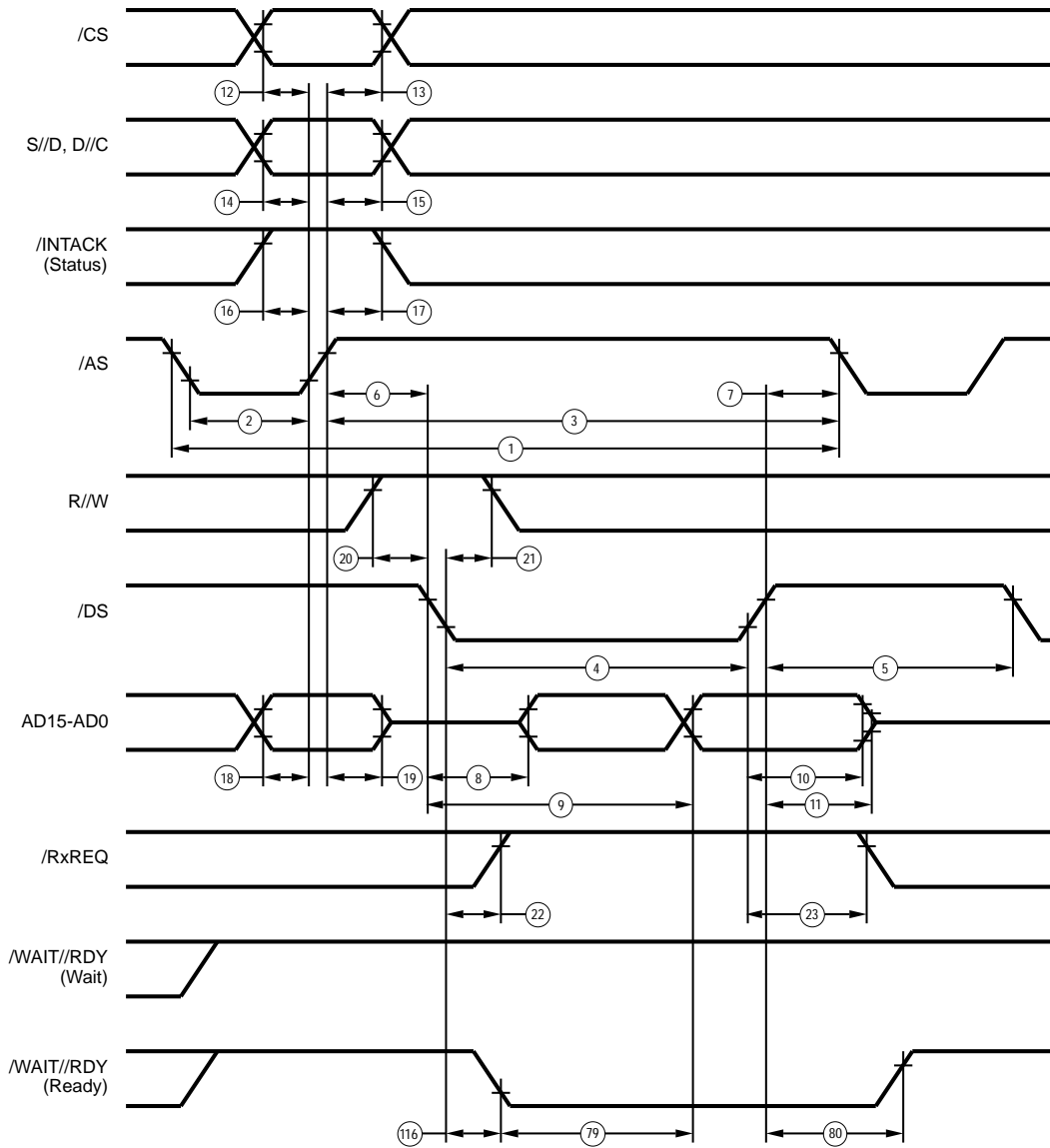
AC CHARACTERISTICS (Continued)

Figure 8. Multiplexed /DS Read Cycle

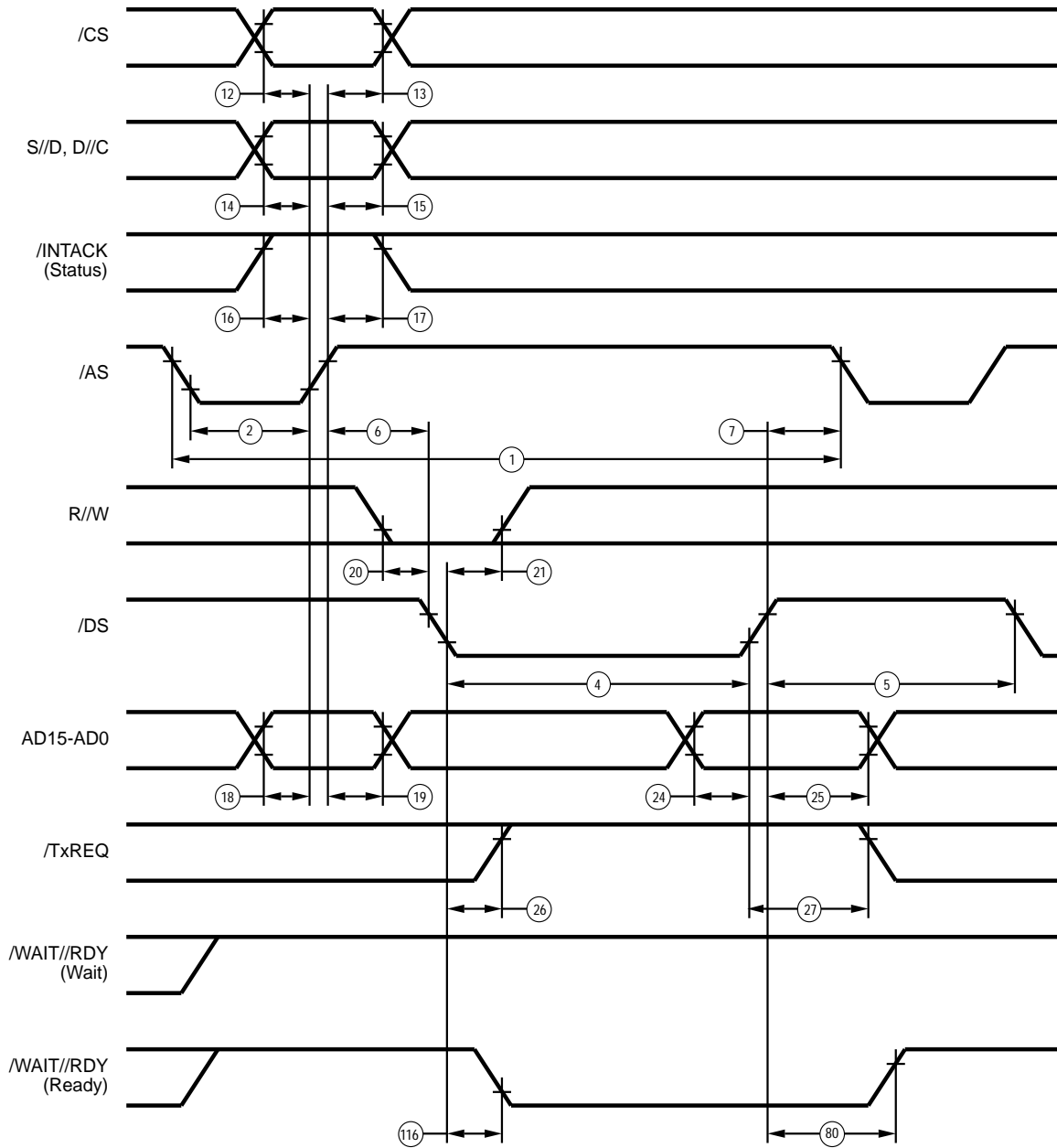**P R E L I M I N A R Y**

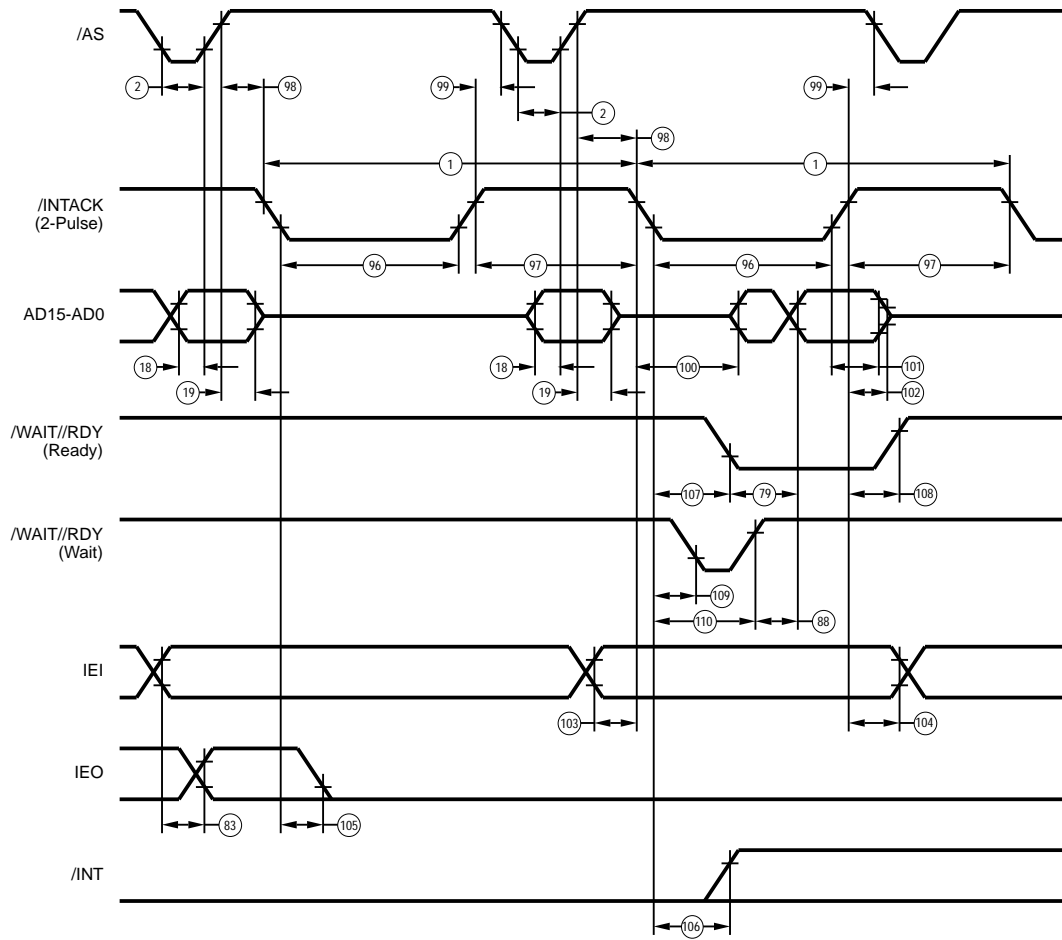**Figure 9. Multiplexed /DS Write Cycle**

AC CHARACTERISTICS (Continued)

Figure 10. Multiplexed Double-Pulse Intack Cycle
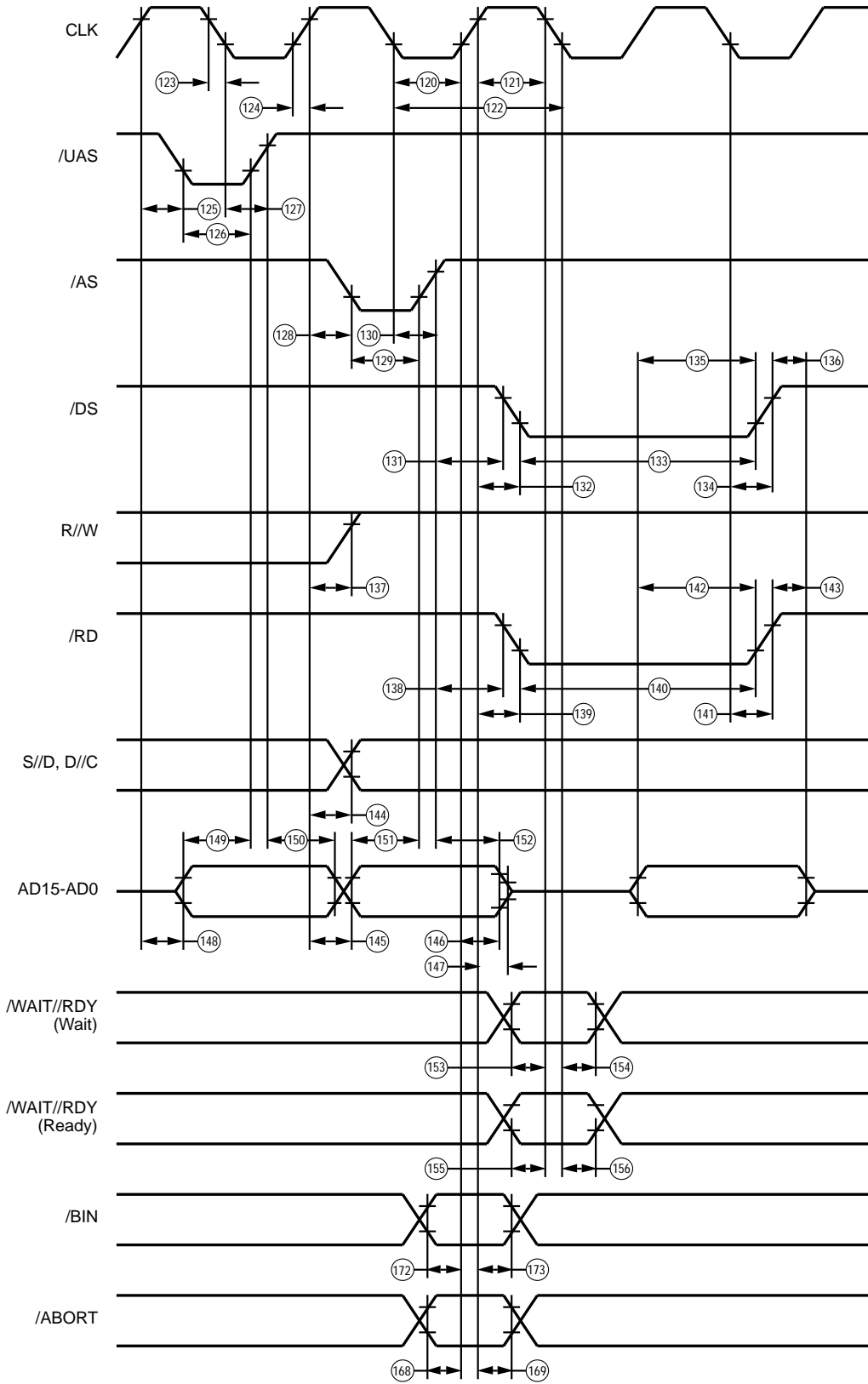
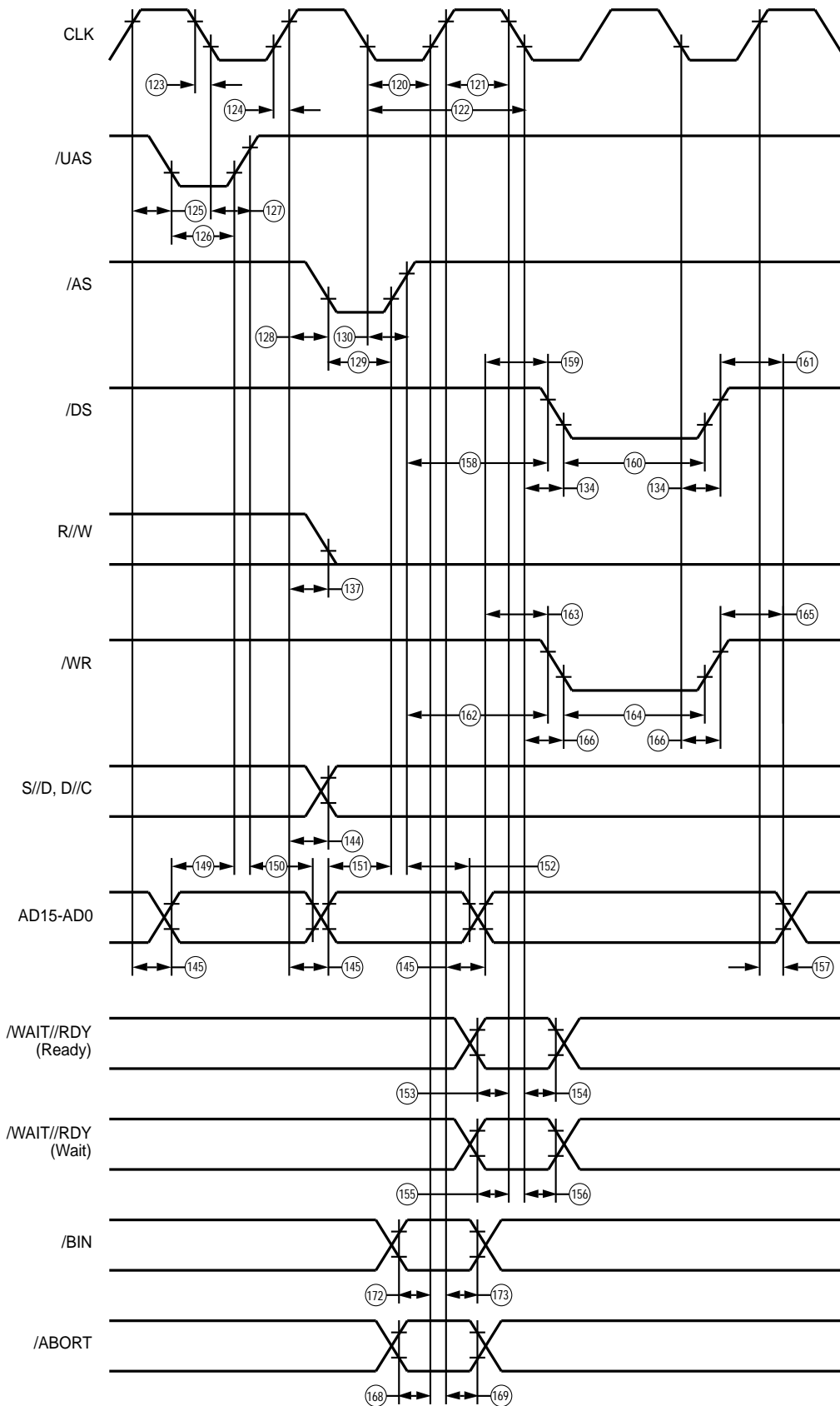**Figure 11. Memory Read**

AC CHARACTERISTICS (Continued)

Figure 12. Memory Write

P R E L I M I N A R Y

AC CHARACTERISTICS

Timing Table

No	Symbol	Parameter	V_{CC} Min	$T_A = 0°C$ to $+70°C$ Max	Units	Note(s)
1	Tcyc	Bus Cycle Time	110		ns	
2	TwASl	/AS Low Width	30		ns	
3	TwASh	/AS High Width	60		ns	
4	TwDSl	/DS Low Width	60		ns	
5	TwDSh	/DS High Width	50		ns	
6	TdAS(DS)	/AS Rise to /DS Fall Delay Time	5		ns	
7	TdDS(AS)	/DS Rise to /AS Fall Delay Time	5		ns	
8	TdDS(DRa)	/DS Fall to Data Active Delay	0		ns	
9	TdDS(DRv)	/DS Fall to Data Valid Delay		60	ns	
10	TdDS(DRn)	/DS Rise to Data Not Valid Delay	0		ns	
11	TdDS(DRz)	/DS Rise to Data Float Delay		20	ns	
12	TsCS(AS)	/CS to /AS Rise Setup Time	15		ns	
13	ThCS(AS)	/CS to /AS Rise Hold Time	5		ns	
14	TsADD(AS)	Direct Address to /AS Rise Setup Time	15		ns	1
15	ThADD(AS)	Direct Address to /AS Rise Hold Time	5		ns	1
16	TsSIA(AS)	Status /INTACK to /AS Rise Setup Time	15		ns	
17	ThSIA(AS)	Status /INTACK to /AS Rise Hold Time	5		ns	
18	TsAD(AS)	Address to /AS Rise Setup Time	15		ns	
19	ThAD(AS)	Address to /AS Rise Hold Time	5		ns	
20	TsRW(DS)	R//W to /DS Fall Setup Time	0		ns	
21	ThRW(DS)	R//W to /DS Fall Hold Time	25		ns	
22	TsDSf(RRQ)	/DS Fall to /RxREQ Inactive Delay		60	ns	4
23	TdDSr(RRQ)	/DS Rise to /RxREQ Active Delay	0		ns	
24	TsDW(DS)	Write Data to /DS Rise Setup Time	30		ns	
25	ThDW(DS)	Write Data to DS Rise Hold Time	0		ns	
26	TdDSf(TRQ)	/DS Fall to /TxREQ Inactive Delay		65	ns	5
27	TdDSr(TRQ)	/DS Rise to /TxREQ Active Delay	0		ns	
28	TwRDl	/RD Low Width	60		ns	
29	TwRDh	/RD High Width	50		ns	
30	TdAS(RD)	/AS Rise to /RD Fall Delay Time	5		ns	
31	TdRD(AS)	/RD Rise to /AS Fall Delay Time	5		ns	
32	TdRD(DRa)	/RD Fall to Data Active Delay	0		ns	
33	TdRD(DRv)	/RD Fall to Data Valid Delay		60	ns	
34	TdRD(DRn)	/RD Rise to Data Not Valid Delay	0		ns	
35	TdRD(DRz)	/RD Rise to Data Float Delay		20	ns	
36	TdRDf(RRQ)	/RD Fall to /RxREQ Inactive Delay		60	ns	4
37	TdRDr(RRQ)	/RD Rise to /RxREQ Active Delay	0		ns	
38	TwWRl	/WR Low Width	60		ns	
39	TwWRh	/WR High Width	50		ns	
40	TdAS(WR)	/AS Rise to /WR Fall Delay Time	5		ns	
41	TdWR(AS)	/WR Rise to /AS Fall Delay Time	5		ns	
42	TsDW(WR)	Write Data to /WR Rise Setup Time	30		ns	
43	ThDW(WR)	Write Data to /WR Rise Hold Time	0		ns	
44	TdWRf(TRQ)	/WR Fall to /TxREQ Inactive Delay		65	ns	5

No	Symbol	Parameter	V_CC Min	T_A = 0°C to +70°C Max	Units	Note(s)
45	TdWRr(TRQ)	/WR Rise to /TxREQ Active Delay	0		ns	
46	TsCS(DS)	/CS to /DS Fall Setup Time	0		ns	2
47	ThCS(DS)	/CS to /DS Fall Hold Time	25		ns	2
48	TsADD(DS)	Direct Address to /DS Fall Setup Time	5		ns	1,2
49	ThADD(DS)	Direct Address to /DS Fall Hold Time	25		ns	1,2
50	TsSIA(DS)	Status /INTACK to /DS Fall Setup time	5		ns	2
51	ThSIA(DS)	Status /INTACK to /DS Fall Hold Time	25		ns	2
52	TsCS(RD)	/CS to /RD Fall Setup Time	0		ns	2
53	ThCS(RD)	/CS to /RD Fall Hold Time	25		ns	2
54	TsADD(RD)	Direct Address to /RD Fall Setup Time	5		ns	1,2
55	ThADD(RD)	Direct Address to /RD Fall Hold Time	25		ns	1,2
56	TsSIA(RD)	Status /INTACK to /RD Fall Setup Time	5		ns	2
57	ThSIA(RD)	Status /INTACK to /RD Fall Hold Time	25		ns	2
58	TsCS(WR)	/CS to /WR Fall Setup Time	0		ns	2
59	ThCS(WR)	/CS to /WR Fall Hold Time	25		ns	2
60	TsADD(WR)	Direct Address to /WR Fall Setup Time	5		ns	1,2
61	ThADD(WR)	Direct Address to /WR Fall Hold Time	25		ns	1,2
62	TsSIA(WR)	Status /INTACK to /WR Fall Setup Time	5		ns	2
63	ThSIA(WR)	Status /INTACK to /WR Fall Hold Time	25		ns	2
78	TdDSf(RDY)	/DS Fall (Intack) to /RDY Fall Delay		200	ns	
79	TdRDY(DRv)	/RDY Fall to Data Valid Delay		40	ns	
80	TdDSr(RDY)	/DS Rise to /RDY Rise Delay		40	ns	
81	TsIEI(DSI)	IEI to /DS Fall (Intack) Setup Time	10		ns	
82	ThIEI(DSI)	IEI to /DS Rise (Intack) Hold Time	0		ns	
83	TdIEI(IEO)	IEI to IEO Delay		30	ns	
84	TdAS(IEO)	/AS Rise (Intack) to IEO Delay		60	ns	
85	TdDSI(INT)	/DS Fall to /INT Inactive Delay		200	ns	
86	TdDSI(Wf)	/DS Fall (Intack) to /WAIT Fall Delay		40	ns	
87	TdDSI(Wr)	/DS Fall (Intack) to /WAIT Rise Delay		200	ns	
88	TdW(DRv)	/WAIT Rise to Data Valid Delay		40	ns	
89	TdRDf(RDY)	/RD Fall (Intack) to /RDY Fall Delay		200	ns	
90	TdRDr(RDY)	/RD Rise to /RDY Rise Delay		40	ns	
91	TsIEI(RDI)	IEI to /RD Fall (Intack) Setup Time	10		ns	
92	ThIEI(RDI)	IEI to /RD Rise (Intack) Hold Time	0		ns	
93	TdRDI(INT)	/RD Fall (Intack) to /INT Inactive Delay		200	ns	
94	TdRDI(Wf)	/RD Fall (Intack) to /WAIT Fall Delay		40	ns	
95	TdRDI(Wr)	/RD Fall (Intack) to /WAIT Rise Delay		200	ns	
96	TwPIAl	Pulsed /INTACK Low Width	60		ns	
97	TwPIAh	Pulsed /INTACK High Width	50		ns	
98	TdAS(PIA)	/AS Rise to Pulsed /INTACK Fall Delay Time	5		ns	
99	TdPIA(AS)	Pulsed /INTACK Rise to /AS Fall Delay Time	5		ns	
100	TdPIA(DRa)	Pulsed /INTACK Fall to Data Active Delay	0		ns	
101	TdPIA(DRn)	Pulsed /INTACK Rise to Data Not Valid Delay	0		ns	
102	TdPIA(DRz)	Pulsed /INTACK Rise to Data Float Delay		20	ns	
103	TsIEI(PIA)	IEI to Pulsed /INTACK Fall Setup Time	10		ns	
104	ThIEI(PIA)	IEI to Pulsed /INTACK Rise Hold Time	0		ns	

No	Symbol	Parameter	V_CC Min	T_A = 0°C to +70°C Max	Units	Note(s)
105	TdPIA(IEO)	Pulsed /INTACK Fall to IEO Delay		60	ns	
106	TdPIA(INT)	Pulsed /INTACK Fall to /INT Inactive Delay		200	ns	
107	TdPIAf(RDY)	Pulsed /INTACK Fall to /RDY Fall Delay		200	ns	
108	TdPIAr(RDY)	Pulsed /INTACK Rise to /RDY Rise Delay		40	ns	
109	TdPIA(Wf)	Pulsed /INTACK Fall to /WAIT Fall Delay		40	ns	
110	TdPIA(Wr)	Pulsed /INTACK Fall to /WAIT Rise Delay		200	ns	
111	TdSIA(INT)	Status /INTACK Fall to IEO Inactive Delay		200	ns	2
112	TwSTBh	/Strobe High Width	50		ns	3
113	TwRESl	/RESET Low Width	170		ns	
114	TwRESh	/RESET High Width	60		ns	
115	TdRES(STB)	/RESET Rise to /STB Fall	60		ns	3
116	TdDSf(RDY)	/DS Fall to /RDY Fall Delay		50	ns	
117	TdWRf(RDY)	/WR Fall to /RDY Fall Delay		50	ns	
118	TdWRr(RDY)	/WR Rise to /RDY Rise Delay		40	ns	
119	TdRDf(RDY)	/RD Fall to /RDY Fall Delay		50	ns	
120	TwCLKl	CLK Low Width	25		ns	
121	TwCLKh	CLK High Width	25		ns	
122	TcCLK	CLK Cycle Time	50		ns	
123	TfCLK	CLK Fall Time		5	ns	
124	TrCLK	CLK Rise Time		5	ns	
125	TdCLKr (UAS)	CLK Rise to /UAS Fall Delay		25	ns	6
126	TwUASl	/UAS Low Width	20		ns	6,7
127	TdCLKf(UAS)	CLK Fall to /UAS Rise Delay		25	ns	6
128	TdCLKr(AS)	CLK Rise to /AS Fall Delay		25	ns	6
129	TwASl	/AS Low Width	20		ns	6,7
130	TdCLKf(AS)	CLK Fall to /AS Rise Delay		25	ns	6
131	TdAS(DSr)	/AS Rise to /DS Fall (Read) Delay	20		ns	6,8
132	TdCLKr(DS)	CLK Rise to /DS Delay		25	ns	6
133	TwDSlr	/DS (Read) Low Width	70		ns	6,9
134	TdCLKf(DS)	CLK Fall to /DS Delay		25	ns	6
135	TsDR(DS)	Read Data to /DS Rise Setup Time	30		ns	6
136	ThDR(DS)	Read Data to /DS Rise Hold Time	0		ns	6
137	TdCLK(RW)	CLK Rise to R//W Delay		25	ns	6
138	TdAS(RD)	/AS Rise to /RD Fall Delay	20		ns	6,8
139	TdCLKr(RD)	CLK Rise to /RD Delay		25	ns	6
140	TwRDl	/RD Low Width	70		ns	6,9
141	TdCLKf(RD)	CLK Fall to /RD Delay		25	ns	6
142	TsDR(RD)	Read Data to /RD Rise Setup Time	30		ns	6
143	ThDR(RD)	Read Data to /RD Rise Hold Time	0		ns	6
144	TdCLK(ADD)	CLK Rise to Direct Address Delay		25	ns	1,6
145	TdCLK(AD)	CLK Rise to Address Delay	TdCLKf(DS)	25	ns	6
146	ThAD(PC)	Address to CLK Rise Hold Time	0		ns	6
147	TdCLK(ADz)	CLK Rise to Address Float Delay		25	ns	6
148	TdCLK(ADa)	CLK Rise to Address Active Delay		25	ns	6
149	TsAD(UAS)	Address to /UAS Rise Setup Time	10		ns	6
150	ThAD(UAS)	Address to /UAS Rise Hold Time	10		ns	6

No	Symbol	Parameter	V$_{CC}$ Min	T$_A$ = 0°C to +70°C Max	Units	Note(s)
151	TsAD(AS)	Address to /AS Rise Setup Time	10		ns	6
152	ThAD(AS)	Address to /AS Rise Hold Time	10		ns	6
153	TsW(CLK)	/WAIT to CLK Fall Setup Time	10		ns	6
154	ThW(CLK)	/WAIT to CLK Fall Hold Time	15		ns	6
155	TsRDY(CLK)	/READY to CLK Fall Setup Time	10		ns	6
156	ThRDY(CLK)	/READY to CLK Fall Hold Time	15		ns	6
157	ThDW(CLK)	Write Data to CLK Rise Hold Time	0		ns	6
158	TdAS(DSw)	/AS Rise to /DS Fall (Write) Delay	40		ns	6,10
159	TsDW(DS)	Write Data to /DS Fall Setup Time	20		ns	6, 7
160	TwDSlw	/DS (Write) Low Width	45		ns	6, 11
161	ThDW(DS)	Write Data to /DS Rise Hold Time	20		ns	6, 8
162	TdAS(WR)	/AS Rise to /WR Fall Delay	40		ns	6, 10
163	TsDW(WR)	Write Data to /WR Fall Setup Time	20		ns	6, 7
164	TwWRl	/WR Low Width	45		ns	6, 11
165	ThDW(WR)	Write Data to /WR Rise Hold Time	20		ns	6, 8
166	TdCLK(WR)	CLK Fall to /WR Delay		25	ns	6
167	TdCLK(BUSz)	CLK Rise to Bus Float Delay		25	ns	6
168	TsABT(CLK)	/ABORT to CLK Rise Setup Time	20		ns	6
169	ThABT(CLK)	/ABORT to CLK Rise Hold Time	15		ns	6
170	TdCLK(BRQ)	CLK Rise to /BUSREQ Delay		25	ns	6
171	TdCLK(BUSa)	CLK Rise to Bus Active Delay		25	ns	6
172	TsBIN(CLK)	/BIN to CLK Rise Setup Time	20		ns	6
173	ThBIN(CLK)	/BIN to CLK Rise Hold Time	15		ns	6
174	TsBRQ(CLK)	/BUSREQ to CLK Rise Setup Time	25		ns	6
175	ThBRQ(CLK)	/BUSREQ to CLK Rise Hold Time	0		ns	6
176	TdBIN(BOT)	/BIN to /BOUT Delay		60	ns	

Notes:

AC Test Conditions:

V$_{CC}$ = 5V ±10% unless otherwise specified, over specified temperature range.

V$_{IH}$ = 2.0V VOH = 2.0V

V$_{IL}$ = 0.8V VOL = 0.8V

Float = +0.5V

1. Direct Address is any of S//D, D//C or AD15-AD8 used as an address bus.
2. The parameter applies only when /AS is not present.
3. Strobe is any of /DS, /RD, /WR or Pulsed /INTACK.
4. Parameter applies only if read empties the receive FIFO.
5. Parameter applies only if write fills the transmit FIFO.
6. Parameter applies only while the IUSC is bus master.
7. Parameter is clock-cycle dependent, TwCLKh + TfCLK - 5.
8. Parameter is clock-cycle dependent, TwCLKl + TrCLK - 5.
9. Parameter is clock-cycle dependent, TcCLK + TwCLKh + TfCLK - 5.
10. Parameter is clock-cycle dependent, TcCLK - 10.
11. Parameter is clock-cycle dependent, TcCLK -5.

Values shown for parameters with notes 7, 8, 9, 10, or 11 are calculated using corresponding equations with minimum values.

AC CHARACTERISTICS
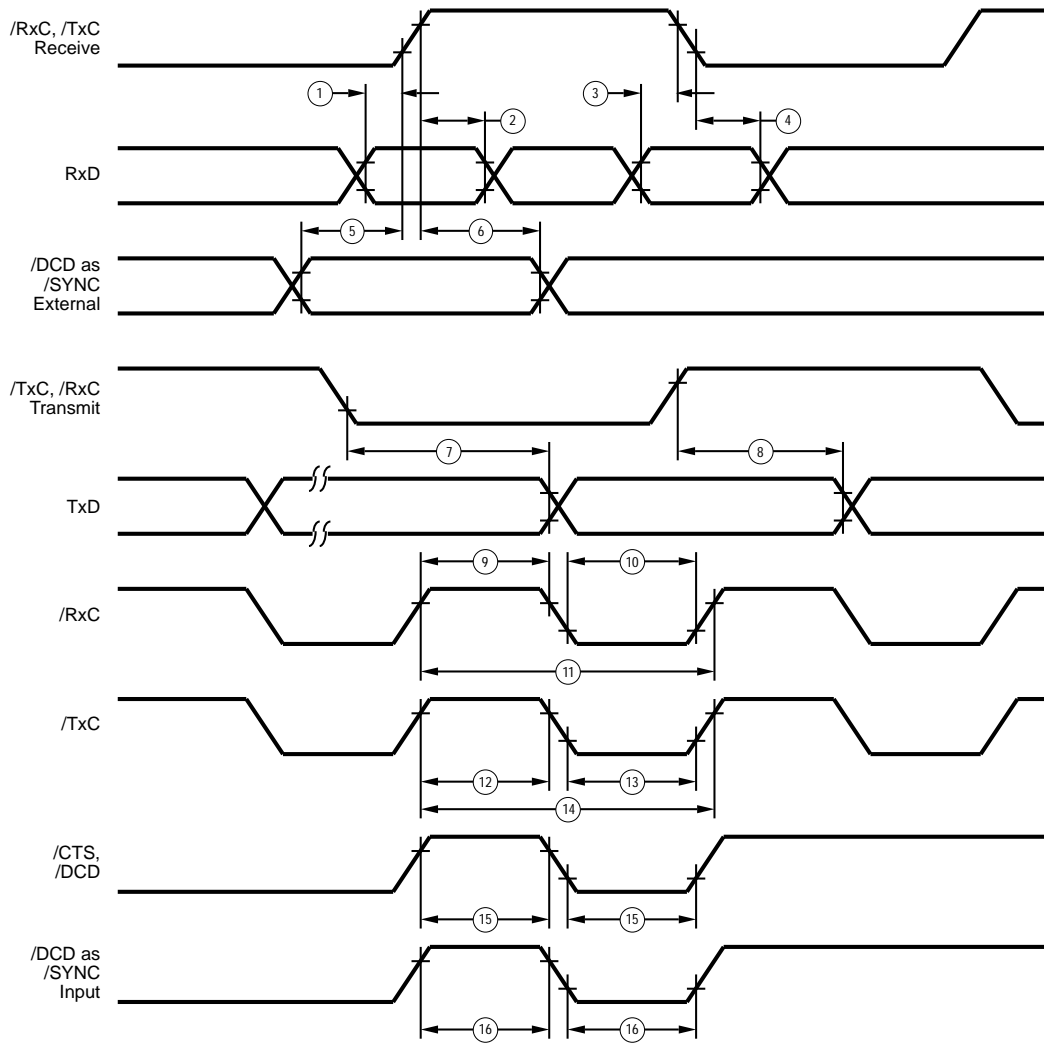General Timing Diagram

Figure 13. General Timing

AC CHARACTERISTICS
General Timing Table

No	Symbol	Parameter	$T_A = 0°C$ to $+70°C$			
			Min	Max	Units	Note(s)
1	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (x1 Mode)	0		ns	1
2	ThRxD(RxCr)	RxD to /RxC Rise Hold Time (x1 Mode)	20		ns	1
3	TsRxd(RxCf)	RxD to /RxC Fall Setup Time (x1 Mode)	0		ns	1,3
4	ThRxD(RxCf)	RxD to /RxC Fall Hold Time (x1 Mode)	20		ns	1,3
5	TsSy(RxC)	/DCD as /SYNC to /RxC Rise Setup Time	0		ns	1
6	ThSy(RxC)	/DCD as /SYNC to /RxC Rise Hold Time (x1 Mode)	20		ns	1
7	TdTxCf(TxD)	/TxC Fall to TxD Delay		35	ns	2
8	TdTxCr(TxD)	/TxC Rise to TxD Delay		35	ns	2,3
9	TwRxCh	/RxC High Width	20		ns	
10	TwRxCl	/RxC Low Width	20		ns	
11	TcRxC	/RxC Cycle Time	50		ns	
12	TwTxCh	/TxC High Width	20		ns	
13	TwTxCl	/TxC Low Width	20		ns	
14	TcTxC	/TxC Cycle Time	50		ns	
15	TwExT	/DCD or /CTS Pulse Width	35		ns	
16	TWSY	/DCD as /SYNC Input Pulse Width	35		ns	

AC CHARACTERISTICS

System Timing Table

No	Symbol	Parameter	$T_A = 0°C$ to $+70°C$			
			Min	Max	Units	Note
1	TdRxC(REQ)	/RxC Rise to /RxREQ Valid Delay		50	ns	2
2	TdRxC(RxC)	/TxC Rise to /RxC as Receiver Output Valid Delay		50	ns	2
3	TdRxC(INT)	/RxC Rise to /INT Valid Delay		50	ns	2
4	TdTxC(REQ)	/TxC Fall to /TxREQ Valid Delay		50	ns	2
5	TdTxC(TxC)	/RxC Fall to /TxC as transmitter Output Valid Delay		50	ns	
6	TdTxC(INT)	/TxC Fall to /INT Valid Delay		50	ns	2
7	TdEXT(INT)	/CTS, /DCD, /TxREQ, /RxREQ transition				
		to /INT Valid Delay		50	ns	

Notes:
1. /RxC is /RxC or /TxC, whichever is supplying the receive clock.
2. /TxC is /TxC or /RxC, whichever is supplying the transmit clock.
3. Parameter applies only to FM encoding/decoding

IUSC TECHNICAL MANUAL CORRECTION

There is a typographical error in the Q2/91 printing of the IUSC Technical Manual. The transmit and receive interrupt pending (IP) and interrupt under service (IUS) bits are shown in reverse order. The correct register bit locations are shown below. The correct bit functions are also shown in the IUSC Product Specification.

Register	Corrected Register Bits			
CDIR	RxIUS=D9	TxIUS-D8	RxIP=D1	TxIP=D0
DICR			RxIE=D1	TxIE=D0
SDIR	RxIUS=D9	TxIUS=D8	RxIP=D1	TxIE=D0

AC CHARACTERISTICS
System Timing Diagram

Figure 14. Z16C32 System Timing

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

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