Z86L7103ZEM

ICEBOX™ FAMILY
IN-CIRCUIT EMULATOR-L71

FEATURES

- Supported Products

Packages	Emulation	OTP Programming
20-Pin PDIP	Z86L71/L78[1]	N/A
28-Pin PDIP	Z86L79/L80[2] Z86L88/L81/L86[3]	N/A N/A
40-Pin PDIP	Z86L72/E72/L73/E73/L87/L89[4]	Z86E72/E73[6]
44-Pin PLCC	Z86L72/E72/L73/E73/L87/L89[5]	Z86E72/E73[6]
44-Pin QFP	N/A	Z86E72/E73[6]

Notes:
1. Using the supplied 20-pin PDIP L71 Emulation Pod/Cable.
2. Using the supplied 28-pin PDIP L79 Emulation Pod/Cable.
3. Using the supplied 28-pin PDIP L88 Emulation Pod/Cable.
4. Using the supplied 40-pin PDIP L72 Emulation Pod/Cable.
5. Using the supplied 44-pin PLCC L72 Emulation Pod/Cable.
6. Using the supplied OTP Programming Adapter.

- In-Circuit Program Debug Emulation
- Real-Time Emulation
- Z8 GUI Emulator Software
- Window-Based User Interface
- On-Line Help
- One-Time Programmable (OTP) Support
- Selectable Baud Rates – 9600 to 57.6 KB
- Bisync Error-Correcting Communications Protocol

GENERAL DESCRIPTION

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The Z86L71 Emulator is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z86L7X and Z86L8X family of infrared remote controllers. The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

The Z8L71 Emulator provides users with a hardware platform to develop and debug software in a real-time environment. In contrast, software simulators provide significantly slower operation, making them less practical for code development.

The Z86L71 Emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature:	20°C ±10°C
Supply Voltage:	+4.75 VDC to 5.25VDC
	(+5.0 VDC typical)
Minimum Emulation Speed:	1 MHz internal SCLK
Maximum Emulation Speed:	8 MHz internal SCLK
	16 MHz external Crystal

Note: A software workaround is required for emulation above 12MHz; Emulator is shipped with 8MHz crystal)

Maximum Emulation Memory:	32K
Maximum Hardware Breakpoints:	32K
Emulation Processor:	Z86C5020GSE
Programming Sockets:	40-pin DIP ZIF socket

Operating Humidity:

10-90% RH (non-condensing)

Power Requirements

+5.0 VDC @ 1.5A Minimum

Dimensions

Width:	6.25 in. (15.8 cm)
Length:	9.50 in. (24.1 cm)
Height:	2.50 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

- IBM PC (or 100-percent compatible) 386-Based Machine
- 33 MHz
- 4 MB RAM
- VGA Video Adapter
- Hard Disk Drive (1 MB free space)
- 3.5-inch, High-Density (HD) Floppy Disk Drive
- RS-232C COM Port
- Mouse or Pointing Device
- Microsoft Windows 3.1
- The following changes to the Minimum Requirements are recommended for increased performance:
  - 486- or Pentium-Based Machine
  - 66 MHz (or faster)
  - 8 MB of RAM (or more)
  - SVGA Video Adapter
  - Color Monitor
  - Printer

KIT CONTENTS

- Z86L71 Emulator

- Cables/Pods
  - Power Cable with Banana Plugs
  - DB25 RS-232C Cable
  - 20-Pin Dip L71 Emulation Pod/Cable
  - 28-Pin Dip L79 Emulation Pod/Cable
  - 28-Pin Dip L88 Emulation Pod
  - 40-Pin Dip L72 Emulation Pod/Cable
  - 44-Pin Dip L72 Emulation Pod

- OTP Programming Adapter
  One Z86E72/E73 Programming Adapter

- Host Software
  - Z8 GUI Emulator Software
  - ZASM Cross-Assemble/MOBJ Object File Utilities

Note: Cross-Assembler and C Compiler are sold separately from Production Languages Corp. and other third -party development tool companies:

Production Languages Corp. (817) 599-8363
E-mail: info @plcorp.com
Internet: www.plcorp.com

Refer to the Zilog Internet site (www.zilog.com) for more information on third-party support.

- Documentation
  - Emulator User's Manual
  - Emulator Product Information Sheet
  - Z8 Cross-Assembler User's Guide
  - Universal Object File (MOBJ) User's Guide
  - Z86L7100ZAC User's Guide
  - Registration Card

Internet: www.zilog.com

LIMITATIONS

1. Switching ICEBOX™ emulators without quitting the GUI is not supported and may cause unexpected results.

2. The maximum loadable symbols is 32,768, provided there is enough system resource (memory).

3. Although GUI 3.00 and later support baud rates up to 57.6K baud, the actual maximum usable rate may be less due to limitations of the user's hardware or system software setup. The maximum usable rate is determined by the user's tolerance of the frequency of communication errors.

4. Do not put a breakpoint at addresses after STOP instruction. This will cause the program counter to continue at that location after a Stop-Mode Recovery.

5. Single-stepping into the Halt instruction will cause an ICEBOX "Fatal Error" message to be displayed on the screen. The ICE chip must be reset, either by /Reset pin on the target board or by resetting the whole ICEBOX by pressing the emulator MASTER RESET button at the back of the emulator.

6. Clicking on the HALT button does not always halt the ICEBOX execution. If the application goes into Stop Mode or Halt Mode, the only way to halt the emulator execution is by doing a Stop-Mode Recovery (as defined by the user program). You may also reset the application using the emulator MASTER RESET button; however, this will reset the whole ICEBOX.

7. RC oscillator emulation is not supported.

8. Since the emulator uses the Z86C50 ICE chip, Port 1 cannot be configured to Low EMI mode. Bit 4 in PCON registers must be set to logic "1".

   Note: This is not a problem with the actual emulated device.

9. When the software enters a STOP mode and the HALT control button in the GUI software is pressed, any SMR source on the application board is activated. The emulator will then jump back to address 000C, which is normal. But when continuing the program with a GO command from 000C, a POR reset is performed, resetting all control registers.

   A workaround is to do a JUMP 000D and execute with GO. This will not issue a POR reset.

10. Port 1 can only be written. The data in Port 1 cannot be read from Port1 directly, but it can be read from Register %03 in Expanded Register Group D.

11. The L71 ICEBOX uses the Z86C50 ICE Chip; therefore, emulation at more than 12 MHz requires that the Expanded Register file timing of the ICE Chip be slowed to SCLK x 2. This is accomplished by loading value %01 to ICECON Register (Bank F, Register A) of the ICE Chip.

    Example:

```
PUSH    RP
LD      RP,#%0F
LD      %A,#%01
POP     RP
```

PRECAUTIONS

ALL Devices

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point.

2. For some 386 PCs, a baud rate of 19.2K or less is necessary because the Windows' communication driver does not guarantee "reliable" operation above 9600 baud. On some slower 386 machines, selecting a high baud rate might crash the Windows' environment or result in excessive communication errors.

3. When simultaneously running two different GUI versions on two different Communication Ports, the former executed version is used for both emulators. This is a Windows Operating System bug.

4. The emulator cannot be operated while performing ESD/EMI testing on the target board.

5. Executing GUI. The GUI will occasionally continue to indicate "Executing" after a Halt instruction. Pushing the GO button will then result in Executing. (Executing showing at the top of the screen.)

6. Ensure that the target cable is correctly aligned (pin-1 to pin-1) before inserting into the target system. Incorrect alignment may damage the emulator and/or the target system.

7. All Z8 control registers are Write-Only unless stated otherwise.

8. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self-test will always leave the same values in the general-purpose registers, while the real device will have a random or undefined value.

9. Power Supply ramp-up/rise time must be such that when the minimum power-on reset time (Tpor) expires, the V_{CC} must be in the supported specified operating range of the device.

10. If Program Counter jumps to an unknown address:

    a. Stack is not set to internal. Register %F8 (P01M Register) bit D2 not set to state “1”.

    b. Stack Pointer Register %FE(SPH) and Register %FF(SPL) are not initialized. For internal Stack, SPH does not have to be initialized since it is not used. The SPH and SPL are reset to 00H after any reset or Stop-Mode Recovery.

    c. Any instruction other than “DI” was used to disable interrupts.

    d. The Stack overflowed into the general-purpose register locations.

    e. Extra “POP”, “PUSH”. “IRET”, or “RET” was encountered.

    f. When making changes to the IMR register, the GLOBAL interrupts must be disabled first using DI instruction.

11. If the Program keeps resetting:

    a. Program Counter rolled over from value “FFFF” to “0000” and proceeded back to beginning of program.

    b. Watch-Dog Timer (WDT) was not refreshed from devices with WDT feature.

12. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications. The Z86C50 ICE chip typical WDT time period is configured using bits 0 and 1 of the WDTMR register located in Bank F of the Expanded Register Group at address 0FH.

Typical Z86C50 ICE Chip WDT Time-Out Period		
Internal RC (ms) Time-Out		
Bit 1	Bit 0	Z86C50
0	0	4
0	1	9
1	0	18
1	1	75

Note: Typical Z86C50 T_{POR} = 6.0 ms.

13. Do not start the emulator with OTP device in the programming socket, as the emulator may not start up correctly.

14. A shorted PLCC or DIP OTP can crash the emulator when inserted into the OTP programming socket. If a PLCC part is inserted in such a way as to cause a temporary short, then functionality is lost. An attempt to perform BLANK CHECK on such a part will cause the “hourglass” to appear continuously. The Windows application must be reset and restarted.

15. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

16. Do not press the emulator MASTER RESET when the ICEBOX is in the OTP dialog for programming. If MASTER RESET is pressed while the GUI is doing OTP programming, close the OTP dialog box and reopen it to reload the information back to the hardware.

    Note: The ICEBOX is really sitting idle, although the Command Status shows “Processing” after the GUI reestablishes the communication link when “Retry” was selected in the “Out of Synchronization with the emulator” dialog box.

17. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization should be disabled prior to invoking the VERIFY operation.

18. The bits of non-implemented features (of devices having a PCON register) must be set to state “1” on the emulator.

19. When interrupts are enabled, breakpointing after a Halt instruction, the emulator will break at the first instruction in the interrupt service routine that is serviced when an interrupt occurs.

20. Port 0, Port 1, and Port 2 have auto latches permanently enabled.

21. SCLK/16 Mode of SMR register is not supported.

22. Programming the ROM protect bit on all Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus, ROM protect does not support the use of a ROM lookup table. The value must be loaded as “immediate values”.

The Port 3 Mode Register (R247 P3m) bit D1 must be set as follows:

0 = Digital Mode
1 = Analog Mode

23. For SMR2 Recovery Source to work correctly, Port 2 must be configured to input. (P2M Register must be written.)

24. There is no software option for the Port 3 pull-up resistor for all OTP devices when using the L71 ICEBOX.

Z86L70/L71/L75

1. The register %F8(P01M register) bit D2 must be set to state “1.

2. WDT Register(F)%0F can only be written in the first 64 internal system clocks from the start of program execution.

3. The PCON register reserved bits for the L71 emulator must be set to “1”.

4. The L71 emulator does not correctly emulate L71 ports P34 and P35 when open-drain. The C50 ICE Chip does not exhibit the same behavior when the P3M Control Register is programmed.

Z86L72/L73/E72/E73

1. WDT Register(F)%0F can only be written in the first 64 internal system clocks from the start of program execution.

2. Register(F)%00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1.

3. The device has 256 bytes of internal register and 512 bytes of internal data memory (%FE00 to %FFFF). The emulator has 256 bytes of internal register and 512 bytes of internal data memory (%FE00 to %FFFF). The E72/E73 OTP has 768 bytes of internal DATA Memory (%FD00 -%FFFF).

Z86L79/L80/L8/L81/L86

1. The register %F8(P01M register) bit D2 must be set to state “1”.

2. WDT Register(F)%0F can only be written in the first 64 internal system clocks from the start of program execution.

Z86L71

1. When the emulator is set up to allow the analog comparators to output their value on P34, and one writes to Port 0, P34 stops following the comparator input.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com