

Z90349/348

DIGITAL TELEVISION CONTROLLER IN-CIRCUIT EMULATOR (ICE) DEVICE

FEATURES

- | | | | | |
|--|---|---|--|--|
| <ul style="list-style-type: none"> ■ Part Number Z90349 Z90348 | <ul style="list-style-type: none"> ROM (Word) 0 0 | <ul style="list-style-type: none"> RAM (Word) 1K 1K | <ul style="list-style-type: none"> Speed (MHz) 12 12 | <ul style="list-style-type: none"> ■ Direct Closed Caption Decoding ■ TV Tuner Serial Interface ■ Customized Character Set ■ Character Control Mode ■ Directly Controlled Receiver Functions ■ V-Chip Decode |
|--|---|---|--|--|
- 144-Pin Grid Array (PGA) Package (Z90349)
100-Pin Quad Flat Pack (QFP) Package (Z90348)
 - 4.5- to 5.5-Volt Operating Range
 - Z89C00 RISC Processor Core
 - 0°C to +70°C Temperature Range

GENERAL DESCRIPTION

The Z90349 and Z90348 are ROMless versions of the Z89300 family of Zilog's Digital Television Controllers designed for use in emulators and development boards to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The powerful Z89C00 RISC processor core allows users to control on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes, including underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency, are made possible through a fully customized 512 character set.

Serial interfacing with the television tuner is provided through the tuner serial port. Digital channel tuning adjustments may be accessed through the industry-standard I²C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Special circuitry can be activated to improve the visibility of text by adding a right-sided shadow effect to the characters.

Receiver functions such as color and volume can be directly controlled by six 8-bit pulse width modulated ports.

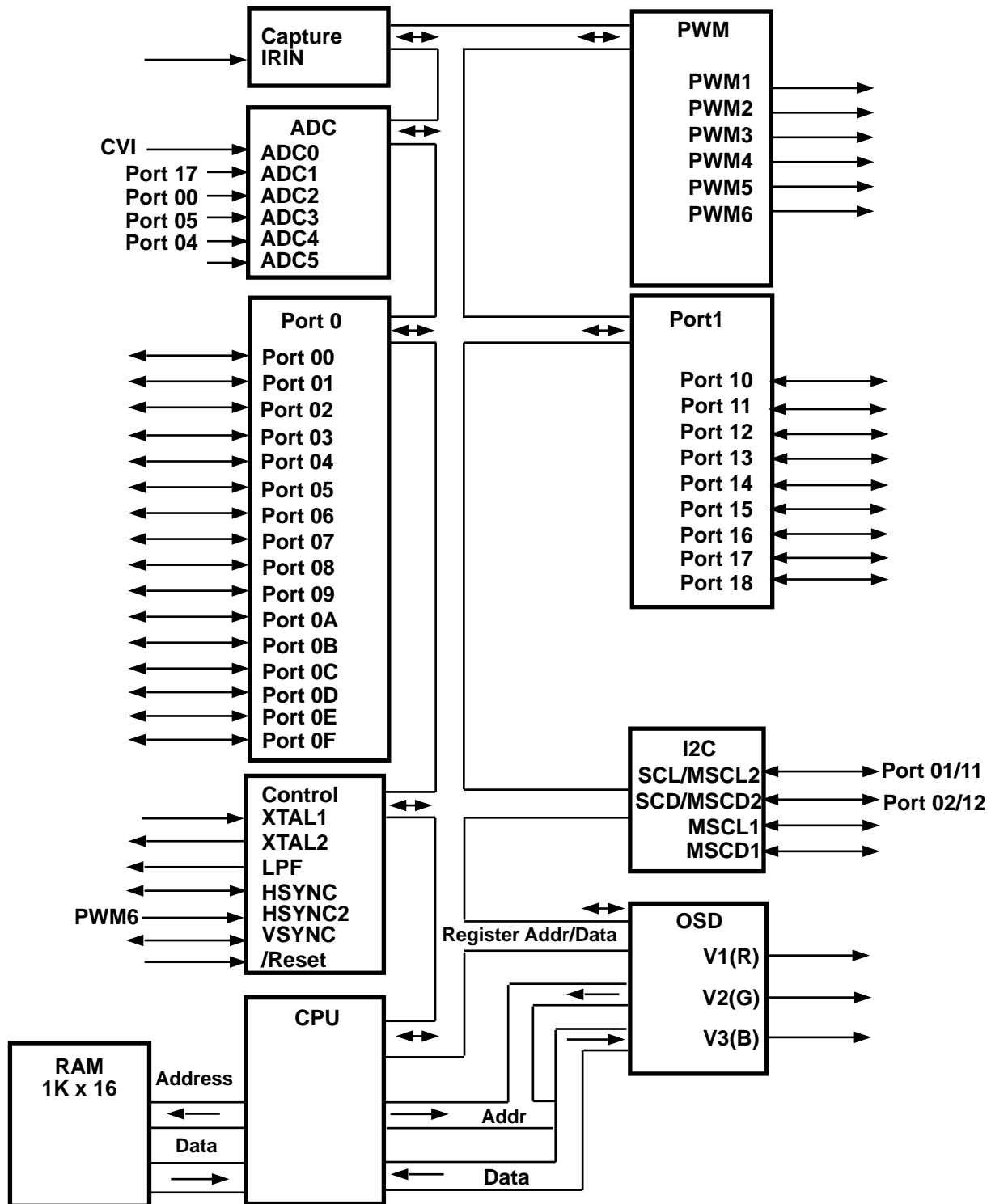
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: /B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

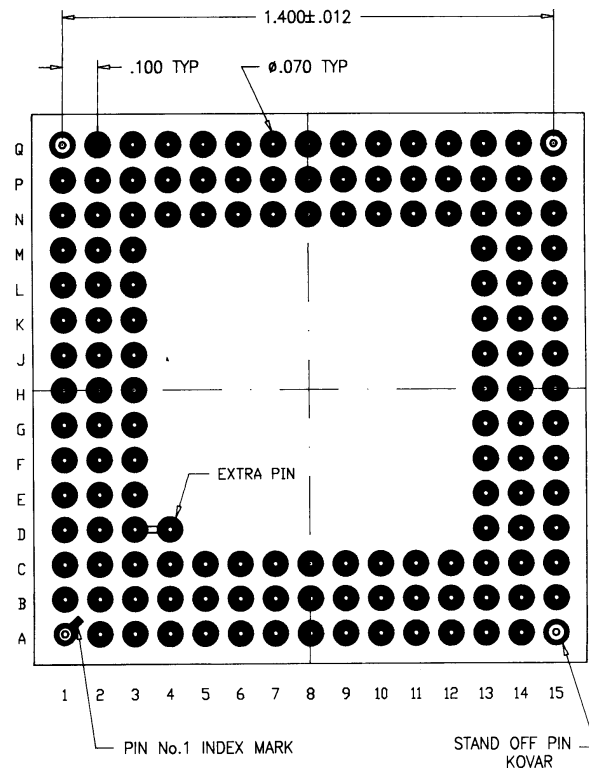
Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

GENERAL DESCRIPTION (Continued)

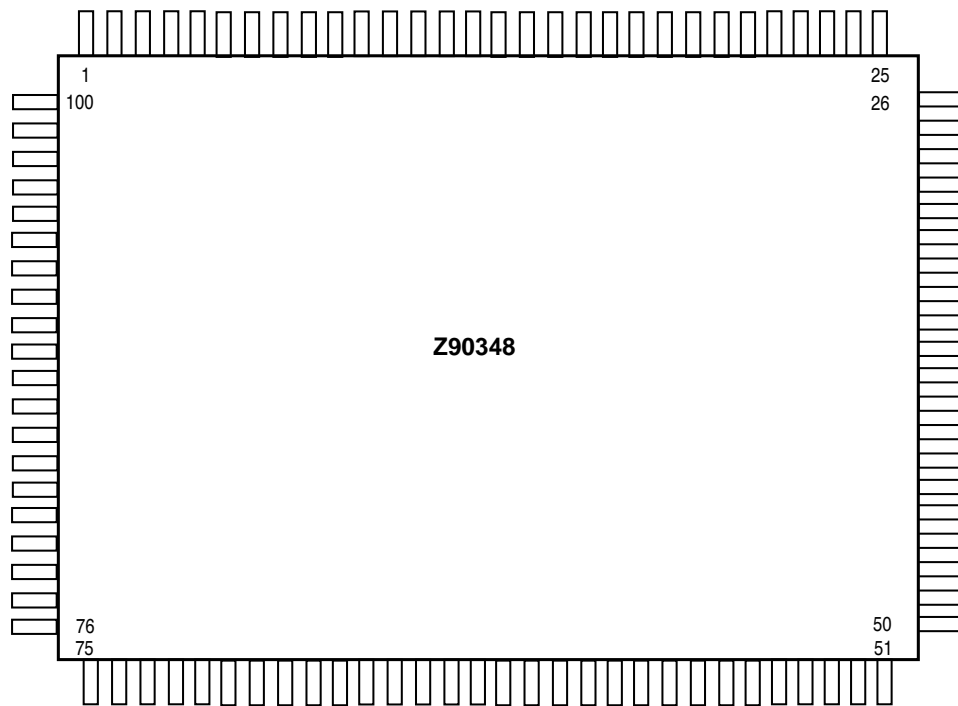


Functional Block Diagram

PIN DESCRIPTION



144-Pin PGA Configuration



100-Pin QFP Configuration

PIN DESCRIPTION (Continued)

Z90349/Z90348 Pin Identification Table

Number	Pin Name	144-Pin	100-Pin	Number	Pin Name	144-Pin	100-Pin
1	P03	D3	52	46	V1 (R)	R7	89
2	P02/I ² CSSC	C2	53	47	gnd	P8	
3	V _{CC}	B1		48	Blank	R8	90
4	gnd	D2		49	HSync	N8	91
5	address12	E3	54	50	int_bus4	N9	
6	address11	C1	55	51	VSync	R9	92
7	P01/I ² CSS0	E2	56	52	P12/I ² CMSC2	R10	93
8	address10	D1	57	53	int_bus5	P9	
9	address9	F3	58	54	P11/I ² CMSC2	P10	94
10	address8	F2	59	55	int_bus6	N10	95
11	address7	E1	60	56	P0E	R11	96
12	address6	G2	61	57	int_bus7	P11	97
13	CVI/ADC0	G3	62	58	I ² CMSC1	R12	98
14	address5	F1	63	59	V _{CC}	R13	
15	address4	G1	64	60	I ² CMSC1	P12	99
16	V _{CC}	H2		61	int_bus8	N11	100
17	gnd	H1		62	/Reset	P13	1
18	address3	H3	65		address 16	R14	
19	LPF	J3	66		address 15	N12	
20	address2	J1	67		XR/W	N13	
21	address1	K1	68		/XOE	P14	
22	address0	J2	69	63	XTAL1	P15	2
23	IE	K2	70	64	XTAL2	L13	3
24	R/W	K3	71	65	int_bus9	N15	
25	AGNDF	L1	72	66	gnd	L14	
26	sys_clk	L2	73	67	data15	M15	4
27	EA0	M1	74	68	data11	X13	5
28	EA1	N1	75	69	GND	K14	6
29	EA2	M2	76	70	data10	L15	7
30	ADC5	L3	77	71	data14	J14	8
31	P04/ADC4	N2	78	72	data13	J13	9
	address19	P1		73	data12	X15	10
	address18	M3		74	_pabus	J15	11*
	address17	N3		75	V _{CC} /V _{DD}	H14	12
32	P05/ADC3	N4	79	76	_romless	H15	13*
33	gnd	P3		77	data9	H13	14
34	P00/ADC2	P2	80	78	data8	G13	15
35	int_bus0	P4		79	data7	G15	16
36	P17/ADC1	N5	81	80	stopwdt	F15	
37	int_bus1	R3	82	81	AGNDX	G14	17
38	AGND	P5	83	82	single-stop	F14	
39	int_bus2	R4		83	data6	F13	18
40	AV _{CC}	N6	84	84	data5	E15	19
41	int_bus3	P6	85	85	data4	E14	20
42	P0F/strans	R5	86	86	data3	D15	21
43	V3 (B)	P7	87	87	PWM1	C15	22
44	V _{CC}	N7		88	data2	D14	23
45	V2 (G)	R6	88	89	data1	E13	24
				90	data0	C14	25
				91	V _{CC}	B15	

Number	Pin Name	144-Pin	100-Pin
92	PWM2	D15	26
93	gnd	C13	
	P1A	B14	
	P1B	A15	
	PIC	C12	
94	PWM3	B13	27
95	PWM4	A14	28
96	PWM5	B12	29
97	int_bus10	C11	30
98	PWM6	A13	31
99	int_bus11	B11	32
100	P10/4<0>	A12	33
101	int_bus12	C10	34
102	P08/R<1>	B10	35
103	VCC	A11	
104	P18/G<0>	B9	36
105	P13/G<1>	C9	37
106	gnd	A10	
107	P14/B<0>	A9	38
108	P15/B<1>	B8	39
109	int_bus13	A8	
110	P16/SCLK	C8	40
111	int_bus14	C7	
112	IRIN	A7	41
113	int_bus15	A6	
114	P0C	B7	42
115	P0B	B6	43
116	P0A	C6	44
117	P19	A5	45
118	P09	B5	46
119	V _{CC}	A4	
120	POD	A3	47
121	address14	B4	48
122	P07/CSync	C5	49
123	address13	B3	50
124	P06/Cnter	A5	51
	P1D	C4	
	P1E	C3	
	P1F	B2	

V1, V2, V3 ANALOG OUTPUT

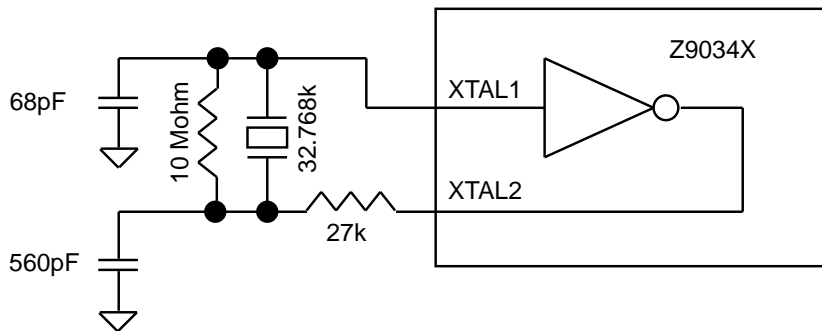
Specifications $V_{cc} = 5.25\text{ V}$

$V_{cc} = 5.25\text{ V}$	Condition	Limit
Output Voltage	Bit = 11	$2.10\text{ V} \pm 0.3\text{ V}$
	Bit = 10	$1.75\text{ V} \pm 0.30\text{ V}$
	Bit = 01	$1.28\text{ V} \pm 0.30\text{ V}$
	Bit = 00	0.0
Setting Time	70% of DC Level, 10pf Load	< 50 ns

V1, V2, V3 ANALOG OUTPUT

Specifications $V_{cc} = 4.75\text{ V}$

$V_{cc} = 4.75\text{ V}$	Condition	Limit
Output Voltage	Bit = 11	$1.90\text{ V} \pm 0.30\text{ V}$
	Bit = 10	$1.60\text{ V} \pm 0.30\text{ V}$
	Bit = 01	$1.20\text{ V} \pm 0.30\text{ V}$
	Bit = 00	0.0
Setting Time	70% of DC Level, 10pf Load	< 50 ns



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	-0.3	$V_{CC}+0.3$	V	Digital Inputs
V_{IA}	Input Voltage	-0.3	$V_{CC}+0.3$	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	-0.3	$V_{CC}+0.3$	V	All Push-Pull Digital Output
I_{OH}	Output Current High		-10/-1 ^a	mA	One Pin
I_{OH}	Output Current High		-100	mA	All Pins
I_{OL}	Output Current Low		20/1 ^b	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_S	Storage Temperature	-65	150	°C	

Notes:a) 1 mA max. when output pad impedance is 600 Ω .b) 1 mA max. when output pad impedance is 600 Ω .**DC CHARACTERISTICS** $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } +5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	$0.2 V_{CC}$	0.4	V	
V_{IH}	Input Voltage High	$0.6 V_{CC}$	V_{CC}	3.6	V	
V_{OL}	Output Voltage Low		0.4	0.16	V	@ $I_{OL} = 1 \text{ mA}$
V_{OH}	Output Voltage High	$V_{CC}-0.9$		4.75	V	@ $I_{OL} = 0.75 \text{ mA}$
V_{XL}	Input Voltage XTAL1 Low		$0.3 V_{CC}$	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	$V_{CC}-2.0$		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	μA	$V_{RL} = 0 \text{ V}$
I_{IL}	Input Leakage	-3.0	3.0	0.01	μA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1}	Supply Current		300	100	μA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		40	5	μA	Stop Mode

AC CHARACTERISTICS
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units	Note
T_{PC}	Input Clock Period	16	100	32	μs	
T_{RC}, T_{FC}	Clock Input Rise and Fall			12	μs	
$T_{D}POR$	Power On Reset Delay	0.8		1.2	s	Depends on Crystal

AC CHARACTERISTICS*
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
$T_{W}RES$	Power-On Reset Min. Width		5TPC		μs
$T_{D}H_S$	H_Sync Incoming Signal Width	5.5	12.5	11	μs
$T_{D}V_S$	V_Sync Incoming Signal Width	0.15	1.5	1.0	ms
$T_{D}E_S$	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	-12	+12	0	μs
$T_{D}O_S$	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	μs
$T_{W}HV_S$	H_Sync/V_Sync Edge Width		2.0	0.5	μs

Notes:

All timing of the I²C bus interface are defined by related specifications of the I²C bus interface.

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