

**Ordering Information**

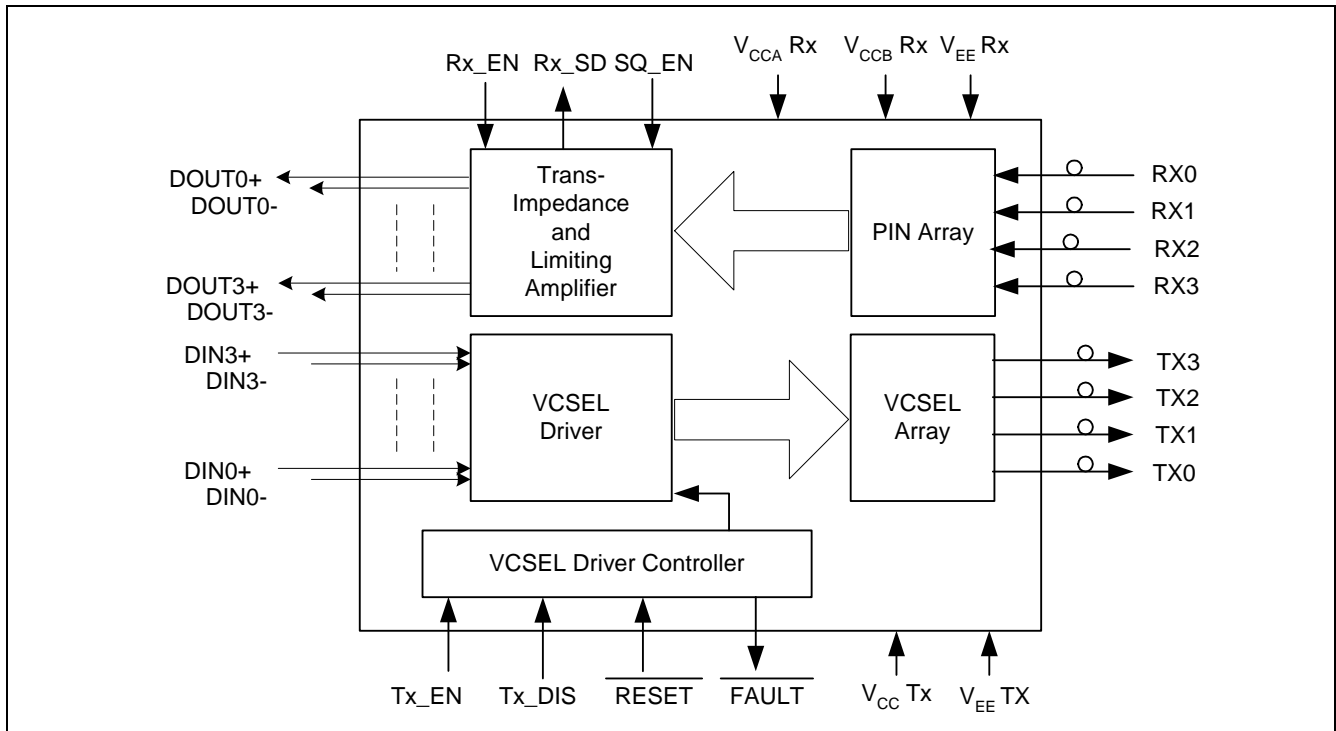
ZL60301/MJD Parallel Fiber Transceiver

Heat sink and EMI shield options  
 are available upon request

**0°C to +80°C**

**Features**

- Complies with POP4 MSA specification
- 4 Transmit channels and 4 Receive channels
- Data rate up to 2.7 Gbps per channel
- 850 nm VCSEL array
- Data I/O is CML compatible with DC blocking capacitors
- Link reach 300 m with 50/125 μm 500 MHz·km fiber at 2.5 Gbps
- Channel BER better than 10<sup>-12</sup>
- Industry standard MPO/MTP™ ribbon fiber connector interface
- Pluggable MegArray® ball grid array connector
- Optionally available with EMI shield and external heat sink
- Laser class 1M IEC 60825-1:2001 compliant
- Low power consumption, max 1 W
- Power supply 3.3 V



**Figure 1 - Transceiver Block Diagram**

## Applications

- High-speed interconnects within and between switches, routers and transport equipment
- Proprietary backplanes
- Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

## Description

The ZL60301 is a very high-speed transceiver for parallel fiber applications. This transceiver performs E/O and O/E conversions for data transmission over multimode fiber ribbon.

The transmit section converts parallel electrical input signals via a laser driver and a VCSEL array into parallel optical output signals at a wavelength of 850 nm.

The receive section converts parallel optical input signals via a PIN photodiode array and a transimpedance and limiting amplifier, into electrical output signals.

The module is fitted with a pluggable industry-standard MegArray<sup>®</sup> BGA connector. This provides ease of assembly on the host board and enables provisioning of bandwidth on demand.

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## Table of Contents

<b>Features</b> .....	<b>1</b>
<b>Applications</b> .....	<b>2</b>
<b>Description</b> .....	<b>2</b>
<b>Absolute Maximum Ratings</b> .....	<b>4</b>
<b>Recommended Operating Conditions</b> .....	<b>4</b>
<b>Transmitter Specifications</b> .....	<b>5</b>
Transmitter Control and Status Signal Requirements .....	7
Transmitter Control and Status Timing Diagrams .....	8
<b>Receiver Specifications</b> .....	<b>10</b>
Receiver Control and Status Signal Requirements .....	11
Receiver Control and Status Timing Diagrams .....	11
<b>Transceiver Module Signals</b> .....	<b>12</b>
Transceiver Pin Description .....	13
<b>Thermal Characteristics</b> .....	<b>14</b>
<b>Regulatory Compliance</b> .....	<b>16</b>
Eye safety .....	16
Electrostatic discharge .....	16
Electrostatic discharge immunity .....	16
Electromagnetic Interference .....	16
Emission .....	16
Immunity .....	16
<b>Handling instructions</b> .....	<b>16</b>
Cleaning the Optical Interface .....	16
Connectors .....	16
ESD handling .....	16
<b>Link Reach</b> .....	<b>17</b>
Link Model Parameters .....	17
<b>Electrical Interface - Application Examples</b> .....	<b>18</b>

## Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	$V_{CC}$	-0.3	4.0	V
Differential input voltage amplitude <sup>1</sup>	$\Delta V$		1.2	V
Voltage on any pin	$V_{PIN}$	-0.3	$V_{CC} + 0.3$	V
Relative humidity (non-condensing)	$M_{OS}$	5	95	%
Storage temperature	$T_{STG}$	-40	100	°C
ESD resistance	$V_{ESD}$		$\pm 1$	kV

1. Differential input voltage amplitude is defined as  $\Delta V = |DIN+ - DIN-|$ .

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	$V_{CC}$	3.135	3.465	V
Operating case temperature	$T_{CASE}$	0	80	°C
Signalling rate (per channel) <sup>1</sup>	$f_D$	1.0	2.7	Gbps
Link distance <sup>2</sup>	LD	2		m
Data I/O DC blocking capacitors <sup>3</sup>	$C_{BLK}$	100		nF
Power supply noise <sup>4</sup>	$V_{NPS}$		200	$mV_{p-p}$

1. Data patterns are to have maximum run lengths and DC balance shifts no worse than that of a Pseudo Random Bit Sequence of length  $2^{23}-1$  (PRBS-23). Information on lower bit rates and longer run lengths are available on request.

2. For maximum distance, see Table 4.

3. For AC-coupling, DC blocking capacitors external to the module with a minimum value of 100 nF is recommended.

4. Power supply noise is defined at the supply side of the recommended filter for all  $V_{CC}$  supplies over the frequency range of 500 Hz to 2700 MHz with the recommended power supply filter in place.

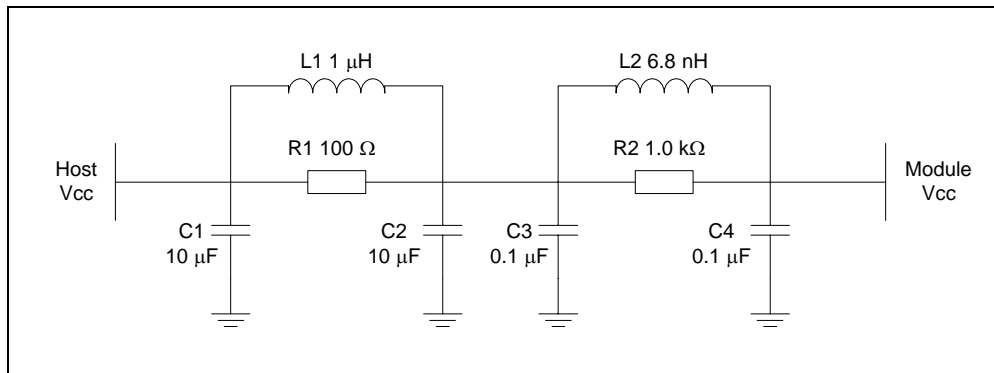


Figure 2 - Recommended Power Supply Filter

## Transmitter Specifications

All parameters below require operating conditions according to “Recommended Operating Conditions” on page 4.

Parameter	Symbol	Min.	Max.	Unit
<i>Optical Parameters</i>				
Launch power (50/125 $\mu\text{m}$ MMF) <sup>1</sup>	$P_{\text{OUT}}$	-8	-2	dBm
Extinguished output power	$P_{\text{OFF}}$		-30	dBm
Extinction ratio <sup>2</sup>	ER	6		dB
Optical modulation amplitude <sup>3</sup>	OMA	0.30		mW
Center wavelength	$\lambda_{\text{C}}$	830	860	nm
Spectral width <sup>4</sup>	$\Delta\lambda$		0.85	nm <sub>rms</sub>
Relative intensity noise OMA <sup>5</sup>	$\text{RIN}_{12\text{OMA}}$		-116	dB/Hz
Optical output rise time (20 - 80%)	$t_{\text{RO}}$		150	ps
Optical output fall time (20 - 80%)	$t_{\text{FO}}$		150	ps
Total jitter contributed (peak to peak) <sup>6</sup>	TJ		120	ps
Deterministic jitter contributed (peak to peak)	DJ		50	ps
Channel to channel skew <sup>7</sup>	$t_{\text{SK}}$		100	ps
<i>Electrical Parameters</i>				
Power dissipation	$P_{\text{D}}$		500	mW
Supply current	$I_{\text{CC}}$		150	mA
Differential input voltage amplitude (peak to peak) <sup>8</sup>	$\Delta V_{\text{IN}}$	200	800	mV <sub>p-p</sub>
Differential input impedance <sup>9</sup>	$Z_{\text{IN}}$	80	120	$\Omega$
Electrical input rise time (20 - 80%)	$t_{\text{RE}}$		160	ps
Electrical input fall time (20 - 80%)	$t_{\text{FE}}$		160	ps

1. The output optical power is compliant with IEC 60825-1 Amendment 2, Class 1M Accessible Emission Limits.

2. The extinction ratio is measured at 622 Mbps.

3. Informative. Corresponds to  $P_{\text{OUT}} = -8$  dBm and  $\text{ER} = 6$  dBm.

4. Spectral width is measured as defined in EIA/TIA-455-127 *Spectral Characterization of Multimode Laser Diodes*.

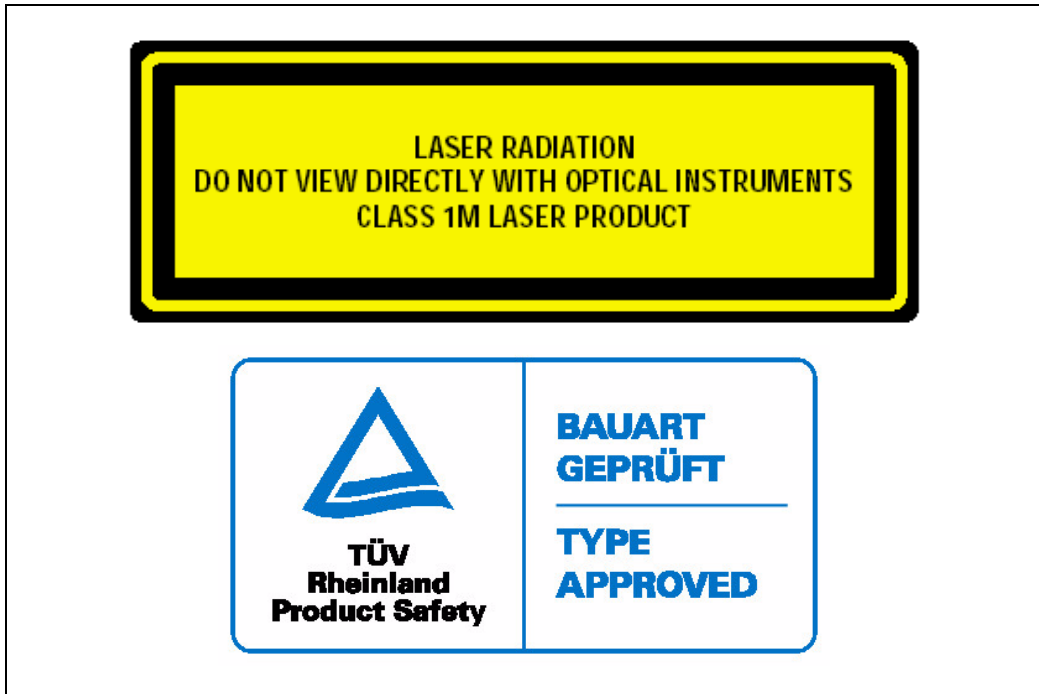
5. Corresponds to a Relative Intensity Noise (RIN) of -120 dB/Hz.

6. Total jitter equals TP1 to TP2 as defined in IEEE 802.3 clauses 38.2 and 38.6 (Gigabit Ethernet).

7. Channel skew is defined for the condition of equal amplitude, zero ps skew signals applied to the transmitter inputs.

8. Differential input voltage is defined as the peak to peak value of the differential voltage between DIN+ and DIN-. Data inputs are CML compatible.

9. Differential input impedance is measured between DIN+ and DIN-.



Classified in accordance with IEC 60825-1/A2:2001, IEC 60825-2 : 2000

Class 1M Laser Product

Emitted wavelength: 840 nm

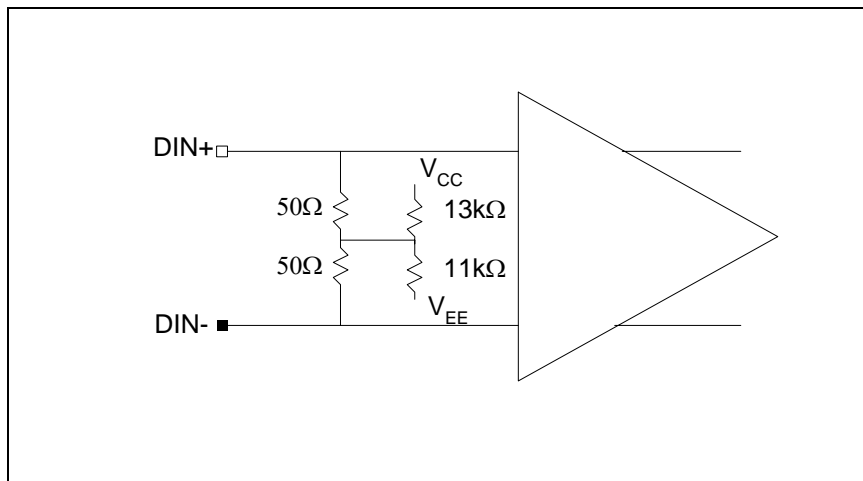


Figure 3 - Differential CML Input Equivalent Circuit

### Transmitter Control and Status Signal Requirements

The following table shows the timing relationships of the status and control signals of the transmit section.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control input voltage high <sup>1</sup>	V <sub>IH</sub>	2.1			V
Control input voltage low	V <sub>IL</sub>			0.62	V
Control pull-up resistor <sup>2</sup>	R <sub>PU</sub>		10		kΩ
Control pull-down resistor <sup>3</sup>	R <sub>PD1</sub>		10		kΩ
Status output voltage low <sup>4, 5</sup>	V <sub>OL</sub>			0.4	V
Status pull-down resistor <sup>4</sup>	R <sub>PD2</sub>		10		kΩ
$\overline{\text{FAULT}}$ assert time	T <sub>FA</sub>			100	μs
$\overline{\text{FAULT}}$ lasers off	T <sub>FD</sub>			100	μs
$\overline{\text{RESET}}$ duration	T <sub>TDD</sub>	10			μs
$\overline{\text{RESET}}$ assert time	T <sub>OFF</sub>		5	10	μs
$\overline{\text{RESET}}$ de-assert time	T <sub>ON</sub>			100	ms
Tx_EN assert time	T <sub>TEN</sub>			1	ms
Tx_EN de-assert time	T <sub>TD</sub>		5	10	μs
Tx_DIS assert time	T <sub>TD</sub>		5	10	μs
Tx_DIS de-assert time	T <sub>TEN</sub>			1	ms

1. Applies to control signals  $\overline{\text{RESET}}$ , Tx\_DIS and Tx\_EN.
2. Applies to control signals  $\overline{\text{RESET}}$  and Tx\_EN. Internal pull-up resistor.
3. Applies to control signal Tx\_DIS. Internal pull-down resistor.
4. Applies to status signal  $\overline{\text{FAULT}}$ . Internal pull-down to V<sub>EE</sub>.
5. With status output sink current max. 2 mA.

### Transmitter Control and Status Timing Diagrams

The following figures show the timing relationships of the status and control signals of the transmit section.

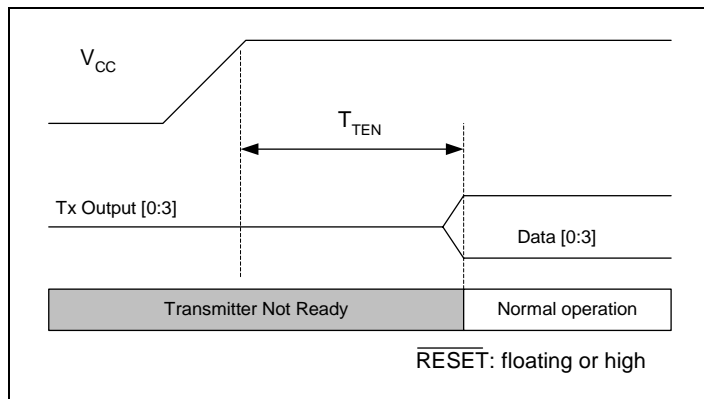


Figure 4 - Transmitter Power-up Sequence

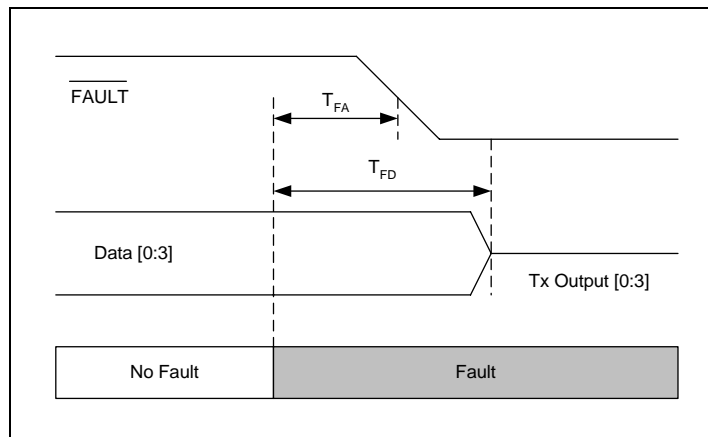


Figure 5 - Transmitter Fault Signal Timing Diagram



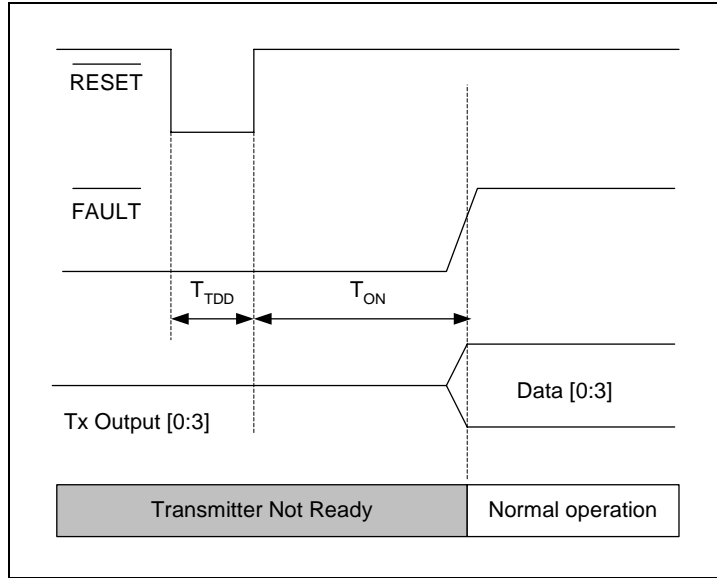


Figure 6 - Transmitter Reset Signal Timing Diagram

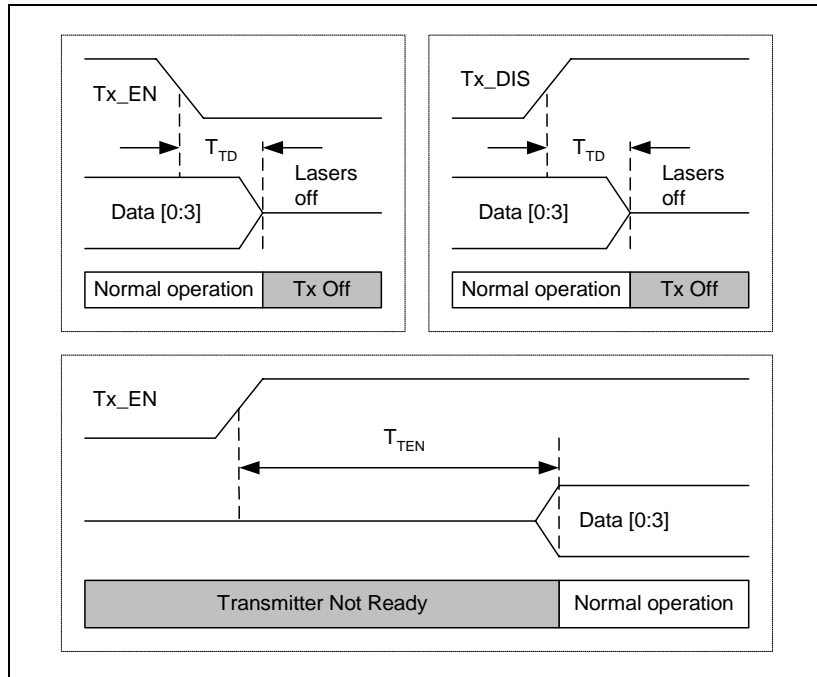


Figure 7 - Transmitter Enable and Disable Timing Diagram

	Tx_DIS High	Tx_DIS Low
Tx_EN High	Transmitter disabled	<b>Normal operation</b>
Tx_EN Low	Transmitter disabled	Transmitter disabled

Table 1 - TruthTable for Transmitter Operation (Pre-condition:  $\overline{\text{RESET}}$  floating or HIGH)

## Receiver Specifications

All parameters below require operating conditions according to “Recommended Operating Conditions” on page 4 and a termination load of 100  $\Omega$  differential at the electrical output.

Parameter	Symbol	Min.	Max.	Unit
<i>Optical Parameters</i>				
Input optical power <sup>1</sup>	$P_{IN}$	-16	-2	dBm
Center wavelength	$\lambda_C$	830	860	nm
Return loss <sup>2</sup>	RL	12		dB
Stressed receiver sensitivity <sup>3</sup>	$P_{SS}$		-11.7	dBm
Channel to channel skew <sup>4</sup>	$t_{SK}$		100	ps
Signal detect assert	$P_{SA}$		-17	dBm
Signal detect de-assert	$P_{SD}$	-31		dBm
<i>Electrical Parameters</i>				
Power dissipation	$P_D$		500	mW
Supply current	$I_{CC}$		150	mA
Differential output voltage amplitude (peak to peak) <sup>5</sup>	$\Delta V_{OUT}$	500	800	mV <sub>p-p</sub>
Output differential load impedance <sup>6</sup>	$Z_L$	80	120	$\Omega$
Stressed receiver eye opening <sup>7</sup>	$P_{SE}$	0.3		UI
Electrical output rise time (20 - 80%)	$t_{RE}$		160	ps
Electrical output fall time (20 - 80%)	$t_{FE}$		160	ps

1. Receive power for a channel is measured for a BER of  $10^{-12}$  and worst case extinction ratio.  $P_{IN}$  (Min) is measured using a fast rise/fall time source with low RIN and adjacent channel(s) operating with incident power of 6 dB above  $P_{IN}$  (Min).
2. Return loss is measured as defined in TIA/EIA-455-107A *Determination of Component Reflectance or Link/System Return Loss Using a Loss Test Set*.
3. The stressed receiver sensitivity is measured using PRBS 2<sup>23</sup>-1 pattern, 2.6 dB inter-symbol interference, ISI (Min), 30 ps duty cycle dependent deterministic jitter, DCD DJ (Min), and 6 dB extinction ratio, ER (Min) (ER penalty = 2.2 dB). All channels not under test are receiving signals with an average input power of 6 dB above  $P_{IN}$  (Min).
4. Channel skew is defined for the condition of equal amplitude, zero ps skew signals applied to the receiver inputs.
5. Differential output voltage is defined as the peak to peak value of the differential voltage between DOUT+ and DOUT- and measured with a 100  $\Omega$  differential load connected between DOUT+ and DOUT-. Data outputs are CML compatible.
6. See Figure 13.
7. The stressed receiver eye opening represents the eye at TP4 as defined in IEEE 802.3 clauses 38.2 and 38.6 (Gigabit Ethernet). The stressed receiver eye opening is measured using PRBS 2<sup>23</sup>-1 pattern, 2.6 dB ISI min, 30 ps DCD DJ min, 6 dB ER min and an average input power of -11.2 dBm (0.5 dB above minimum stressed receiver sensitivity as defined in IEEE 802.3 clause 38.6). All channels not under test are receiving signals with an average input power of 6 dB above  $P_{IN}$  (Min).

### Receiver Control and Status Signal Requirements

The following table shows the timing relationships of the status and control signals of the receive section.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control input voltage high <sup>1</sup>	$V_{IH}$	2.0			V
Control input voltage low <sup>1</sup>	$V_{IL}$			0.9	V
Control input pull-up current <sup>1</sup>	$ I_{IN} $	10		100	$\mu A$
Status output voltage low <sup>2, 3</sup>	$V_{OL}$			0.4	V
Status output pull-up resistor <sup>2</sup>	$R_{PU}$		3.25		$k\Omega$
Receiver signal detect assert time	$T_{SD}$		50	200	$\mu s$
Receiver signal detect de-assert time	$T_{LOS}$		50	200	$\mu s$
Receiver enable assert time	$T_{RXEN}$		33		ms
Receiver enable de-assert time	$T_{RXD}$		5		$\mu s$

1. Applies to control signals Rx\_EN, SQ\_EN.
2. Applies to status signal Rx\_SD. Internal pull-up to  $V_{CC}$ .
3. With status output sink current max 2 mA.

### Receiver Control and Status Timing Diagrams

The following figures show the timing relationships of the status and control signals of the receive section.

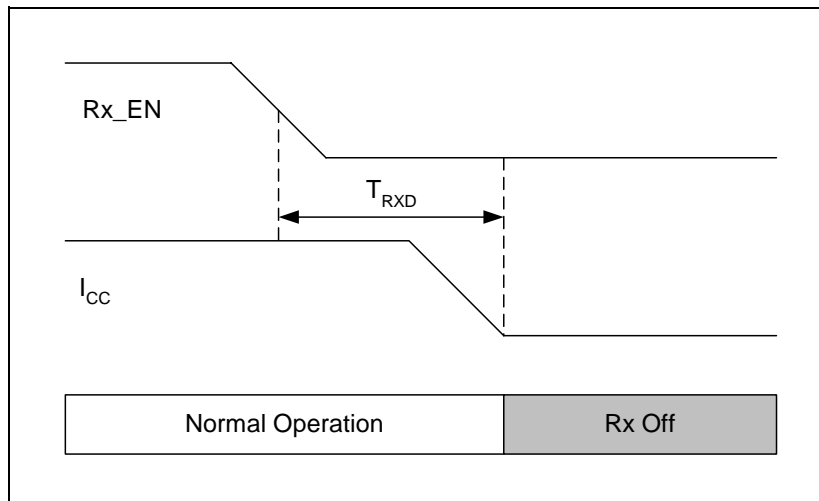


Figure 8 - Receiver Enable Signal Timing Diagram

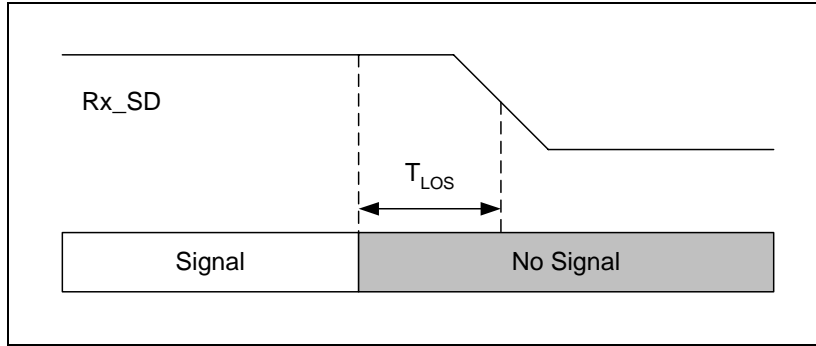


Figure 9 - Receiver Signal Detect Timing Diagram

**Transceiver Module Signals**

The pluggable parallel optical transceiver uses a 100 position FCI MegArray electrical connector (FCI PN: 84513-101), and an industry standard MTP™(MPO) optical receptacle compliant with IEC 61754-7.

	<b>K</b>	<b>J</b>	<b>H</b>	<b>G</b>	<b>F</b>	<b>E</b>	<b>D</b>	<b>C</b>	<b>B</b>	<b>A</b>
<b>1</b>	DOUT00-	V <sub>EE</sub> Rx	DOUT03+	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	DIN03-	V <sub>EE</sub> Tx	DIN00+
<b>2</b>	DOUT00+	V <sub>EE</sub> Rx	DOUT03-	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	DIN03+	V <sub>EE</sub> Tx	DIN00-
<b>3</b>	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx
<b>4</b>	DOUT01+	V <sub>EE</sub> Rx	DOUT02-	NIC	NIC	NIC	NIC	DIN02+	V <sub>EE</sub> Tx	DIN01-
<b>5</b>	DOUT01-	V <sub>EE</sub> Rx	DOUT02+	NIC	NIC	NIC	NIC	DIN02-	V <sub>EE</sub> Tx	DIN01+
<b>6</b>	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	V <sub>EE</sub> Rx	NIC	NIC	NIC	NIC	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx	V <sub>EE</sub> Tx
<b>7</b>	V <sub>CCB</sub> Rx	V <sub>CCB</sub> Rx	V <sub>CCB</sub> Rx	NIC	NIC	NIC	NIC	V <sub>CC</sub> Tx	V <sub>CC</sub> Tx	V <sub>CC</sub> Tx
<b>8</b>	NIC	DNC	DNC	DNC	RX_EN	TX_DIS	TX_EN	DNC	DNC	DNC
<b>9</b>	NIC	DNC	DNC	SD	SQ_EN	RESET	FAULT	DNC	DNC	DNC
<b>10</b>	V <sub>CCA</sub> Rx	V <sub>CCA</sub> Rx	V <sub>EE</sub> Rx	NIC	NIC	NIC	NIC	V <sub>EE</sub> Tx	V <sub>CC</sub> Tx	V <sub>CC</sub> Tx

Table 2 - Transceiver Pinout Assignments (Top view, toward MPO/MTP™ connector end) (10x10 array, 1.27 mm pitch)

Module front view - MTP key up											
Tx0	Tx1	Tx2	Tx3	-	-	-	-	Rx3	Rx2	Rx1	Rx0
Host printed circuit board											

Table 3 - Transceiver Optical Channel Assignment

### Transceiver Pin Description

The transceiver module case is electrically isolated from Transmitter signal common and Receiver signal common. Connection through mounting screw holes or frontplate whichever is applicable. Make the appropriate electrical connection for EMI shield integrity.

Signal Name	Type	Description	Comments
DIN[0:3] +/-	Data input	Transmitter data in, channel 0 to 3	Internal differential termination at 100 $\Omega$ .
V <sub>CC</sub> Tx		Transmitter power supply rail	
V <sub>EE</sub> Tx		Transmitter signal common. All transmitter voltages are referenced to this potential unless otherwise stated.	Directly connect these pads to the PC board transmitter signal ground plane.
TX_EN	Control input	Transmitter enable. HIGH: normal operation LOW: disable transmitter	Active high, internal pull-up. See Table 1.
TX_DIS	Control input	Transmitter disable. HIGH: disable transmitter LOW: normal operation	Active high, internal pull-down. See Table 1.
$\overline{\text{FAULT}}$	Status output	Transmitter fault. HIGH: normal operation LOW: laser fault detected on at least one channel	When active, all channels are disabled. Clear by reset signal. Internal pull-up.
$\overline{\text{RESET}}$	Control input	Transmitter reset. HIGH: normal operation LOW: reset to clear fault signal	Internal pull-up.
DOUT[0:3] +/-	Data output	Receiver data out, channel 0 to 3.	
V <sub>CCA</sub> Rx		PIN preamplifier power supply rail.	
V <sub>CCB</sub> Rx		Receiver quantizer power supply rail.	
V <sub>EE</sub> Rx		Receiver signal common. All receiver voltages are referenced to this potential unless otherwise stated.	Directly connect these pads to the PC board receiver signal ground plane.
RX_EN	Control input	Receiver enable. HIGH: normal operation LOW: disable receiver	Internal pull-up.
RX_SD	Status output	Receiver signal detect. HIGH: valid optical input on all channels LOW: loss of signal on at least one channel	Internal pull-up.
SQ_EN	Control input	Squelch enable. HIGH: squelch function enabled. Data OUT is squelched on any channels that have loss of signal LOW: squelch function disabled	Internal pull-up.
DNC		Do not connect to any potential, including ground.	
NIC		No internal connection.	

$V_{CCA}$  and  $V_{CCB}$  Rx can be connected to the same power supply. However, to insure maximum receiver sensitivity and minimize the impact of noise from the power supply, it is recommended to keep the power supplies separate and to use the recommended power supply filtering network on  $V_{CCA}$  Rx, see Figure 2.

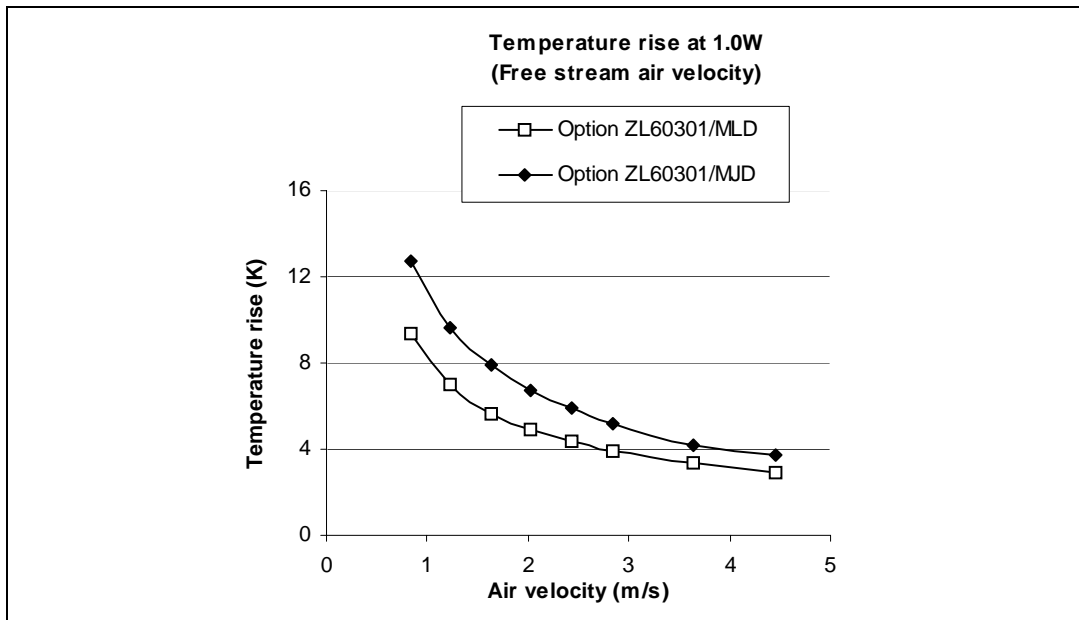
## Thermal Characteristics

There are three options for heat sinks depending on the cooling needs. They are:

1. Direct application without any attached external heat sink
2. Use a generic external heat sink specified by Zarlink
3. Use a customer designed external heat sink

In Figure 10 and Figure 11, the temperature rise and thermal resistance as a function of air velocity (free air velocity at the top of the module) is shown for option 1 and 2. The thermal resistance is defined as the temperature difference between the case temperature and ambient flowing air divided by the total heat dissipation of the module.

Improved thermal properties can be achieved by using a larger heat sink especially if more height is available (option 3). For this option, a more detailed discussion with Zarlink is recommended regarding heat sink design attachment materials.



**Figure 10 - Temperature Difference Between Ambient Flowing Air and Case at a Heat Dissipation of 1.0 W**

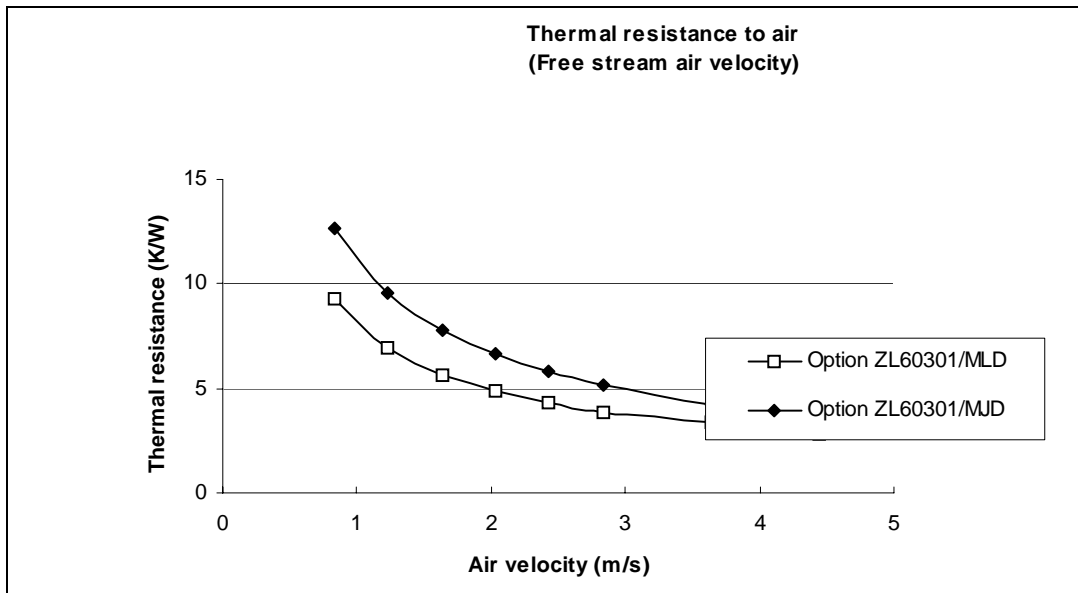


Figure 11 - Thermal Resistance, as a Function of Air Velocity (the airflow is along the shortest side of the module)

For any other orientation, the thermal resistance is 75-100% of the values shown above.

## Regulatory Compliance

### Eye safety

The maximum optical output power is specified to comply with Class 1M in accordance with IEC 60825-1:2001. In addition the transmitter complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No.50, dated July 26, 2001. No maintenance or service of the product may be performed.

### Electrostatic discharge

The module is classified as Class 1 (> 1000 Volts) according to MIL-STD-883, test method 3015.7, with regards to the electrical pads.

### Electrostatic discharge immunity

The part withstand a 15 kV (air discharge) and 8 kV (contact discharge) either indirect or directly to receptacle; tested according to IEC 61000-4-2, while in operation without addition of bit errors.

### Electromagnetic Interference

#### Emission

The electromagnetic emission is tested in front of the module (module fitted with EMI shield), with the module mounted in a frontplate cutout. The part is tested with FCC Part 15, 30 – 1000 MHz and 1 GHz to 5<sup>th</sup> harmonic of the highest fundamental frequency (6.75 GHz), and is specified to be Class B with > 6 dB margin.

#### Immunity

The electromagnetic immunity is tested without a front panel or enclosure. The module specification is maintained with an applied field of 10 V/m for frequencies between 10 kHz and 10 GHz, according to IEC 61000-4-3 and GR-1089-CORE.

## Handling instructions

### Cleaning the Optical Interface

A protective connector plug is supplied with each module. This plug should remain in place whenever a fiber cable is not inserted. This will keep the optical port free from dust or other contaminants, which may potentially degrade the optical signal. Before reattaching the connector plug to the module, visually inspect the plug and remove any contamination. If the module's optical port becomes contaminated, it can be cleaned with high-pressure nitrogen (the use of fluids, or physical contact, is not advised due to potential for damage).

Before a fiber cable connector is attached to the module, it is recommended to clean the fiber cable connector using an optical connector cleaner, or according to the cable manufacturer's instructions. It is also recommended to clean the optical port of the module with high-pressure nitrogen.

### Connectors

For optimum performance, it is recommended that the number of insertions is limited to 50 for the electrical MegArray connector and 200 for the optical MPO/MTP connector.

### ESD handling

When handling the modules, precautions for ESD sensitive devices should be taken. These include use of ESD protected work areas with wrist straps, controlled work-benches, floors etc.



## Link Reach

The following table lists the minimum reach distance of the pluggable parallel fiber optic transceiver for different multi-mode fiber (MMF) types and bandwidths assuming worst case parameters. Each case allows for a maximum of 2 dB per channel connection loss for patch cables and other connectors.

Fiber Type [core / cladding $\mu\text{m}$ ]	Modal Bandwidth @ 850 nm [MHz*km]	Reach Distance @ 1 Gbps [m]	Reach Distance @ 2.5 Gbps [m]	Reach Distance @ 2.7 Gbps [m]
62.5/125 MMF	200	350	135	115
62.5/125 or 50/125 MMF	400	650	260	220
50/125 MMF	500	750	300	270

**Table 4 - Link Reach for Different Fiber Types and Data Rates**

## Link Model Parameters

The link reaches above have been calculated using the following link model parameters and Gigabit Ethernet link model version 2.3.5 (filename: 5pmd047.xls).

Parameter	Symbol	Value	Unit
Mode partition noise k-factor	k	0.3	
Modal noise	MN	0.3	dB
Dispersion slope parameter	$S_O$	0.11	ps/nm <sup>2</sup> *km
Wavelength of zero dispersion	$U_O$	1320	nm
Attenuation coefficient at 850 nm	$\alpha_{\text{dB}}$	3.5	dB/km
Conversion factor	C1	480	ns.MHz
Q-factor [BER $10^{-12}$ ]	Q	7.04	
TP4 eye opening		0.3	UI
DCD allocation at TP3	DCD DJ	0.08	UI
RMS baseline wander S.D.	$\sigma_{\text{BLW}}$	0.025	
RIN coefficient	$k_{\text{RIN}}$	0.70	
Conversion factor	c_rx	329	ns.MHz

Electrical Interface - Application Examples

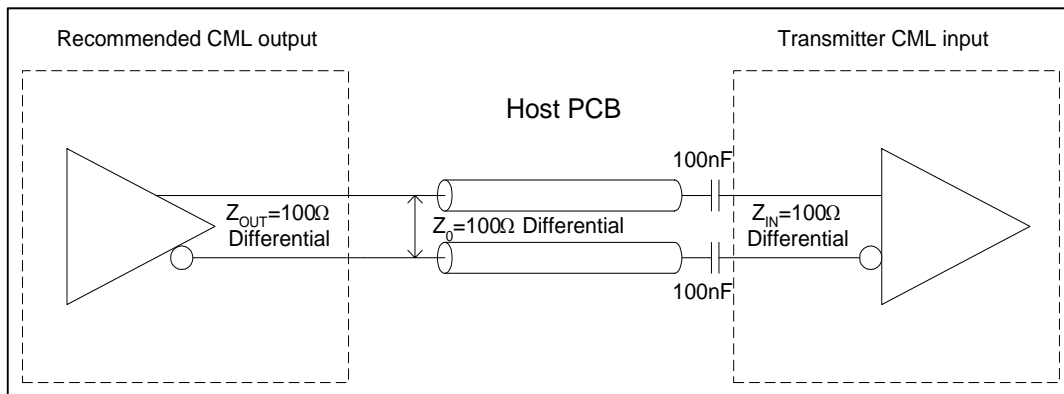


Figure 12 - Recommended Differential CML Input Interface

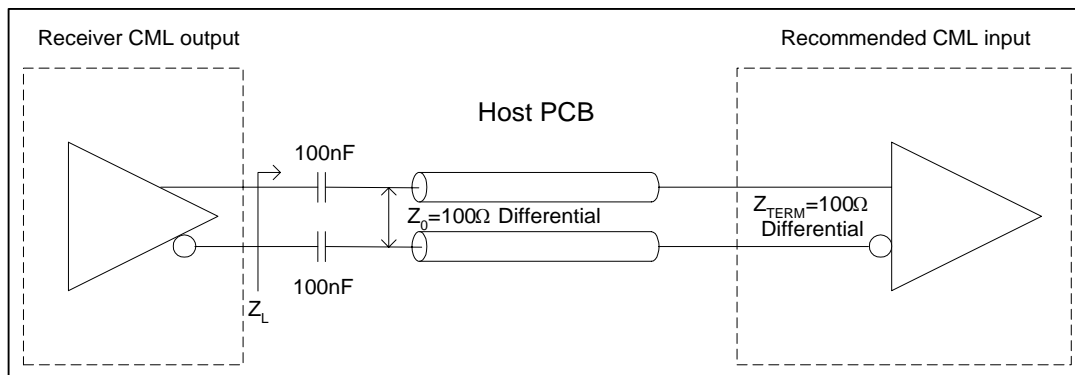
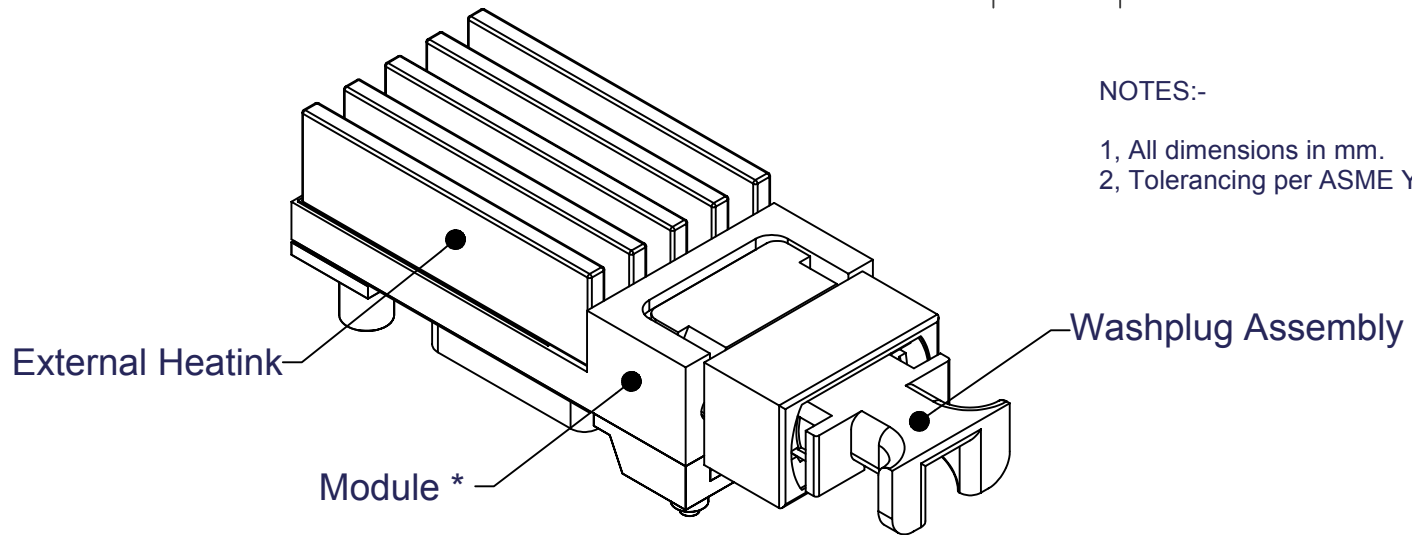
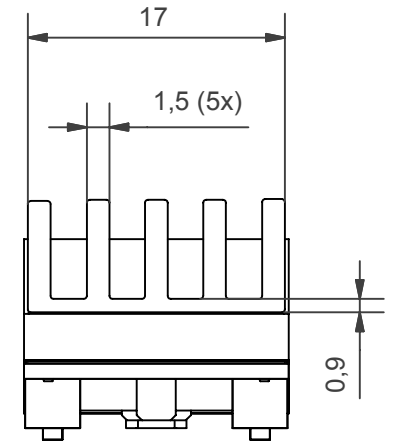
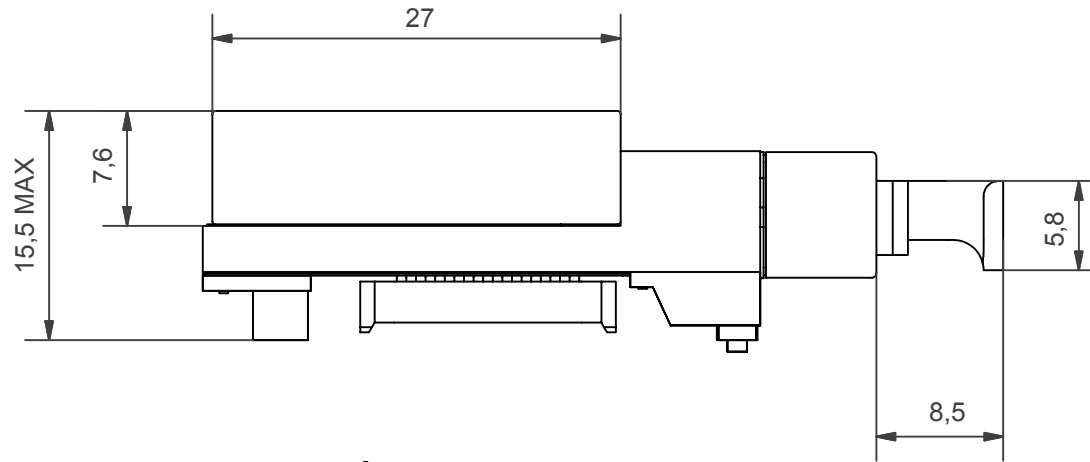
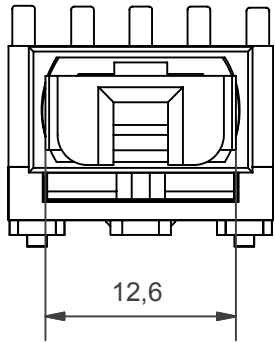


Figure 13 - Recommended Differential CML Output Interface

FRONT VIEW ( 2 : 1 )



NOTES:-

- 1, All dimensions in mm.
- 2, Tolerancing per ASME Y14.5M-1994

\* For details of the module, see separate data sheet and/or package drawing.

Projection Method

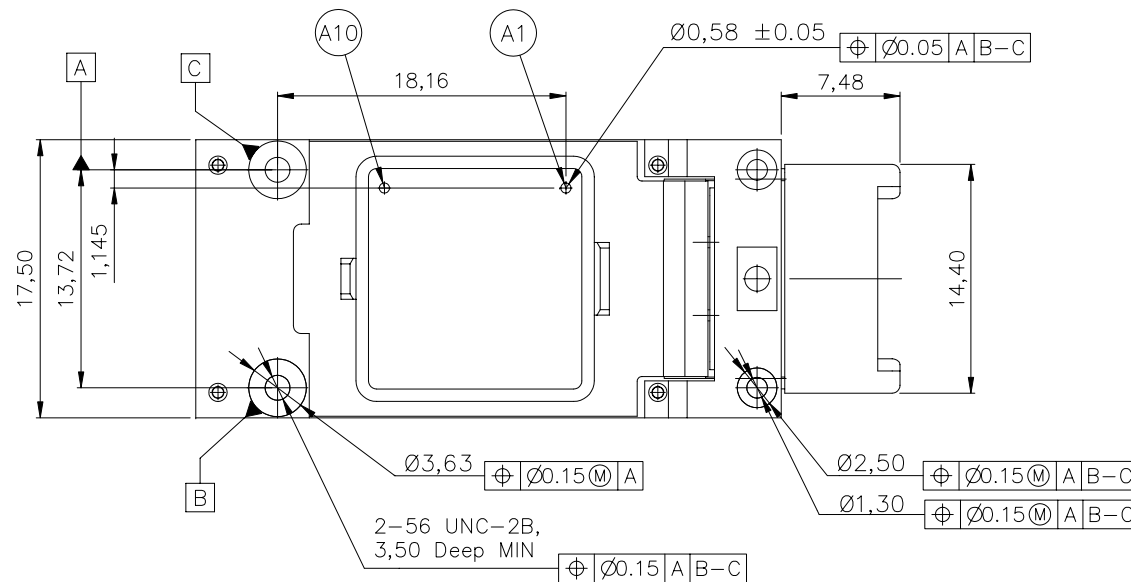
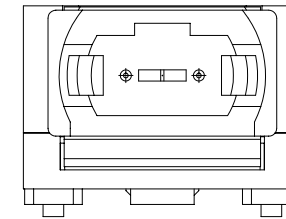
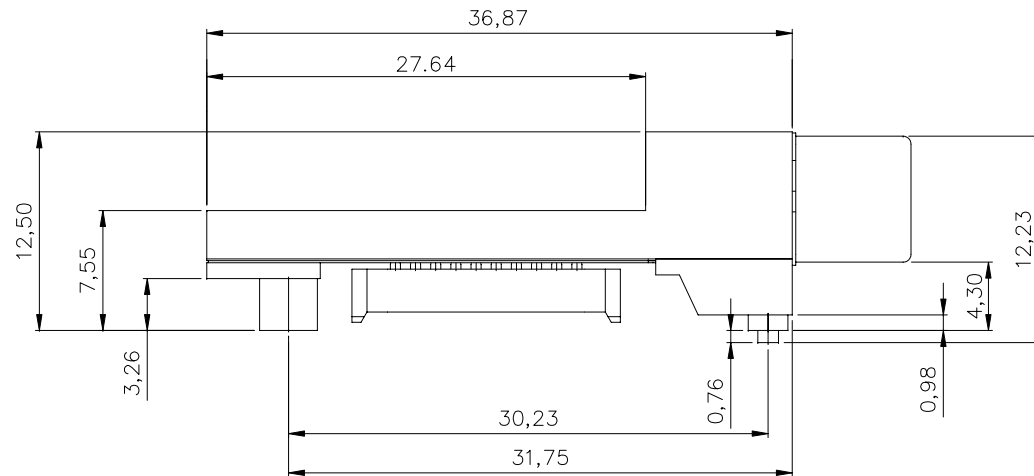
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ISSUE	2			
ACN	104518 rev2			
DATE	11-AUG-04			
APPRD.	MD/MA			



Package code	ML
Previous package codes	
Title	104518

Drawing type	Package Drawing, Module Layout External Heatsink
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NOTES:-

1. All dimensions in mm.
2. Tolerancing per ASME Y14.5M-1994.

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DATE	12-JUN-03			
APPRD.	TD/BE			

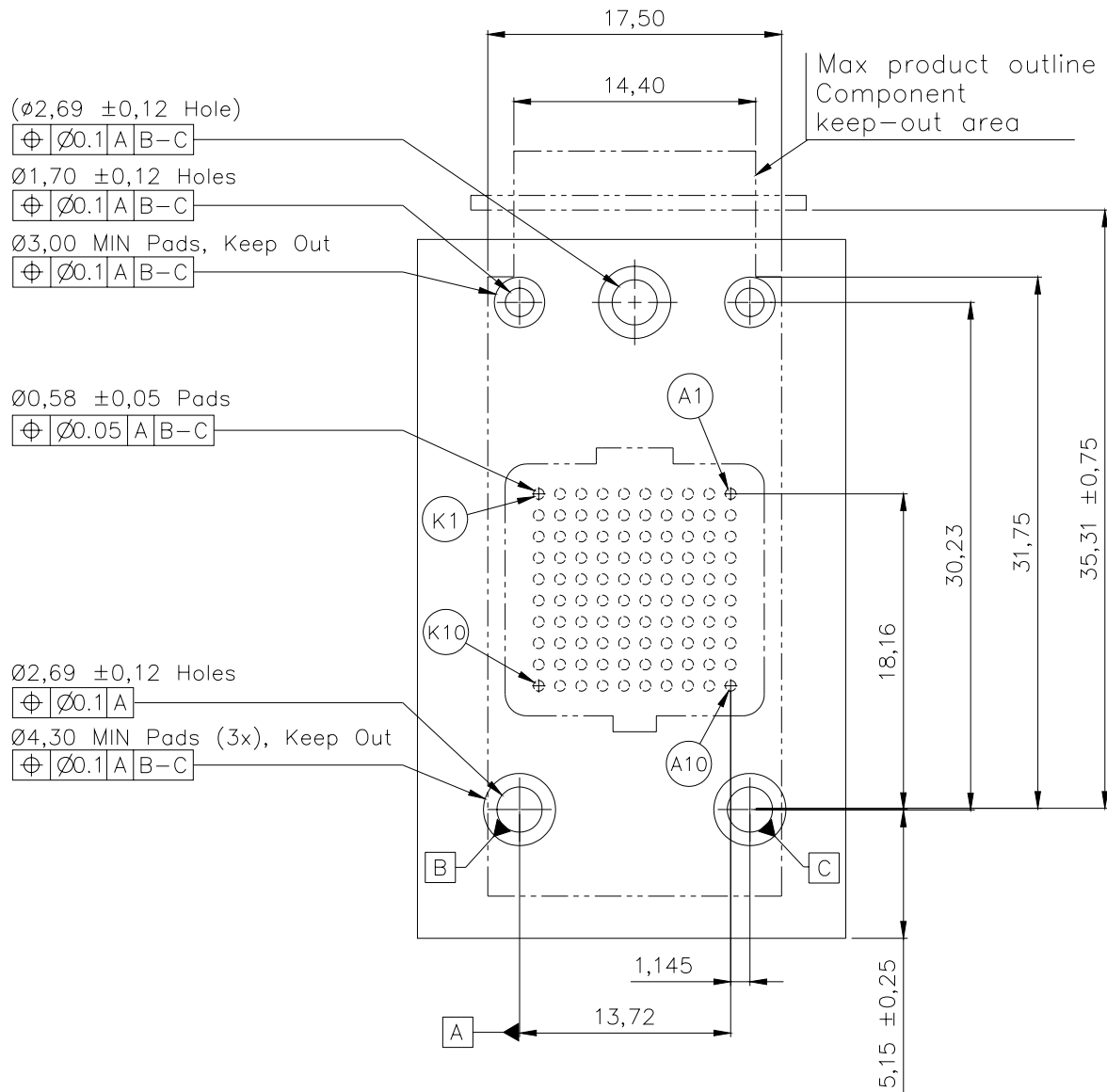


Previous package codes

Package code **MJ**

Drawing type  
Package drawing - module layout

Title **JS004296**



NOTES:-

1. All dimensions in mm.
2. Tolerancing per ASME Y14.5M-1994.

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Previous package codes

Package code **MJ**

Drawing type  
 Package Drawing,  
 Host circuit board footprint layout

Title **JS004296**



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