CableCARD™ INTERFACE CONTROLLER
CXD1969
Customer Requirements Specification

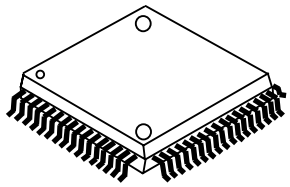
DESCRIPTION

The CXD1969 is an 'Plug & Play' and OpenCable™ CableCARD™ interface controller IC designed for use with OpenCable™ compliant CableCARD™ modules. It performs the communication interface between a host microcontroller and the CableCARD™. The IC communicates to the Host either by a 68k-type or I^2C connection. Communication between the CXD1969 and the CableCARD™ is highly efficient due to the inclusion of a fully integrated hardware Physical layer.

MPEG2 Transport Stream interfaces are fully programmable ensuring compatibility to commonly used Front End demodulators and MPEG2 decoders.

A SCTE 28 compliant software stack is also available for this device.

100 pin Plastic LQFP



FEATURES

PC Card Interface
- Fully integrated CableCARD™ interface.
- Support for generic PC Cards.
- Supports 3V3 modules (VPP either 3V3 or 5V)
- Integrated Physical layer with 1Kbyte buffers.

Host Interface
- 68k-type host bus interface
  - 27MHz or 33MHz operating frequency.
- I^2C host bus interface.
  - 100kHz or 400kHz operation.
- Maskable/programmable interrupt capability.
- 3V3 logic levels.

OOB Interface
- Supports SCTE 28 Bidirectional OOB I/F.

Transport Stream Interfaces
- Accepts MPEG2 compliant TS.
- SCTE28 compliant parallel TS interfaces to/from POD Card.
- TS interface from tuner (up to 72Mbits/s).
- Serial TS interface to downstream device (up to 72Mbits/s).
- Four serial input and output modes.

Miscellaneous
- Integrated PLL for serial TS.
- 5V compatible I/Os.
- LQFP 100-pin package.

APPLICATIONS
- iDTV
- Set Top Box
- Personal Video Recorder (PVR)

2 Key differences between CXD2099AR and CXD1969

- Clock frequency can be 27MHz or 33MHz
- No change to 68k host interface
- Polarity/function of HIRQ is now programmable
- Removed ability to extend data and address lines by the use of external buffers
- TS Input I/F is now serial only, (parallel TS input removed)
- No change to TS Output I/F
- Hot-swap state machine removed
- Support for dual-slot removed
- VCCSW and OVERLOAD functionality removed
- VCCSEL changed to VPPSEL to support 3V3 or 5V PODs
- Bidirectional OOB I/F added
- Technology process change, some changes to DC spec
- Pinout optimized for POD