Genesys Logic, Inc.

GL824/GL824C

USB 2.0
On-The-Go Controller

Datasheet
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Revision History

Revision	Date	Description
1.00	10/24/2005	First Formal Release
1.01	02/24/2006	1.Modify External Memory Flash Interface to ATA/ATAPI Interface 2.Change DRVVBUS pin's description. 3.Change SDRAM Interface to SDRAM/HOST Interface
1.02	04/19/2006	Change flash ROM to reprogrammable flash memory in page10.
1.03	06/02/2006	Modified the timing diagram of host interface
1.04	07/10/2006	Modified the timing diagram and parameter of host interface
1.05	08/15/2006	Modified the timing diagram of host interface
1.06	11/07/2006	Modified the timing diagram of host interface

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TABLE OF CONTENTS

CHAPTER 1 GENERAL DESCRIPTION 9

CHAPTER 2 FEATURES 10

CHAPTER 3 PIN ASSIGNMENT 12

3.1 PINOUT 12

3.2 PIN LIST 14

3.3 PIN DESCRIPTIONS 16

CHAPTER 4 BLOCK DIAGRAM 24

CHAPTER 5 FUNCTION DESCRIPTION 25

5.1 OTG (ON-THE-GO) 25

5.2 SIE (SERIAL INTERFACE ENGINE) 25

5.3 EPFIFO (ENDPOINT FIFO) 25

5.4 SSI (SYNCHRONOUS SERIAL INTERFACE) 25

5.4.1 One Byte Receive/Transmit Mode 25

5.4.2 Continues Receive/Transmit Data Mode 26

5.5 UART (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) 27

5.6 HOST INTERFACE 27

CHAPTER 6 ELECTRICAL CHARACTERISTICS 31

6.1 ABSOLUTE MAXIMUM RATINGS 31

6.2 OPERATING CONDITIONS 31

6.3 DC CHARACTERISTICS 31

6.4 PMOS CHARACTERISTICS 32

6.5 AC CHARACTERISTICS 34

6.5.1 External Flash 34

6.5.2 SmartMedia 35

6.5.3 xD-Picture 36

6.5.4 Memory Stick 37

6.5.5 Memory Stick PRO 37

6.5.6 Secure Digital / MultiMedia Card 37

6.5.7 CompactFlash Card 38

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6.5.8 Reset Timing 39
6.5.9 ATA/ ATAPI 39
6.5.10 Register Transfers 41
6.5.11 Multiword DMA data transfer 42
6.5.12 Ultra DMA data transfer 46
CHAPTER 7 PACKAGE DIMENSION 54
CHAPTER 8 ORDERING INFORMATION 56

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LIST OF FIGURES

FIGURE 3.1 - 208 PIN LQFP PINOUT DIAGRAM 12
FIGURE 3.2 – 128 PIN LQFP PINOUT DIAGRAM 13
FIGURE 4.1 - GL824 BLOCK DIAGRAM 24
FIGURE 5.1 - ONE BYTE RECEIVE/TRANSMIT TIMING DIAGRAM (CLOCK OPPOSITE) 26
FIGURE 5.2 - ONE BYTE RECEIVE/TRANSMIT TIMING DIAGRAM (CLOCK NORMAL) 26
FIGURE 5.3 - CONTINUES RECEIVE/TRANSMIT DATA TIMING DIAGRAM (CLOCK OPPOSITE) 26
FIGURE 5.4 - CONTINUES RECEIVE/TRANSMIT DATA TIMING DIAGRAM (CLOCK NORMAL) 26
FIGURE 5.5 - DATA FRAME 27
FIGURE 5.6 - COMMAND WRITE TIMING DIAGRAM 28
FIGURE 5.7 - STATUS READ TIMING DIAGRAM 28
FIGURE 5.8 - DATA WRITE TIMING DIAGRAM 29
FIGURE 5.9 - DATA READ TIMING DIAGRAM 29
FIGURE 6.1 – EMBEDDED PMOS SWITCH ARCHITECTURE 32
FIGURE 6.2 – I-V CURVE OF PMOS SWTICH 33
FIGURE 6.3 – TRANSIENT ANALYSIS OF PMOS SWITCH 34
FIGURE 6.4 – TIMING DIAGRAM OF EXTERNAL FLASH 34
FIGURE 6.5 - TIMING DIAGRAM OF SMARTMEDIA 35
FIGURE 6.6 - TIMING DIAGRAM OF XD-PICTURE 36
FIGURE 6.7 - TIMING DIAGRAM OF MEMORYSTICK 37
FIGURE 6.8 - TIMING DIAGRAM OF MEMORYSTICK PRO 37
FIGURE 6.9 - TIMING DIAGRAM OF SD / MMC 37
FIGURE 6.10 - TIMING DIAGRAM OF COMPACTFLASH 38
FIGURE 6.11 - TIMING DIAGRAM OF RESET 39
FIGURE 6.12 – REGISTER TRANSFERS TIMING 41
FIGURE 6.13 - INITIATING A MULTIWORD DMA DATA BURST 43
FIGURE 6.14 - SUSTAINING A MULTIWORD DMA DATA BURST 44
FIGURE 6.15 - DEVICE TERMINATING A MULTIWORD DMA DATA BURST 44

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FIGURE 6.16 - HOST TERMINATING A MULTIWORD DMA DATA BURST 45
FIGURE 6.17 - INITIATING AN ULTRA DMA DATA-IN BURST 47
FIGURE 6.18 - SUSTAINED ULTRA DMA DATA-IN BURST 47
FIGURE 6.19 - HOST PAUSING AN ULTRA DMA DATA-IN BURST 48
FIGURE 6.20 - DEVICE TERMINATING AN ULTRA DMA DATA-IN BURST 48
FIGURE 6.21 - HOST TERMINATING AN ULTRA DMA DATA-IN BURST 49
FIGURE 6.22 - INITIATING AN ULTRA DMA DATA-OUT BURST 50
FIGURE 6.23 - SUSTAINED ULTRA DMA DATA-OUT BURST 50
FIGURE 6.24 - DEVICE PAUSING AN ULTRA DMA DATA-OUT BURST 51
FIGURE 6.25 - HOST TERMINATING AN ULTRA DMA DATA-OUT BURST 52
FIGURE 6.26 - DEVICE TERMINATING AN ULTRA DMA DATA-OUT BURST 53
FIGURE 7.1 - GL824 208 PIN LQFP PACKAGE 54
FIGURE 7.2 - GL824C 128 PIN LQFP PACKAGE 55

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LIST OF TABLES

TABLE 3.1 -GL824 208 PIN LQFP PIN LIST 14
TABLE 3.2 – GL824C 128-PIN LQFP PIN LIST 15
TABLE 3.3 – GL824 208 PIN DESCRIPTIONS 16
TABLE 3.4 – GL824C 128 PIN DESCRIPTIONS 20
TABLE 5.1 - AC CHARACTERISTICS 27
TABLE 5.2 - HOST INTERFACE AC CHARACTERISTICS 29
TABLE 6.1 - ABSOLUTE MAXIMUM RATINGS 31
TABLE 6.2 - OPERATING CONDITIONS 31
TABLE 6.3 - DC CHARACTERISTICS 31
TABLE 6.4 – PMOS CHARACTERISTICS 32
TABLE 6.5 - ULTRA DMA DATA BURST TIMING REQUIREMENTS 46
TABLE 8.1 - ORDERING INFORMATION 56

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CHAPTER 1 GENERAL DESCRIPTION

The GL824/824C USB On-The-Go (OTG) Dual-Role-Device controller which include Milti-I/F and ATA/ATAPI interface is a highly integral microprocessor, which optimized and specially designed for embedded system, portable device, multi-function peripheral and consumer products with External uP interface, SSI, I2C and Flash cards interface.Using the GL824, developers can create OTG-compliant dual-role products capable of point-to-point communication. Its focus on power efficiency makes the GL824 ideal for set top box, DVD player, PDA, PMP, Digital TV and home entertainment with USB OTG and Flash card reader.

The GL824/GL824C had USB 2.0 Multi-I/F and SD/MMC/MS/MSPro Interface Flash Card Reader Controller. It supports USB 2.0 high-speed transmission to:
CompactFlash ™ (CF) Type I/II, Micro Drive, Secure Digital™ (SD), Mini SD™, MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), HS-MMC, MMC-Mobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick Pro™ (MS Pro), Memory Stick Pro™ Duo (MS Pro Duo) Memory Stick ROM, SmartMedia™ (SM) 5V/3.3V, and xD-Picture Card ™ (xD) on one chip (GL824C are SD/MMC/MS/MSPro I/F only).

The GL824/GL824C also embeds a powerful 8-bit MCU engine to handle the operations among the USB host, peripheral, OTG and ATA/ATAPI controllers. Provide flexibility Card-to-HDD, HDD-to-Card, USB-to-HDD, HDD-to-USB, USB-to-Card and Card-to-USB multi-path copy back bridge.

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CHAPTER 2 FEATURES

- USB OTG Controller
  - Compliant with USB specification Rev. 2.0 at high-speed and full-speed data transfer rate
  - Compliant with On-The-Go (OTG) supplement Rev. 1.0
  - Complies with USB Storage Class specification rev. 1.0
  - Support Suspend, Resume, HNP and SRP
  - External source to drive Vbus signal
  - Supports 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 1 clocks per instruction cycle
  - Embedded 64K*2 Byte reprogrammable flash memory and internal 256 byte SRAM
  - Embedded 8K Byte external SRAM
- Support power saving mode
- Support firmware upgrade via USB and external serial flash memory
- On-Chip power MOSFETs for supplying flash media card power except Compact Flash. (GL824 only)
- Interface
  - Support external SDRAM interface (option)
  - Support 16bit host interface (Support external uP Read/Write Status/Command and Read/Write FIFO) (option)
  - Supports ATA/ATAPI interface
  - Support serial MP3 decoder interface
  - Support serial LCD Panel interface
  - Support memory cards interface
  - Support SSI interface for master and slave mode up to 15MHz
  - Support I2C interface
  - Support UART interface
- ATA/ATAPI interface
  - Complies with ATA/ATAPI-6 specification rev 1.0
  - Support 16-bit Multiword DMA mode and Ultra DMA mode interface (Ultra 33/66)
- CompactFlash™ interface (GL824 only)
  - Support CFA specification v2.1 / v3.0
  - Support True IDE mode
  - Support 8 / 16 bit data mode and different timing

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- xD-Picture Interface (GL824 only)
  - xD-Picture specification v1.2B
  - xD-Picture Type M card support
- SmartMedia™ interface (GL824 only)
  - 8 bit data width and different speed
  - Support different page size, and automatic append redundant area data (8 / 16 bytes)
- MemoryStick™ / MemoryStick Pro interface
  - Compliant with MemoryStick interface specification
  - Support INS signal
  - Support automatic CRC16 generation and verification
- Secure Digital™ and MultiMediaCard™
  - Compliant with Secure Digital / MMC interface specification
  - Supports both SD / MMC mode access CLK/CMD/DAT0/DAT1/DAT2/DAT3/DAT4/DAT5/DAT6/DAT7
  - Supports SD specification v1.0 / v1.1
  - Supports MMC specification v4.0 / v4.1 x1 / x4 / x8 data transmission
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- High efficient hardware engine
  - Automatic data read / write with card by hardware engine
  - Easier firmware development
- On board 24Mhz Crystal driver circuit
- Available in 208-pin LQFP 24x24 mm package, support all card interface with external Flash/Serial Interface for MP3 Decoder/2Pins Serial Interface LCD panel/ATA(ATAPI)/SDRAM(Host Interface) (GL824)
- Available in 128-pin LQFP 14x14 mm package, Support SD/MMC/MS/MSPro card interface/Serial Interface for MP3 Dcecoder (Only support Serial Data/Control interface in the same pins)/ATA(ATAPI)/SDRAM(Host Interface) (GL824C)

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CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

Figure 3.1 - 208 Pin LQFP Pinout Diagram

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Figure 3.2 – 128 Pin LQFP Pinout Diagram

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3.2 Pin List

Table 3.1 -GL824 208 Pin LQFP Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	GPIO5(ISP)	B	53	RVSS	P	105	INTRQ	I	157	NC	-
2	GPIO6	B	54	PGND	P	106	DD11	B	158	SM_ALE	O
3	GPIO7	B	55	X2	O	107	C_IOWZ	O	159	WE_/WE_	O/I
4	BSYNC	B	56	X1	I	108	DD4	B	160	SM_REZ	O
5	DREQ	B	57	PVCC	P	109	CF_IORZ	O	161	DQ8	B
6	DCLK	O	58	PIO1	B	110	DD10	B	162	SM_WEZ	O
7	SDATA	B	59	PIO2	B	111	CF_CS1Z	O	163	DQ7	B
8	SSICLK	B	60	PIO3	B	112	DD5	B	164	SM_RBZ	B
9	SSIDI	B	61	PIO4	B	113	CF_CS0Z	O	165	DQ9	B
10	SSIDO	B	62	TEST	I	114	DD9	B	166	SM_WPZ	B
11	CVCC	P	63	EXTRST_	I	115	CFSM_D15	B	167	DQ6	B
12	CGND	P	64	CF_CDZ	B	116	DD6	B	168	SM_D0	B
13	PGND	P	65	CS0_	O	117	CFSM_D7	B	169	DQ10	B
14	PVCC	P	66	CFSM_D10	B	118	DD8	B	170	SM_D1	B
15	SD_CDZ	B	67	DA0	O	119	CFSM_D14	B	171	DQ5	B
16	SD_WPZ	B	68	CFSM_D9	B	120	DD7	B	172	SM_D7	B
17	SD_D1	B	69	DA2	O	121	CFSM_D6	B	173	DQ11	B
18	SD_D0	B	70	CFSM_D2	B	122	ARESET_	B	174	SM_D2	B
19	SD_CLK	O	71	DA1	O	123	CFSM_D13	B	175	DQ4	B
20	SD_CMD	B	72	PMOSI1	I	124	CFSM_D5	B	176	SM_D6	B
21	SD_D3	B	73	PMOSO1	O	125	CVCC	P	177	DQ12	B
22	SD_D2	B	74	PMOSI2	I	126	CGND	P	178	SM_D3	B
23	GPIO1/ MMC_D4	B	75	PMOSO2	O	127	PGND	P	179	DQ3	B
24	GPIO2/ MMC_D5	B	76	PVCC	P	128	PVCC	P	180	SM_D5	B
25	GPIO3/ MMC_D6	B	77	PGND	P	129	SA3	O	181	DQ13	B
26	GPIO4/ MMC_D7	B	78	CGND	P	130	SA4	O	182	SM_D4	B
27	MS_BS	O	79	CVCC	P	131	SA2	O	183	DQ2	B
28	MS_D1	B	80	AINTRQ	I	132	SA5	O	184	DQ14	B
29	MS_D0	B	81	DMACK_	O	133	SA1	O	185	DQ1	B
30	MS_D2	B	82	AIORDY	I	134	SA6	O	186	DQ15	B
31	MS_INS	B	83	DIOR_	O	135	SA7	O	187	DQ0	B
32	MS_D3	B	84	DIOW_	O	136	SA0/A0	O/I	188	CVCC	P
33	MS_CLK	O	85	DMARQ	I	137	SA10	O	189	CGND	P
34	DRVVBUS	O	86	CS1_	O	138	SA8	O	190	PGND	P
35	VDD	P	87	CFSM_D8	B	139	BA1/RSTS	O	191	PVCC	P
36	ID	I	88	DD15	B	140	SA9	O	192	PMOSI3	I

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37	VSS	P	89	CFSM_D1	B	141	CFSM_D12	B	193	PMOSO3	O
38	AVSSA	P	90	DD0	B	142	BA0/WSTS	O	194	PMOSI4	I
39	VBUS	I	91	CFSM_D0	B	143	CFSM_D4	B	195	PMOSO4	O
40	RREF	B	92	DD14	B	144	SA11	O	196	RXD	B
41	AGND	P	93	CF_A0	O	145	CFSM_D11	B	197	TXD	O
42	AVDD	P	94	DD1	B	146	SA12	O	198	PIO5	B
43	DVDD	P	95	CF_A1	O	147	CFSM_D3	B	199	PIO6	B
44	DGND	P	96	DD13	B	148	CKE	O	200	PIO7	B
45	GNDS	P	97	CF_A2	O	149	SM_CDZ	B	201	PIO8	B
46	AGND1	P	98	DD2	B	150	RAS_/RE_	O/I	202	I2CK	O
47	AGND1	P	99	IORDY	I	151	SM_WPDZ	B	203	I2CD	B
48	DP	A	100	DD12	B	152	CKO	O	204	GPIO8	B
49	DM	A	101	CF_RST	B	153	SM_CLE	O	205	VSSA	P
50	AVDD	P	102	DD3	B	154	CAS_/CS_	O/I	206	VSEL	I
51	RVO	O	103	NC	-	155	XD_CDZ	B	207	VBAT	I
52	RVDD	I	104	NC	-	156	DQM	O	208	VDDA	P

Table 3.2 – GL824C 128-Pin LQFP Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DCLK	O	33	RVO	O	65	DD11	B	97	WE	O/I
2	SDATA	B	34	RVDD	I	66	DD4	B	98	DQ8	B
3	SSIDI	B	35	RVSS	P	67	DD10	B	99	DQ7	B
4	CVCC	P	36	X2	O	68	DD5	B	100	DQ9	B
5	CGND	P	37	X1	I	69	DD9	B	101	DQ6	B
6	PVCC	P	38	PVCC	P	70	DD6	B	102	DQ10	B
7	SD_D1	B	39	PIO1	B	71	DD8	B	103	DQ5	B
8	SD_D0	B	40	PIO2	B	72	DD7	B	104	DQ11	B
9	SD_CLK	O	41	TEST	I	73	ARESET_	O	105	DQ4	B
10	SD_CMD	B	42	EXTRST_	I	74	CVCC	P	106	DQ12	B
11	SD_D3	B	43	CS0	O	75	CGND	P	107	DQ3	B
12	SD_D2	B	44	DA0	O	76	PVCC	P	108	DQ13	B
13	MS_BS	O	45	DA2	O	77	SA3	O	109	DQ2	B
14	MS_D1	B	46	DA1	O	78	SA4	O	110	DQ14	B
15	MS_D0	B	47	PVCC	P	79	SA2	O	111	DQ1	B
16	MS_D2	B	48	PGND	P	80	SA5	O	112	DQ15	B
17	MS_INS	B	49	CVCC	P	81	SA1	O	113	DQ0	B
18	MS_D3	B	50	AINTRQ	I	82	SA6	O	114	CVCC	P
19	MS_CLK	O	51	DMACK_	O	83	SA7	O	115	CGND	P
20	DRVVBUS	O	52	AIORDY	I	84	SA0/A0	O/I	116	PVCC	P
21	VDD	P	53	DIOR_	O	85	SA10	O	117	RXD	B

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22	ID	I	54	DIOW_	O	86	SA8	O	118	TXD	O
23	VSS	P	55	DMARQ	I	87	BA1/RSTS	O	119	PIO5	B
24	VBUS	I	56	CS1	O	88	SA9	O	120	I2CK	O
25	RREF	B	57	DD15	B	89	BA0/WSTS	O	121	I2CD	B
26	AGND3	P	58	DD0	B	90	SA11	O	122	GPIO8	B
27	AVDD3	P	59	DD14	B	91	SA12	O	123	VSSA	P
28	DGND1	P	60	DD1	B	92	CKE	O	124	VSEL	I
29	AGND1	P	61	DD13	B	93	RAS_/RE_	O/I	125	VBAT	I
30	DP	B	62	DD2	B	94	CKO	O	126	VDDA	P
31	DM	B	63	DD12	B	95	CAS_/CS_	O/I	127	BSYNC	B
32	AVDD1	P	64	DD3	B	96	DQM	O	128	DREQ	B

3.3 Pin Descriptions

Table 3.3 – GL824 208 Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
GPIO5(ISP)	1	B (pu)	General Purpose I/O 5 (In System Programming)
GPIO6	2	B (pu)	General Purpose I/O 6
GPIO7	3	B (pu)	General Purpose I/O 7
BYYNC	4	B (pd)	Byte synchronization signal (for MP3 decoder I/F)
DREQ	5	B (pd)	Data request input (for MP3 decoder I/F)
DCLK	6	O (pd)	Serial output data bus clock (for MP3 decoder I/F)
SDATA	7	B (pd)	Serial output data (for MP3 decoder I/F)
SSICLK	8	B (pd)	Synchronous Serial Clock Output
SSIDI	9	B (pd)	Synchronous Serial data input
SSIDO	10	B (pd)	Synchronous Serial data output
DRVVBUS	34	O	Drive VBUS on control output pin
ID	36	I	ID
VBUS	39	I	VBUS
RREF	40	B	Reference resistor
DP	48	B	USB D+
DM	49	B	USB D-
PIO1~8	58~61, 198~201	B (pd)	Programmable I/O #1~#8
Test	62	I (pd)	Test pin

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EXTRST_	63	I (pd)	External reset
RXD	196	B (pu)	UART receives data input
TXD	197	O (pu)	UART transmits data output
I2CK	202	O (pu)	I^2C bus clock
I2CD	203	B (pu)	I^2C data
VSEL	206	I	Key voltage detection input
VBAT	207	I	Battery voltage detection input

ATA/ATAPI Interface			
Pin Name	**Pin#**	**Type**	**Description**
CS0_	65	O	PESETZ (PCVS2Z)
CS1_	86	O	PESETZ (PCVS1Z)
DA0~2	67,71,69	O	Address 0~2
AINTRQ	80	I (pd)	IREQZ
DMACK_	81	O	DMACK
AIORDY	82	I (pu)	IORDY (WAITZ)
DIOR_	83	O	I/O read strobe
DIOW_	84	O	I/O write strobe
DMARQ	85	I (pd)	DMARQ
DD0~15	90,94,98,102, 108,112,116, 120,118,114, 110,106,100, 96,92,88	B (pd)	Data 0~15
ARESET_	122	O	ARESET

SDRAM/Host Interface			
Pin Name	**Pin#**	**Type**	**Description**
SA1~12	133,131,129, 130,132,134, 135,138,140, 137,144,146	O	SDRAM_A1~A12
SA0/A0	136	O/I (pd)	SDRAM_A0 / share pin with A0 pin of HOST interface
BA0/WSTS	142		SDRAM_BA0 / share pin with write status pin of HOST interface
BA1/RSTS	139	O	SDRAM_BA1 / share pin with read status pin of HOST interface
CKE	148	O	SDRAM_CKE
RAS_/RE_	150	O/I (pu)	SDRAM_RAS / share pin with read enable pin of HOST interface

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CKO	152	O	Clock
CAS_/CS_	154	O/I (pu)	SDRAM_CAS / Share pin with chip select pin of HOST interface
DQM	156	O	SDRAM_UDQM
WE_/WE_	159	O/I (pu)	Write enable / Share pin with write enable pin of HOST interface
DQ0~15	187,185,183, 179,175,171, 167,163,161, 165,169,173, 177,181,184, 186	B (pd)	SDRAM_D0~D15 / Share pin with Data0~15 bus of HOST interface

CompactFlash / MicroDrive Interface			
Pin Name	**Pin#**	**Type**	**Description**
CF_CDZ	64	B (pu)	Card detection
CFSM_D0~15	91,89,70,147, 143,124,121, 117,87,68, 66,145,141, 123,119,115	B (pd)	Data bus 0~15
CF_A0~2	93,95,97	O	Address 0~2
IORDY	99	I (pu)	I/O read stobe
CF_RST	101	B (pd)	Reset
INTRQ	105	I (pd)	INTRQ
CF_IOWZ	107	O	I/O write strobe
CF_IORZ	109	O	I/O read strobe
CF_CS1Z	111	O	CS1Z
CF_CS0Z	113	O	CS0Z

SmartMeia / xD-Picture Card / NAND Flash Memory Interface			
Pin Name	**Pin#**	**Type**	**Description**
SM_CDZ	149	B (pu)	Card detection
SM_WPDZ	151	B (pu)	Write Protect Detect
SM_CLE	153	O	Command latch enable
XD_CDZ	155	B (pu)	Card detection
SM_ALE	158	O	Address latch enable
SM_REZ	160	O	Read enable
SM_WEZ	162	O	Write enable
SM_RBZ	164	B (pu)	Read/Busy

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SM_WPZ	166	B (pu)	Write Protect Detect
SM_D0~7	168,170,174, 178,182,180, 176,172	B (pd)	Address 0~7

SecureDigital / MultiMediaCard Interface			
Pin Name	**Pin#**	**Type**	**Description**
SD_CDZ	15	B (pu)	Card detection#
SD_WPZ	16	B (pu)	Write Protect Detection
SD_D0~3 MMC_D4~7	18,17,22,21, 23~26	B (pu)	Data 0~7
SD_CLK	19	O	SD/MMC clock
SD_CMD	20	B (pu)	SD/MMC command and response

Memory Stick Pro / Memory Stick Interface			
Pin Name	**Pin#**	**Type**	**Description**
MS_BS	27	O	Bus state
MS_D0~3	29,28,30,32	B (pd)	Data 0~3
MS_INS	31	B (pu)	Card detection
MS_CLK	33	O	Clock

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
GPIO1~8	23~26,1~3, 204	B (pu)	General Purpose I/O #1~#8
NC	103,104,157	-	No connection

Power / Ground			
Pin Name	**Pin#**	**Type**	**Description**
CVCC	11,79,125, 188	P	Core power 2.5V
CGND	12,78,126, 189	P	Core Ground
PGND	13,77,127, 190	P	Pad ground
PVCC	14,76,128, 191	P	Pad power 3.3V
VDD	35	P	Digital circuit power 2.5V
VSS	37	P	Digital circuit ground
AVSSA	38	P	AVSSA
AGND	41	P	Analog ground #3

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AVDD	42	P	Analog power#3
DVDD	43	P	Digital power #1
DGND	44	P	Digital ground #1
GNDS	45	P	Ground
AGND	46	P	Analog ground #1
AGND	47	P	Analog ground #1
AVDD	50	P	Analog power
RVO	51	P	2.5V regulator output
RVDD	52	P	2.5V regulator power
RVSS	53	P	2.5V regulator ground
PGND	54	P	24MHz crystal ground
X2	55	P	24MHz crystal output
X1	56	P	24MHz crystal input
PVCC	57	P	24MHz crystal power 3.3V
PMOSI1~4	72,74,192, 194	I	PMOS #1~#4 input 3.3V
PMOSO1~4	73,75,,193, 195	O	PMOS #1~#4 output 3.3V
VSSA	205	P	ADC ground
VDDA	208	P	ADC 3.3V power

Table 3.4 – GL824C 128 Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
BYYNC	127	B (pd)	Byte synchronization signal (for MP3 decoder I/F)
DREQ	128	B (pd)	Data request input (for MP3 decoder I/F)
DCLK	1	O (pd)	Serial output data bus clock (for MP3 decoder I/F)
SDATA	2	B (pd)	Serial output data (for MP3 decoder I/F)
SSIDI	3	B (pd)	Synchronous Serial data input
DRVVBUS	20	O	Drive VBUS on control output pin
ID	22	I	ID
VBUS	24	I	VBUS
RREF	25	B	Reference resistor
DP	30	B	USB D+
DM	31	B	USB D-
PIO1	39	B (pd)	Programmable I/O #1
Test	41	I (pd)	Test pin

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EXTRST_	42	I (pd)	External reset
RXD	117	B (pu)	UART receives data input
TXD	118	O (pu)	UART transmits data output
I2CK	120	O (pu)	I^2C bus clock
I2CD	121	B (pu)	I^2C data
VSEL	124	I	Key voltage detection input
VBAT	125	I	Battery voltage detection input

ATA/ATAPI Interface			
Pin Name	**Pin#**	**Type**	**Description**
CS0_	43	O	PESETZ (PCVS2Z)
CS1_	56	O	PESETZ (PCVS1Z)
DA0~2	44,46,45	O	Address 0~2
AINTRQ	50	I (pd)	IREQZ
DMACK_	51	O	DMACK
AIORDY	52	I (pu)	IORDY (WAITZ)
DIOR_	53	O	I/O read strobe
DIOW_	54	O	I/O write strobe
DMARQ	55	I (pd)	DMARQ
DD0~15	58,60,62,64, 66,68,70, 72,71,69, 67,65,63, 61,59,57	B (pd)	Data 0~15
ARESET_	73	O	ARESET

SDRAM Interface			
Pin Name	**Pin#**	**Type**	**Description**
SA1~12	81,79,77, 78,80,82, 83,86,88, 85,90,91	O	SDRAM_A1~A12
SA0/A0	84	O/I (pd)	SDRAM_A0 / share pin with A0 pin of HOST interface
BA0/WSTS	89		SDRAM_BA0 / share pin with write status pin of HOST interface
BA1/RSTS	87	O	SDRAM_BA1 / share pin with read status pin of HOST interface
CKE	92	O	SDRAM_CKE
RAS_/RE_	93	O/I (pu)	SDRAM_RAS / share pin with read enable pin of HOST interface

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CKO	94	O	Clock
CAS_/CS_	95	O/I (pu)	SDRAM_CAS / Share pin with chip select pin of HOST interface
DQM	96	O	SDRAM_UDQM
WE_/WE_	97	O/I (pu)	Write enable / Share pin with write enable pin of HOST interface
DQ0~15	113,111,109, 107,105,103, 101,99,98, 100,102,104, 106,108,110, 112	B (pd)	SDRAM_D0~D15 / Share pin with Data0~15 bus of HOST interface

SecureDigital / MultiMediaCard Interface			
Pin Name	**Pin#**	**Type**	**Description**
SD_CDZ	119	B (pu)	Card detection#
SD_WPZ	40	B (pu)	Write Protect Detection
SD_D0~3	8,7,12,11,	B (pu)	Data 0~3
SD_CLK	9	O	SD/MMC clock
SD_CMD	10	B (pu)	SD/MMC command and response

Memory Stick Pro / Memory Stick Interface			
Pin Name	**Pin#**	**Type**	**Description**
MS_BS	13	O	Bus state
MS_D0~3	15,14,13,18	B (pd)	Data 0~3
MS_INS	17	B (pu)	Card detection
MS_CLK	19	O	Clock

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
GPIO8	122	B (pu)	General Purpose I/O #8

Power / Ground			
Pin Name	**Pin#**	**Type**	**Description**
CVCC	4,49,74, 114	P	Core power 2.5V
CGND	5,48,75, 115	P	Core Ground
PVCC	6,47,76, 116	P	Pad power 3.3V
VDD	21	P	Digital circuit power 2.5V

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VSS	23	P	Digital circuit ground
AGND	26	P	Analog ground #3
AVDD	27	P	Analog power#3
DGND	28	P	Digital ground #1
GNDS	29	P	Ground
AVDD	32	P	Analog power
RVO	33	P	2.5V regulator output
RVDD	34	P	2.5V regulator power
RVSS	35	P	2.5V regulator ground
X2	36	P	24MHz crystal output
X1	37	P	24MHz crystal input
PVCC	38	P	24MHz crystal power 3.3V
VSSA	123	P	ADC ground
VDDA	126	P	ADC 3.3V power

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

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CHAPTER 4 BLOCK DIAGRAM

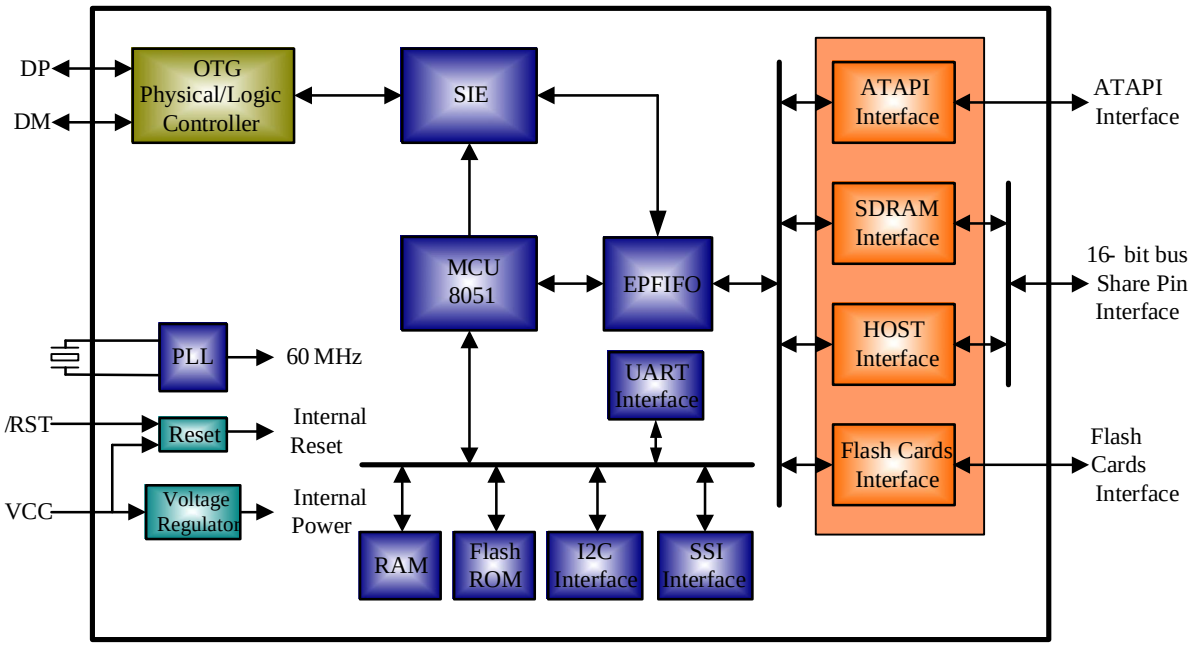

Figure 4.1 - GL824 Block Diagram

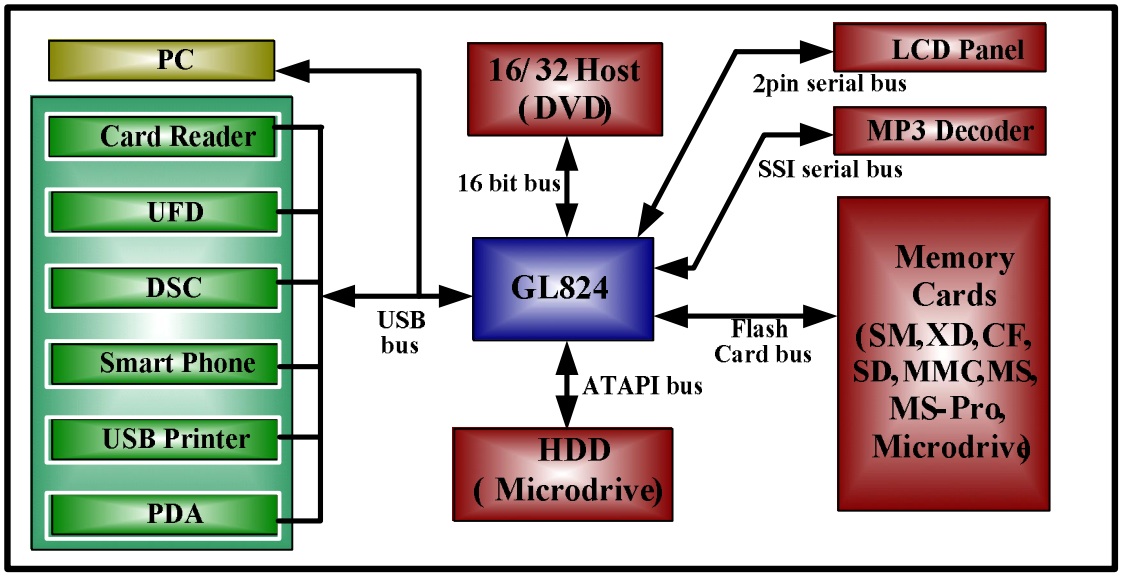

Figure 4.2 - GL824 System Block Diagram

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CHAPTER 5 FUNCTION DESCRIPTION

5.1 OTG (On-The-Go)

A dual-role OTG device that has the following features and characteristics:

- Liminted Hos capability
- High/Full-speed operation as peripheral
- High/Full-speed support as host
- Targeted Peripheral List
- Session Request Protocol
- Host Negotiation Protocol
- One Mini-AB receptacle
- Minimum 8mA output on VBUS

5.2 SIE (Serial Interface Engine)

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to habdle USB packets and transactions.

5.3 EPFIFO (Endpoint FIFO)

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3) and Bulk In/Out FIFO (BULKFIFO).

- Control FIFO — FIFO of control endpoint 0.
  It is 64-bytes FIFO, and it is used for endpoint 0 data transfer.
- Interrupt FIFO — 64-bytes depth FIFO of endpoint 3 for status interrupt.
- Bulk In/Out FIFO — It can be in the TX mode or RX mode:
  a. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  b. It can be directly accessed by Uc.
  c. Support automatic hardware SmartMedia ECC error correction.

5.4 SSI (Synchronous Serial Interface)

The Synchronous Serial Interface provides serial data in and out for communication with serial fingerprint sensor The SSI uses following pins: SSICLK, SSIDO and SSIDI.

SSICLK: Synchronous Serial Interface Clock
SSIDO: Synchronous Serial Interface Data Output
SSIDI: Synchronous Serial Interface Data Input

5.4.1 One Byte Receive/Transmit Mode

GL824 provides a programmable synchronous serial interface. The SSI not only supports both clock normal and clock opposite phases but also supports MSB or LSB data formats. One Byte Receive/Transmit timing diagram see **Figure 5.1** ~ **Figure 5.2**. User can read/write register/command from/to fingerprint sensor in this mode.

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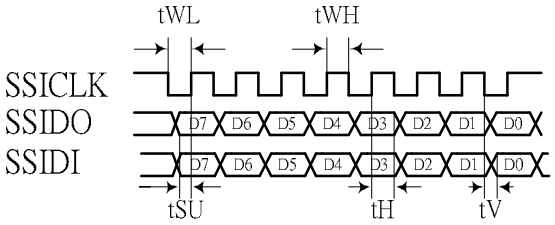

Figure 5.1 - One Byte Receive/Transmit Timing Diagram (Clock Opposite)

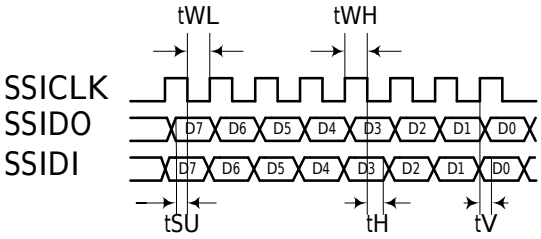

Figure 5.2 - One Byte Receive/Transmit timing diagram (clock normal)

5.4.2 Continues Receive/Transmit Data Mode

For fingerprint sensor application, GL824 gets image row/column data by continues receive mode. **Figure 5.3** shows the data receive timing diagram. The SSICLK clock rate can be configured by DIV register.

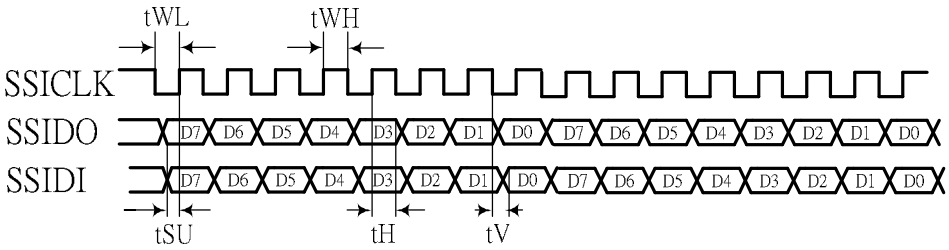

Figure 5.3 - Continues Receive/Transmit Data timing diagram (clock opposite)

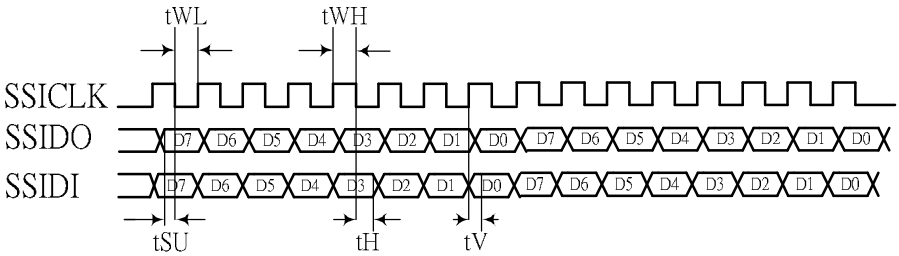

Figure 5.4 - Continues Receive/Transmit Data timing diagram (clock normal)

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Table 5.1 - AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
tWL	Clock Low Time	35	-	ns
tWH	Clock High Time	35	-	ns
tSU	Data Setup Time	1/2 * tWL	-	ns
tH	Data Hold Time	3/4 * tWL	-	ns
tV	Data Valid Time	1/4 * tWL	-	ns

5.5 UART (Universal Asynchronous Receiver/Transmitter)

GL824 has three 16-bit timers/counters that are same as the timer of the standard 8052 family up to 921.6Kbps. The serial port has three asynchronous modes of operation. For fingerprint sensor application, the data frame consists of 10 bits: one start bit, eight data bits and one stop bit. Serial data is transmitted on the TxD pin and received on the RxD pin. The data frame shows in **Figure 5.5**.

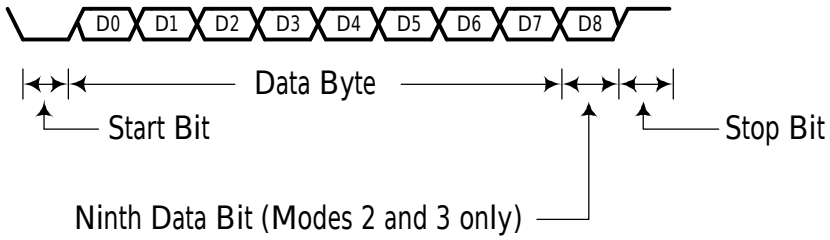

Figure 5.5 - Data Frame

5.6 Host Interface

- **Pin Description**

/CS: Chip Select and active low.

A0: Command/Status and Data select. When A0 is high, GL824 is operation at Command Write and Status Read mode. When A0 is low, GL824 is operation at continues data receive/transfer mode.

/RE: Read Enable; Active low. GL824 read frequency must lower than 30 MHz.

/WE: Write Enable; Active low. Write frequency must lower than 30 MHz.

Data[0:15]: 16 bit Data bus

WSTS: Command/Data Write Status. When WSTS is high, it indicated that GL824 is ready for HOST write command/data.

RSTS: Command/Data Read Status. When RSTS is high, it indicated that GL824 is ready for HOST read data/status.

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Command Write

Command, address and data are all written through Data[0:15] port by bring /WE to low, while A0 is high and WSTS also pull high, it indicated that GL824 is ready for HOST write command. When /CS is low, command is latched on the rising edge of /WE. When WSTS goes low it indicates that Command is latched into command register by GL824.

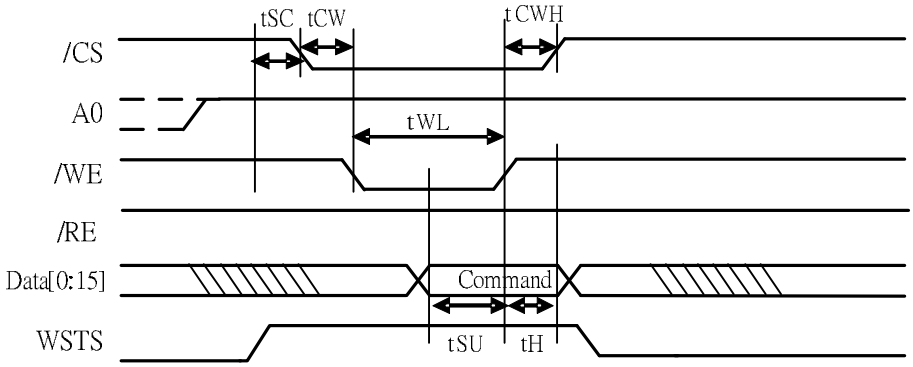

Figure 5.6 - Command Write Timing Diagram

Status Read

Register status, address and data can be read through Data[0:15] port by bring RE to low, while A0 is high and RSTS also return high, it indicated that GL824 is ready for HOST read status. When /CS is low. Register status latched on the rising edge of /RE. After status read operation is finished, RSTS is low.

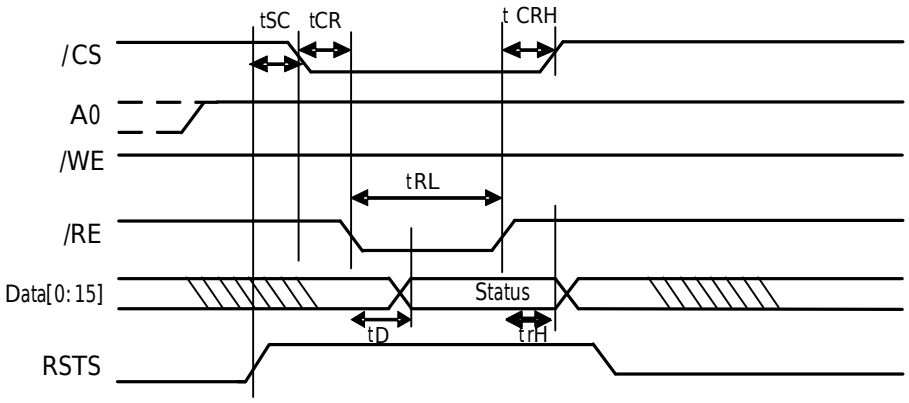

Figure 5.7 - Status Read Timing Diagram

Data Write

External HOST pull A0 low, while WSTS active high, it indicated that Data Buffer Memory is ready to be written by external microprocessor through Data[0:15] port. HOST continues write 256 words data by bring /CS is low. Data is latched on the rising edge of /WE. The GL824 Data Buffer Memory Address Pointer is increased automatically. After data continues write operation is finished and latched into Data Buffer Memory, WSTS will drive low. When GL824 Data Buffer Memory is ready for HOST write data, WSTS return to high.

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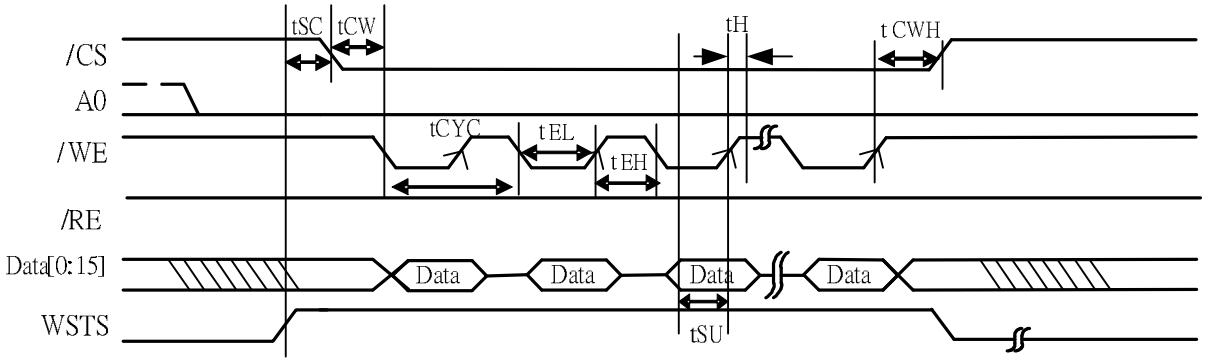

Figure 5.8 - Data Write Timing Diagram

Data Read

External HOST pull A0 low, while RSTS active high, it indicated that Data Buffer Memory is ready to be read by external microprocessor through Data[0:15] port. HOST continues read 256 words data by bring /CS is low. Data is latched on the rising edge of /RE. The GL824 Data Buffer Memory Address Pointer is increased automatically. After data continues read operation is finished, RSTS is low. When GL824 Data Buffer Memory is ready for HOST read data, RSTS return to high.

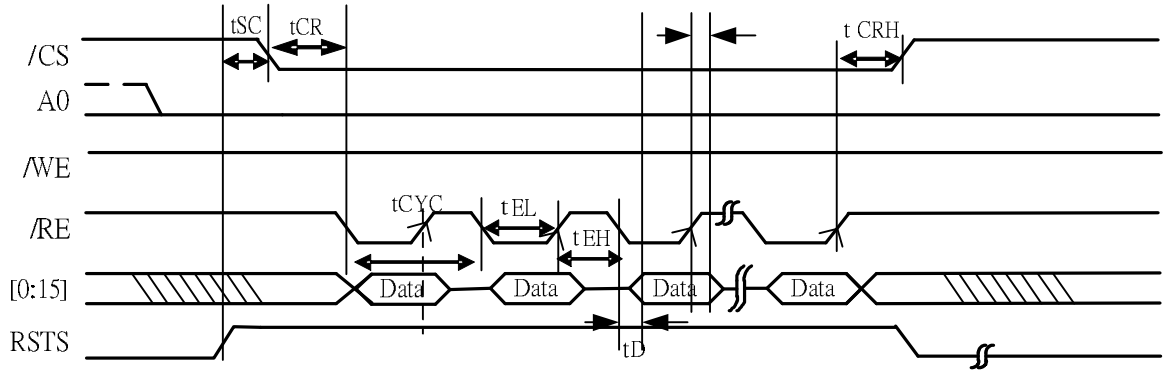

Figure 5.9 - Data Read Timing Diagram

Table 5.2 - Host Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
tCW	Chip Select Low to Write Enable Low delay time	5	-	ns
tCWH	Chip Select High for Write Enable High delay time	5	-	ns
tSC	A0 High to Write Enable Low delay time	5	-	ns
tWL	Write Enable Low time	20	-	ns
tSU	Data Setup Time for /WE signal	20	-	ns
tH	Data Hold Time for /WE signal	5	-	ns
tRL	Read Enable Low time	20	-	ns
tCYC	Write Enable clock cycle time	40	-	ns
tEH	Write Pulse High width	20	-	ns
tEL	Write pulse Low width	20	-	ns
tCR	Chip Select Low to Read Enable Low delay time	5	-	ns
tCRH	Chip Select High for Read Enable High delay time	5	-	ns
trH	Command/Data read hold time for enable signal	-	5	ns

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tD	Data ready for command/Data read	5	-	ns

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CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	24 MHz ± 0.25%

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	-	3.6	V
V_{IH}	Input High Voltage		2.6	-	5	V
V_{IL}	Input Low Voltage		0	-	0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-5	-	5	µA
V_{OH}	Output High Voltage		3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
I_{OH}	Output Current High	VDD=3.3V V_{OH}=2.6V	-	8	-	mA
I_{OL}	Output Current Low	VDD=3.3V V_{OL}=0.8V	-	8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	500	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	100	mA

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6.4 PMOS Characteristics

Table 6.4 – PMOS Characteristics

(Core Power=2.5V, IO Power=3.3V)

Simulation Results	TT (25°C)	SS (80°C)	FF (0°C)
Driving Strength	124.4	102.5	140.5
Turn-On Slew Rate (V/uS)	0.256	0.175	0.2560.321
On-Resistance (ohm)	1.61	1.95	1.611.42

Note:

1. Driving strength is defined as the PMOS sinking current when Vio=3.3V, Vd=3.1V.
2. Turn-on slew rate is defined as the falling speed of PMOS's gate voltage from 3.2V to 0.2V.
3. On-resistance is calculated by 0.2V divided by driving strength.

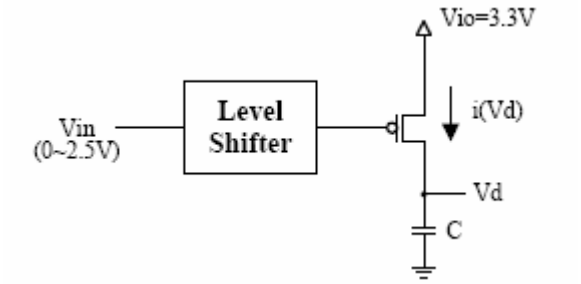

Figure 6.1 – Embedded PMOS Switch Architecture

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Output IV curve at typical corner vdd=2.5v, v3ring=3.3v, temp=25C

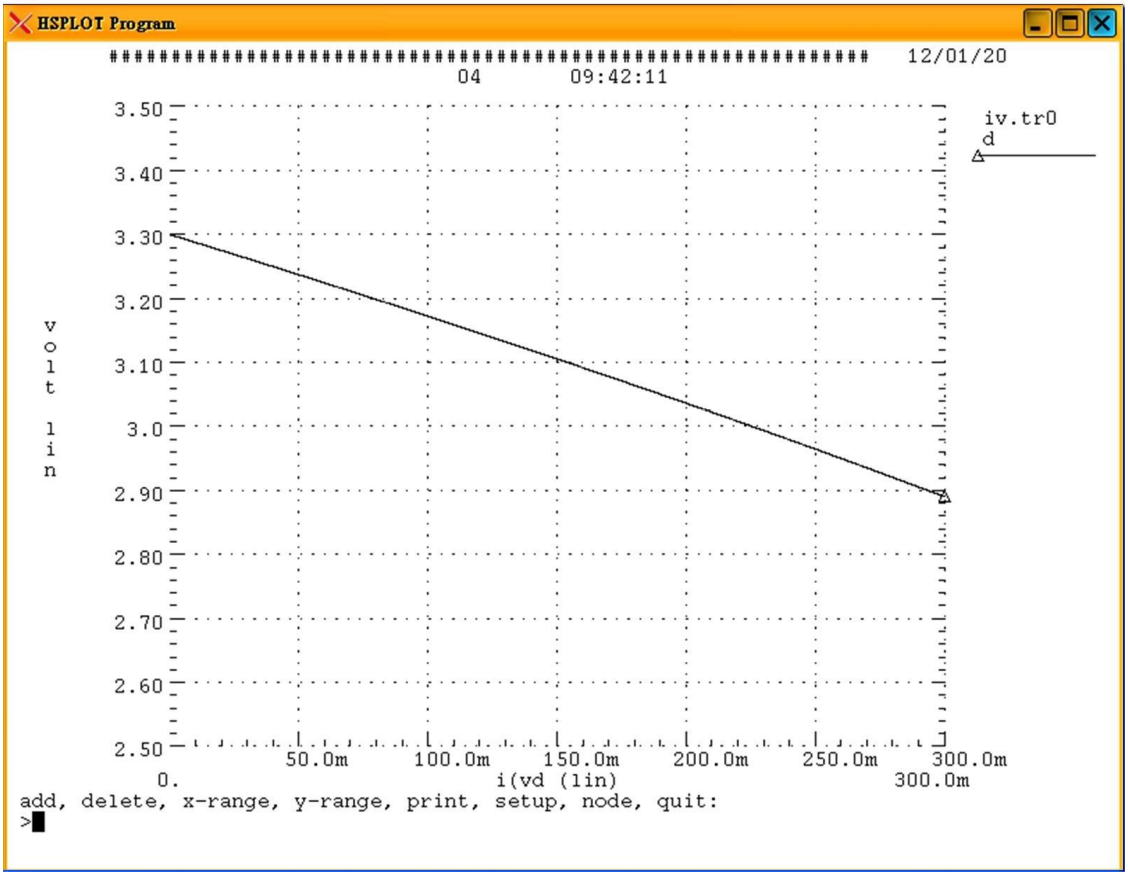

Figure 6.2 – I-V Curve of PMOS Swtich

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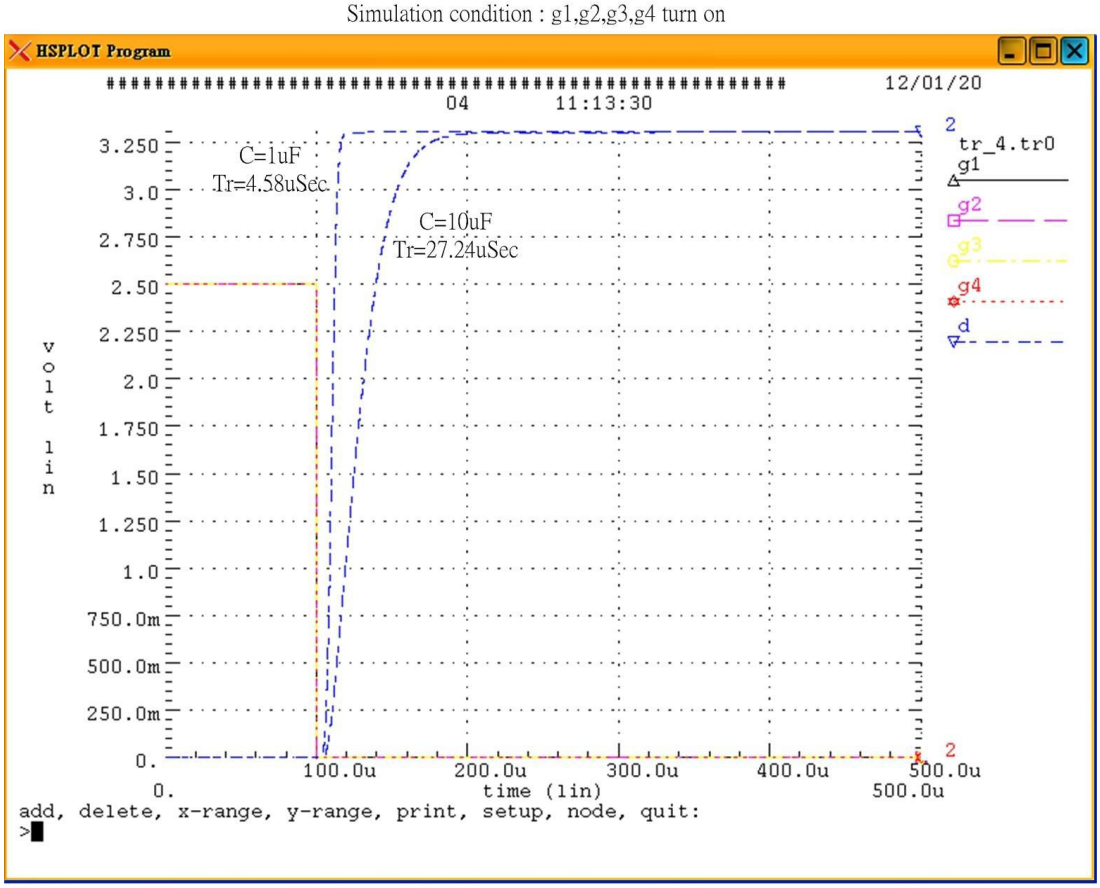

Tr is defined as v(d) rises from 20%*3.3v to 80%3.3v

Figure 6.3 – Transient Analysis of PMOS Switch

6.5 AC Characteristics

6.5.1 External Flash

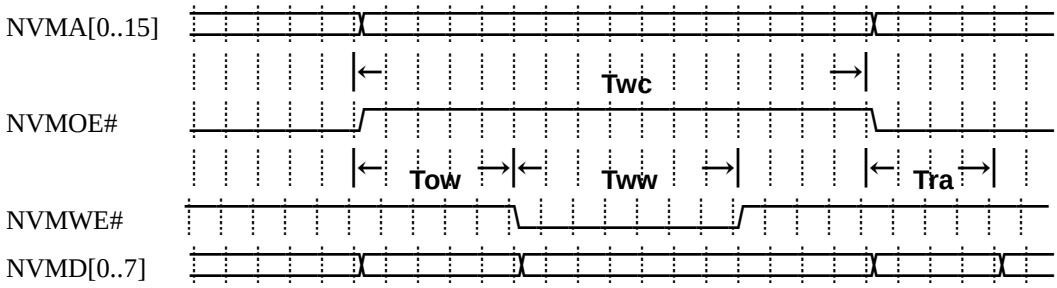

Figure 6.4 – Timing Diagram of External Flash

Parameter	Description	Min	Typ	Max	Unit
T_{WC}	Write data cycle time	-	102.5	-	ns
T_{WW}	Write pulse width	-	41.6	-	
T_{OW}	OE# to WE# time	-	38.6	-	
T_{RA}	Read Access time	-	-	90	

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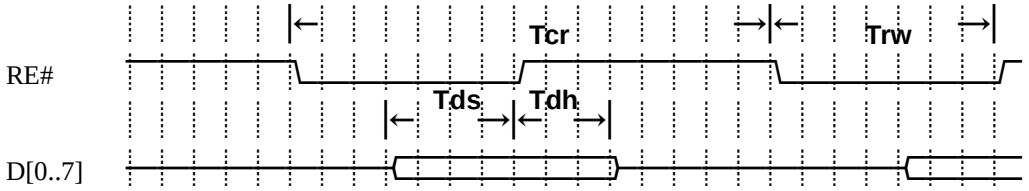
6.5.2 SmartMedia

Read



Write

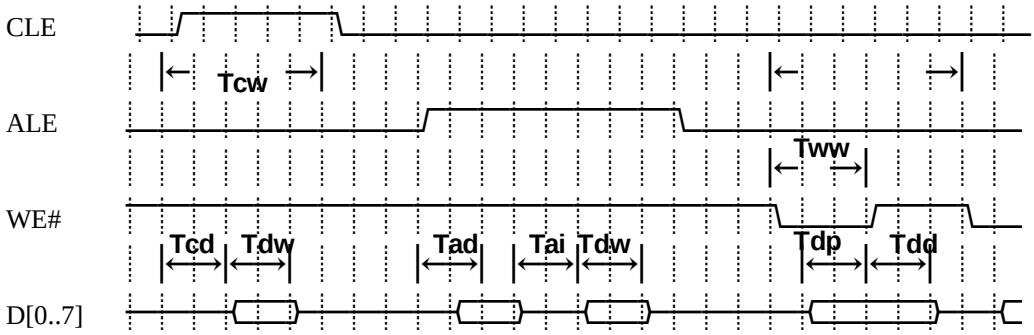


Figure 6.5 - Timing Diagram of SmartMedia

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcw	CLE active width	Normal	-	165	-	ns
		Slow	-	198	-	
Twc	Write data cycle time	Normal	-	100	-	
		Slow	-	166	-	
Tww	Write pulse width	Normal	-	66	-	
		Slow	-	100	-	
Tcd	CLE-to-command delay	-	-	33.3	-	
Tdw	Data width	Normal	-	67	-	
		Slow	-	100	-	
Tad	ALE-to-address delay	-	-	33.3	-	
Tai	Address data interval time	-	-	33.3	-	
Tdp	Data pre-output delay	-	-	33.3	-	
Tdd	Data delay time	-	-	33.3	-	
Tcr	Read data cycle time	Normal	-	133.3	-	
		Slow	-	166.6	-	
Trw	Read pulse width	-	-	100	-	
Tds	Data setup time	-	-	40	-	
Tdh	Data hold time	-	-	20	-	

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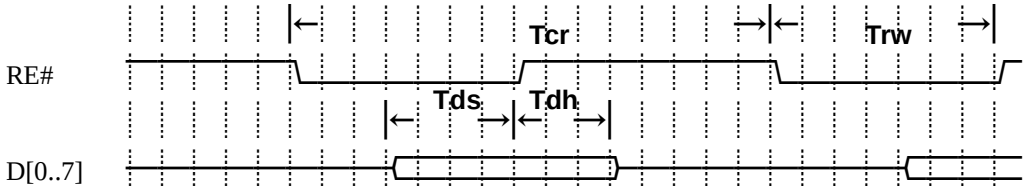
6.5.3 xD-Picture

Read



Write

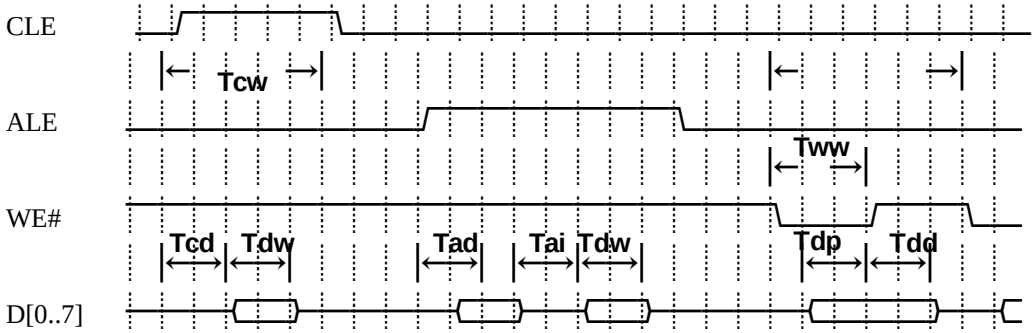


Figure 6.6 - Timing Diagram of xD-Picture

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcw	CLE active width	Normal		165		ns
		Slow		198		
Twc	Write data cycle time	Normal		100		
		Slow		166		
Tww	Write pulse width	Normal		66		
		Slow		100		
Tcd	CLE-to-command delay			33.3		
Tdw	Data width	Normal		67		
		Slow		100		
Tad	ALE-to-address delay			33.3		
Tai	Address data interval time			33.3		
Tdp	Data pre-output delay			33.3		
Tdd	Data delay time			33.3		
Tcr	Read data cycle time	Normal		133.3		
		Slow		166.6		
Trw	Read pulse width			100		
Tds	Data setup time			40		
Tdh	Data hold time			20		

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6.5.4 Memory Stick

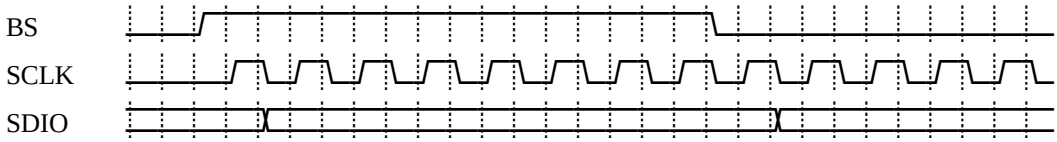

Figure 6.7 - Timing Diagram of MemoryStick

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	20M		

6.5.5 Memory Stick PRO

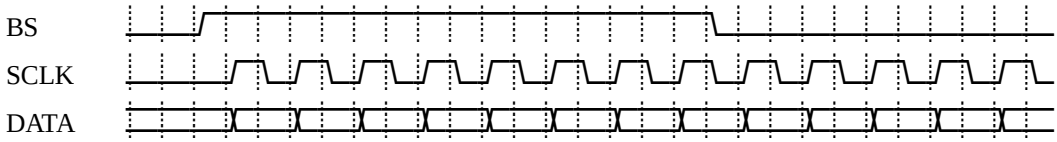

Figure 6.8 - Timing Diagram of MemoryStick PRO

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	30M	Hz	
		1	40M		

6.5.6 Secure Digital / MultiMedia Card

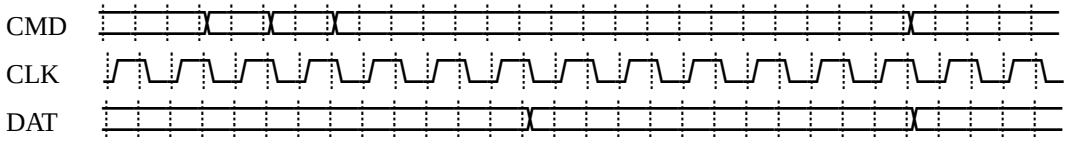

Figure 6.9 - Timing Diagram of SD / MMC

Parameter	Description	Mode	Typ	Unit	Remark
Fck	CLK frequency	0	375K	Hz	
		1	6M		
		2	15M		
		3	24M		
		4	48M		

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6.5.7 CompactFlash Card

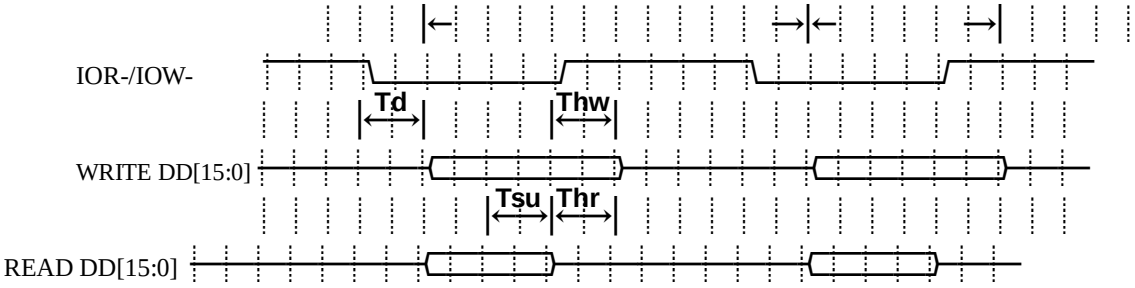

Figure 6.10 - Timing Diagram of CompactFlash

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcyc	Read/Write Cycle Time	0	600	-	-	ns
		1	383	-	-	
		2	240	-	-	
		3	180	-	-	
		4	120	-	-	
		5	100	-	-	
		6	80	-	-	
Tw	Read/Write Active Width	0	165	-	-	
		1	125	-	-	
		2	100	-	-	
		3	80	-	-	
		4	70	-	-	
		5	65	-	-	
		6	55	-	-	
Td	Delay Time for Write Data	0	0	-	-	
		1	0	-	-	
		2	0	-	-	
		3	0	-	-	
		4	0	-	-	
		5	0	-	-	
		6	0	-	-	
Thw	Data Hold Time following IOW-	0	30	-	-	
		1	20	-	-	
		2	15	-	-	
		3	10	-	-	
		4	10	-	-	
		5	5	-	-	
		6	5	-	-	
Tsu	Data Setup Time before IOR-	0	50	-	-	
		1	35	-	-	
		2	20	-	-	
		3	20	-	-	

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		4	20	-	-	
		5	15	-	-	
		6	10	-	-	
Thr	Data Hold Time following IOR-	0	5	-	-	
		1	5	-	-	
		2	5	-	-	
		3	5	-	-	
		4	5	-	-	
		5	5	-	-	
		6	5	-	-	

6.5.8 Reset Timing

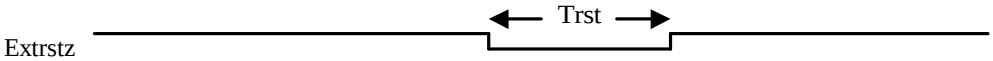

Figure 6.11 - Timing Diagram of Reset

Parameter	Description	Minimum	Unit	Remark
Trst	This active low signal is used by the system to reset the chip; the active low pulse should be at least 1us wide.	1	us	

6.5.9 ATA/ ATAPI

The GL824 complies with ATA / ATAPI-6 specification rev 1.0, which supports following data transfer modes:

1. DMA (Direct Memory Access) data transfer:
   DMA data transfer means of data transfer between device and host memory without host processor intervention.
   - Multiword DMA: Multiword DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When a Multiword DMA transfer is enabled as indicated by IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data, this data transfer protocol shall be used for the data transfers associated with these commends. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)
   - Ultra DMA: Ultra DMA Is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)

Following listed the symbols and their respective definitions that are used in the timing diagram:

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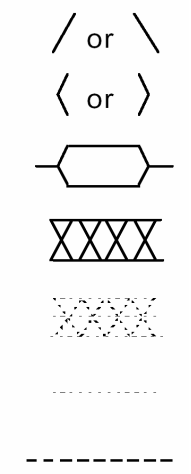
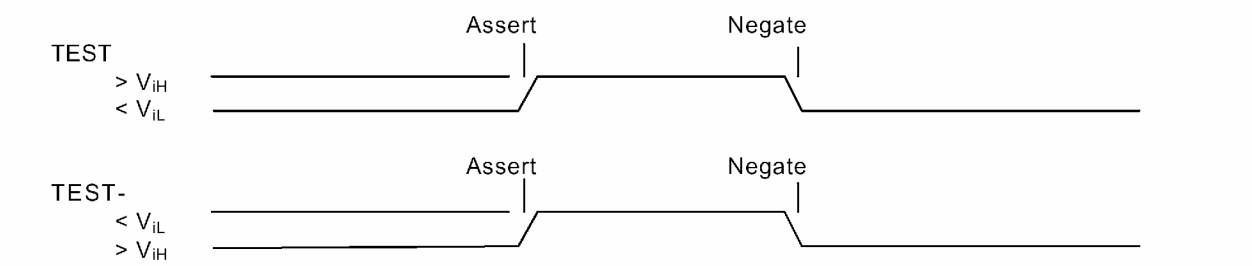


- Signal transition (asserted or negated)
- Data transition (asserted or negated)
- Data valid
- Undefined but not necessarily released
- Asserted, negated or released
- Released
- The “other” condition if a signal is shown with no change

All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named Test going from negated to asserted and back to negated, based on the polarity of the signal.



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6.5.10 Register Transfers

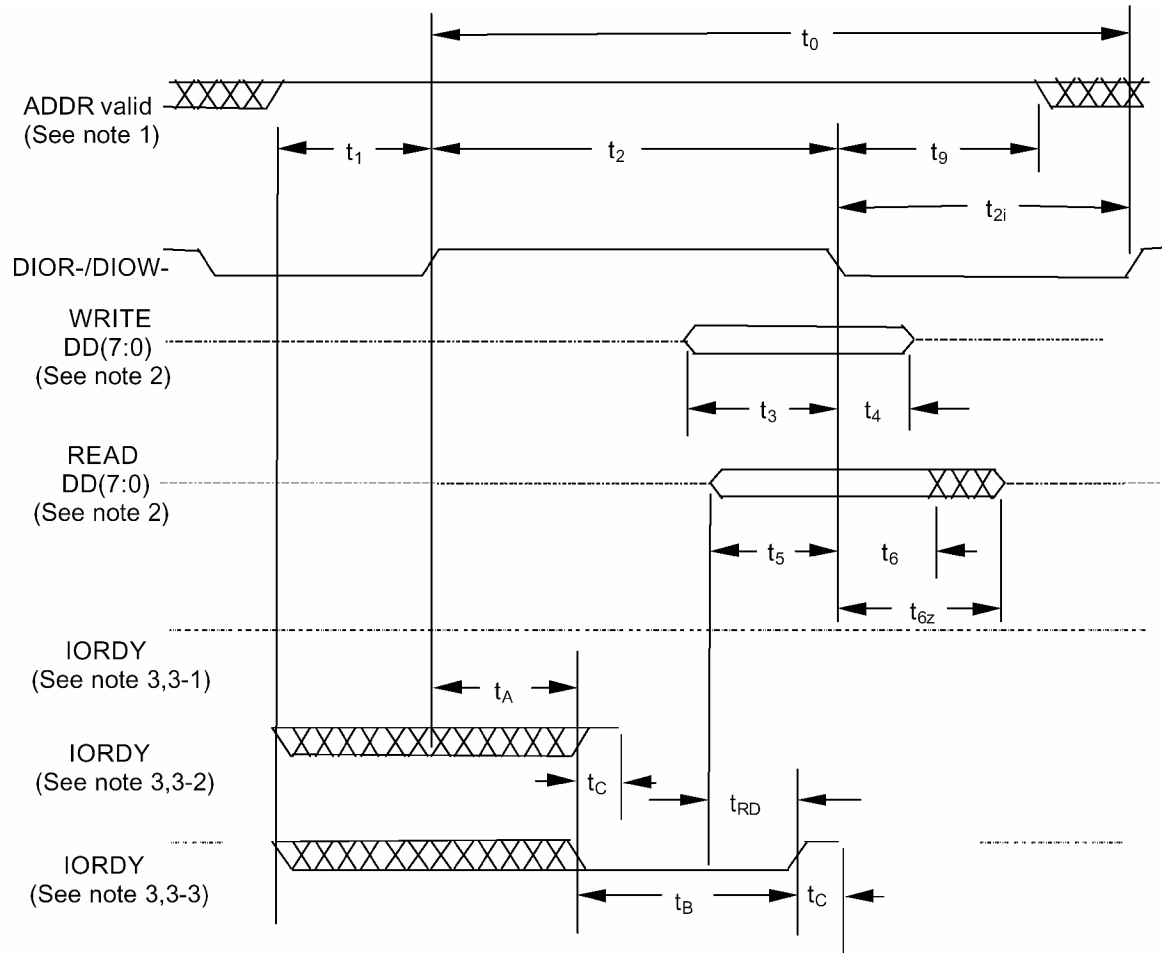

Figure 6.12 – Register Transfers Timing

Notes:

1. Device address consists of signals CS0_, CS1_ and DA(2:0).
2. Data consists of IODD(7:0).
3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR_ or DIOW_. The assertion and negation of IORDY are described as following:
   - 3.1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
   - 3.2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
   - 3.3 Device negates IORDY before t_A, IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is released. For cycles where a wait is generated and DIOR_ is asserted, the device shall read data on IODD(0:7) for t_{RD} before asserting IORDY.
4. DMACK_ shall remain negated during a register transfer.

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Register transfer timing parameters		Timing (ns)
t_0	Cycle time	2000
t_1	Address valid to DIOR_/ DIOW_ setup	1000
t_2	DIOR_/ DIOW_ pulse width 8-bit	300
t_{2i}	DIOR_/ DIOW_ recovery time	900
t_3	DIOW_ data setup	80
t_4	DIOW_ data hold	40
t_5	DIOR_ data setup	-
t_6	DIOR_ data hold	-
t_{6Z}	DIOR_ data tristate	-
t_9	DIOR_/ DIOW_ to address valid hold	900
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	
t_A	IORDY Setup time	-
t_B	IORDY Pulse Width	-
t_C	IORDY assertion to release (max)	-

6.5.11 Multiword DMA data transfer

Register transfer timing parameters		Timing (ns)
t_0	Cycle time	120
t_D	DIOR_/ DIOW_ asserted pulse width	80
t_E	DIOR_ data access	-
t_F	DIOR_ data hold	-
t_G	DIOR_/ DIOW_ data setup	40
t_H	DIOW_ data hold	18
t_I	DMACK to DIOR_/ DIOW_ setup	18
t_J	DIOR_/ DIOW_ to DMACK hold	20
t_{KR}	DIOR_ negated pulse width	36
t_{KW}	DIOW_ negated pulse width	36
t_{LR}	DIOR_ to DMARQ delay	-
t_{LW}	DIOW_ to DMARQ delay	-
t_M	CS(1:0) (max) valid to DIOR_/ DIOW_	36
t_N	CS(1:0) hold	18
t_Z	DMACK_ to read data released	-

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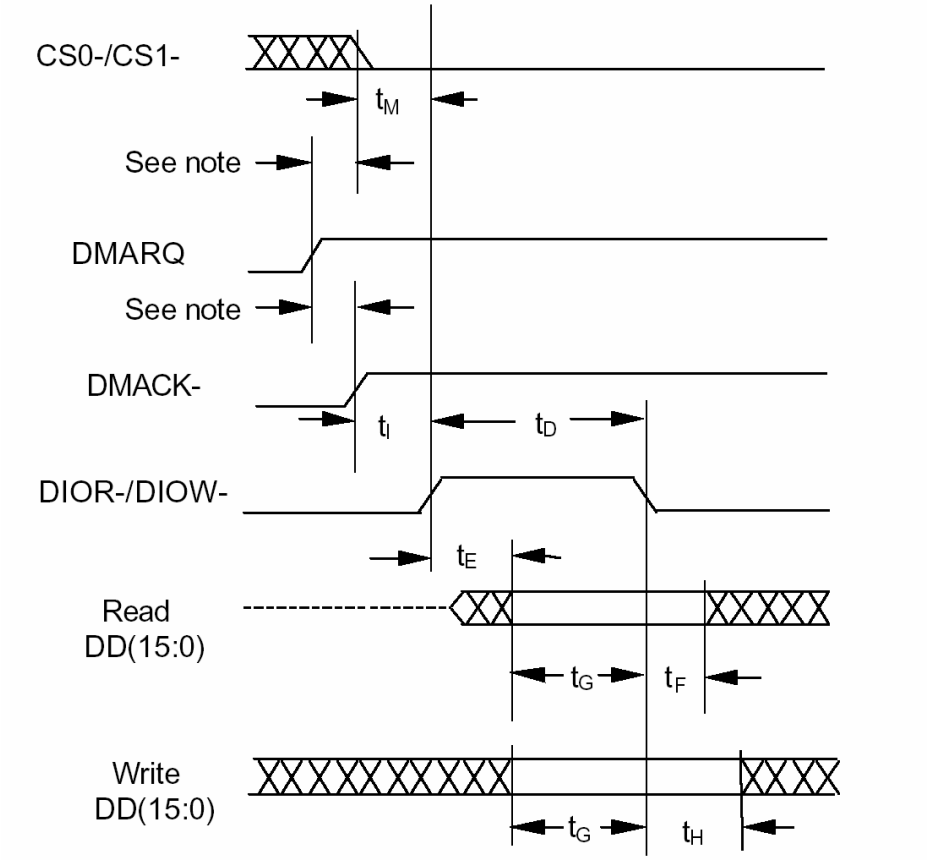

Note:
The host shall not assert DMACK_ or negate both CS0_ and CS1_ until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK_ or the negation of both CS0_ and CS1_ is not defined.

Figure 6.13 - Initiating a Multiword DMA Data Burst

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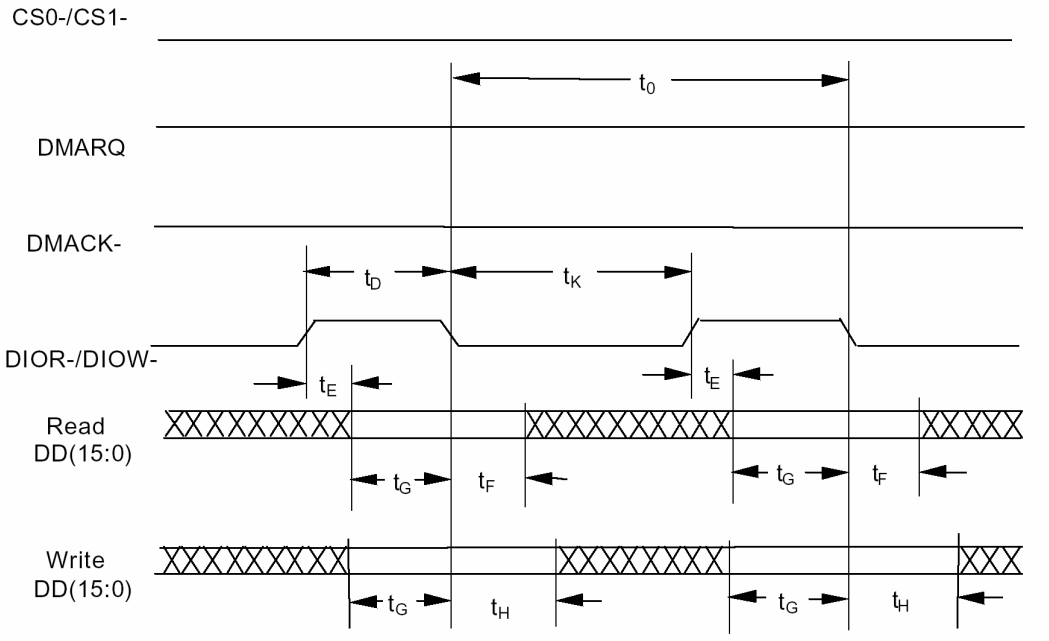
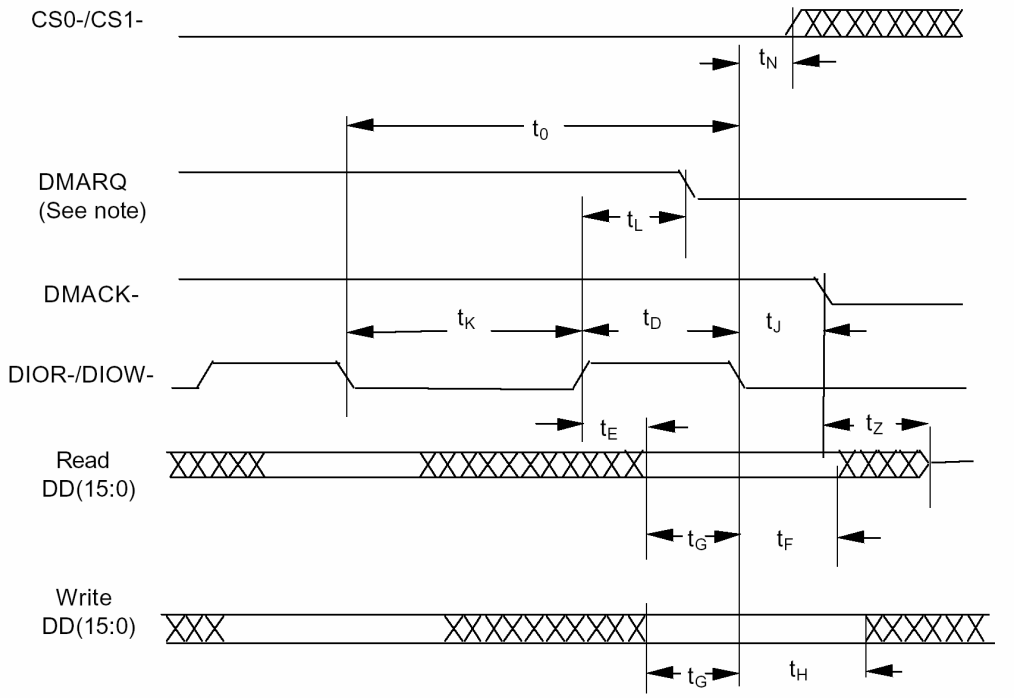


Figure 6.14 - Sustaining a Multiword DMA Data Burst



Note:
To terminate the data burst, the Device shall negate DMARQ within the t_L of the assertion of the current DIOR_ or DIOW_ pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR_ or DIOW_ pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation.

Figure 6.15 - Device Terminating a Multiword DMA Data Burst

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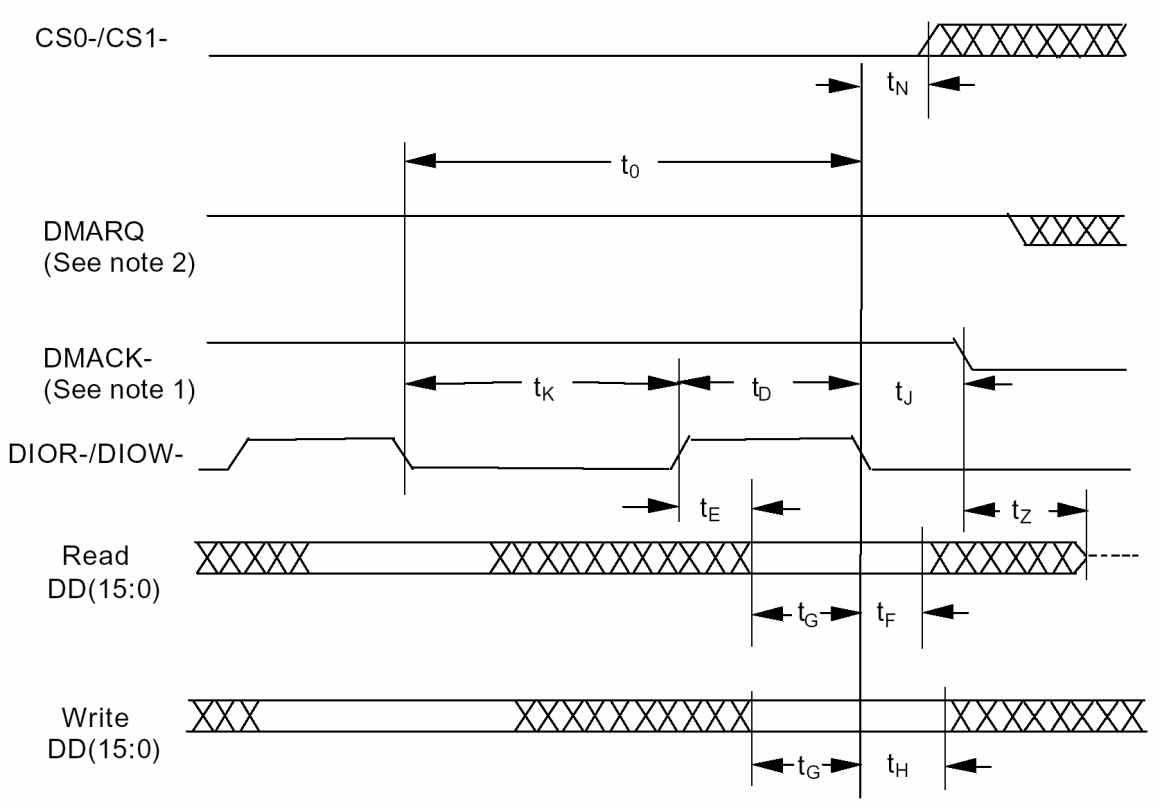

Note:

1. To terminate the transmission of a data burst, the Host shall negate DMACK_ within the specified time after a DIOR_ or DIOW_ pulse. No further DIOR_ or DIOW_ pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK_ or may negate DMARQ at any time after detecting that DMACK_ has been negated.

Figure 6.16 - Host terminating a Multiword DMA Data Burst

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6.5.12 Ultra DMA data transfer

Table 6.5 - Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Comment
	min	max	min	max	min	max	min	max	Min	max	
$t_{2CYCTYP}$	240		160		120		90		60		Typical sustained average two cycle time
t_{CYC}	112		73		54		39		25		Cycle time allowing for asymmetry and clock variations
t_{2CYC}	230		154		115		86		57		Two cycle time allowing for clock variations
t_{DS}	15		10		7		7		5		Data setup time at recipient
t_{DH}	5		5		5		5		5		Data hold time at recipient
t_{DVS}	70		48		30		20		6		Data valid setup time at sender
t_{DVH}	6		6		6		6		6		Data valid hold time at sender
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STORBE time
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited interlock time
t_{MLI}	20		20		20		20		20		Interlock time with minimum
t_{UI}	0		0		0		0		0		Unlimited interlock time
t_{AZ}		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{ZAH}	20		20		20		20		20		Minimum delay time required for output
t_{ZAD}	0		0		0		0		0		Drivers to assert or negate
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time
t_{SR}		50		30		20		NA		NA	STROBE to DMARDY_ time
t_{RFS}		75		70		60		60		60	Ready to final STROBE time
t_{RP}	160		125		100		100		100		Minimum time to assert STOP or negate DMARQ
t_{IORDYZ}		20		20		20		20		20	Maximum time before releasing IORDY
t_{ZIORDY}	0		0		0		0		0		Minimum time before driving STROBE
t_{ACK}	20		20		20		20		20		Setup and hold times for DMACK_
t_{SS}	50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP

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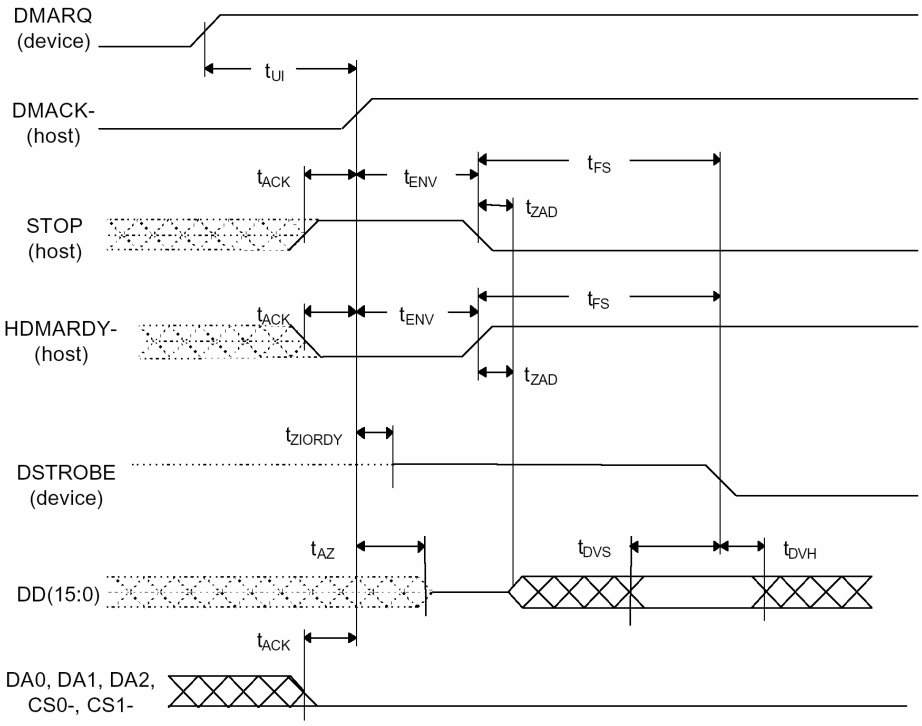
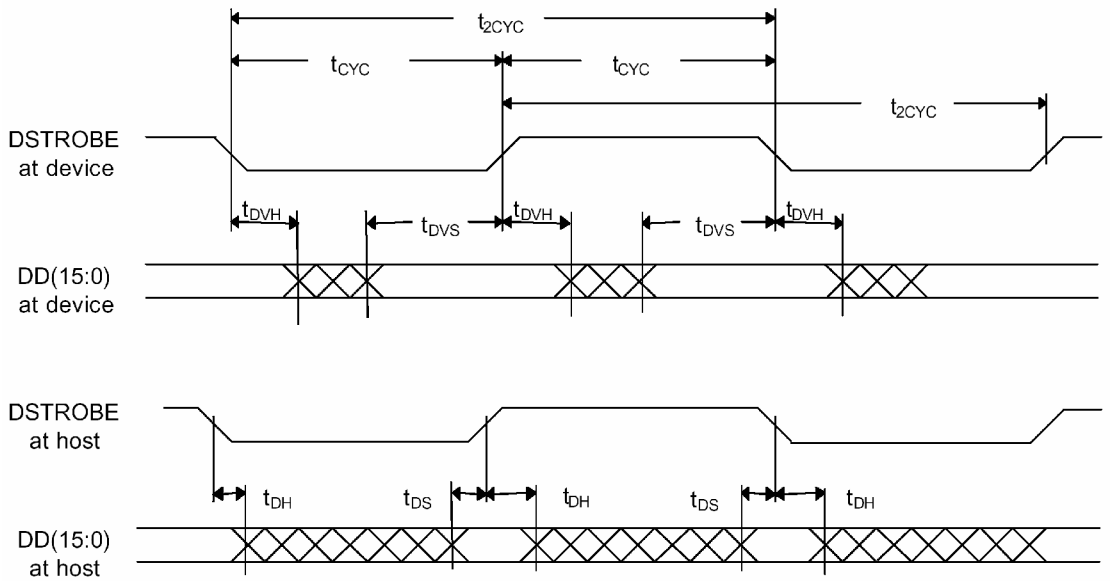


Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are not in efficient until DMARQ and DMACK are asserted.

Figure 6.17 - Initiating an Ultra DMA Data-In Burst



Notes:
IODD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 6.18 - Sustained Ultra DMA Data-In Burst

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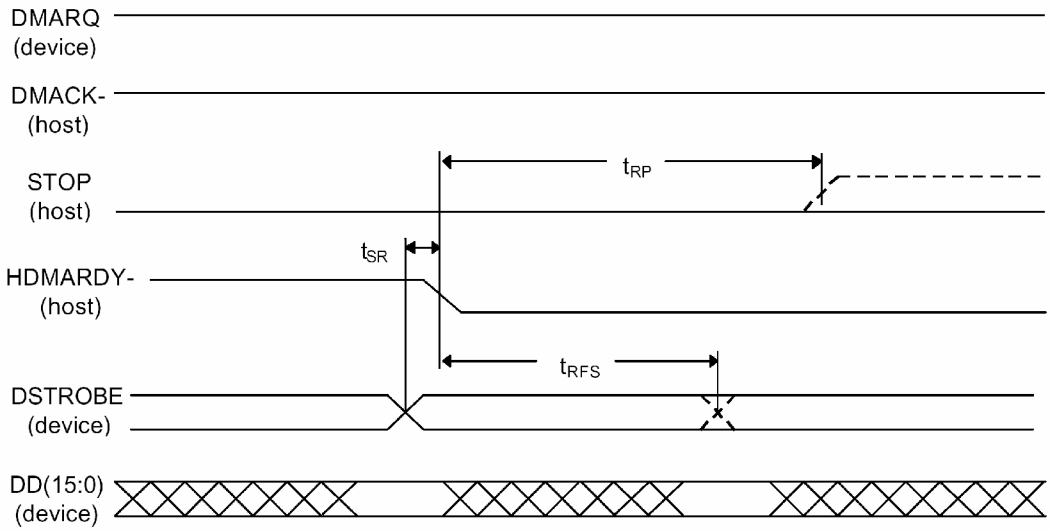
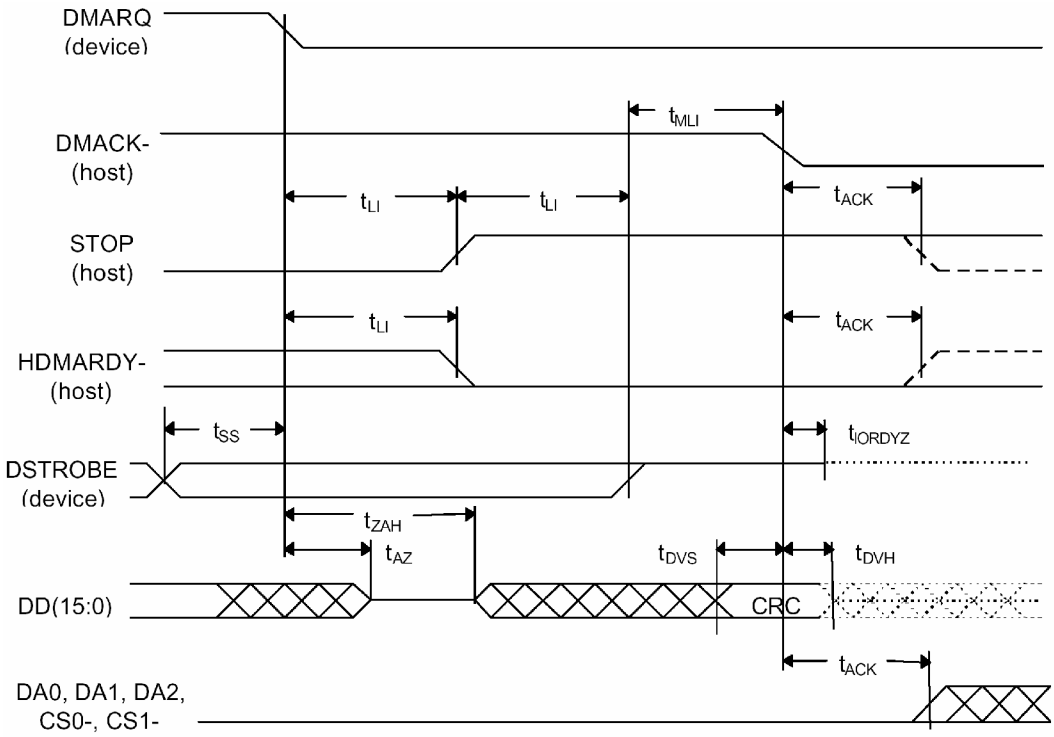


Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the device.

Figure 6.19 - Host Pausing an Ultra DMA Data-In Burst



Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.20 - Device Terminating an Ultra DMA Data-In Burst

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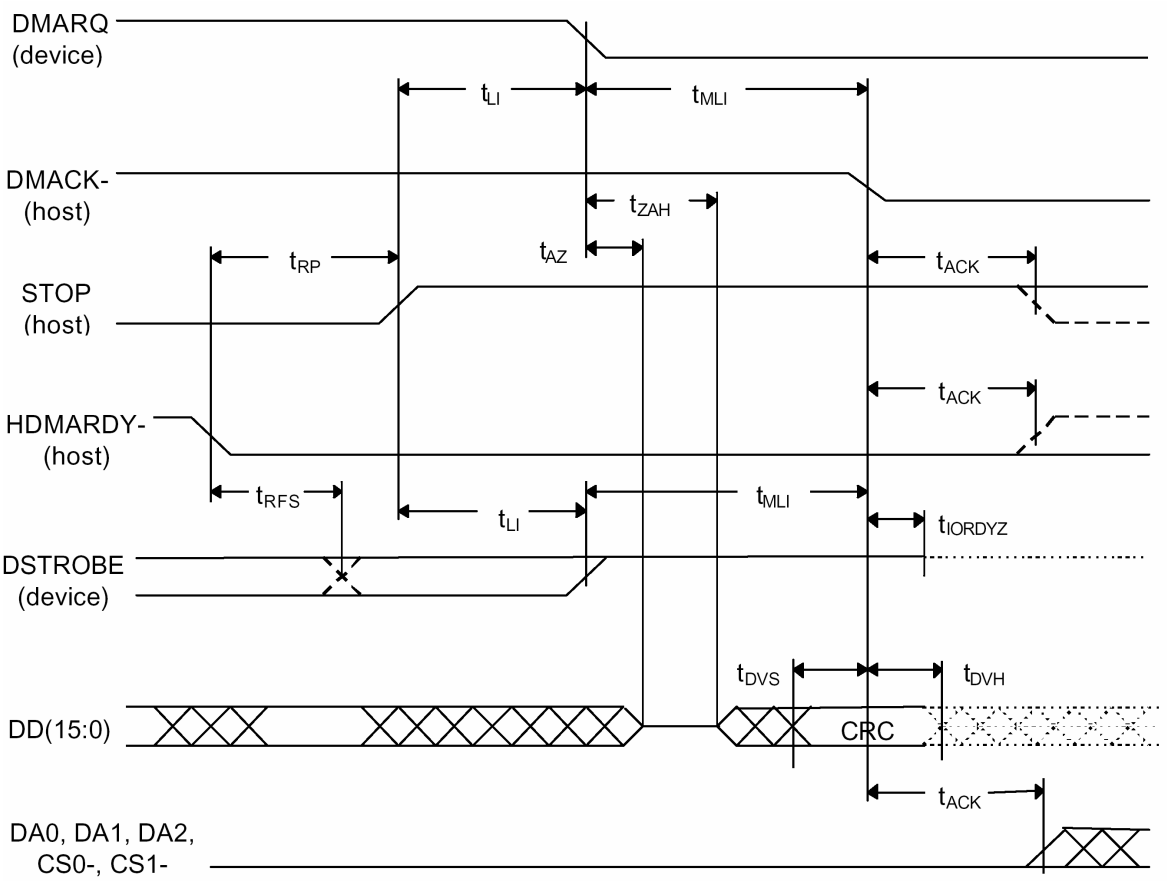

Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.21 - Host Terminating an Ultra DMA Data-In Burst

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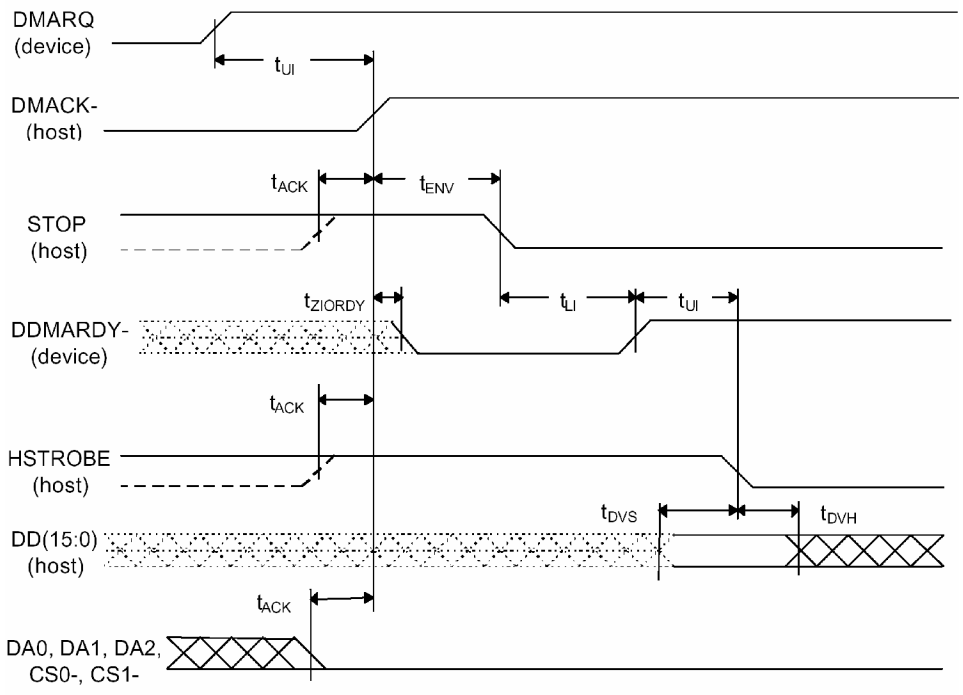
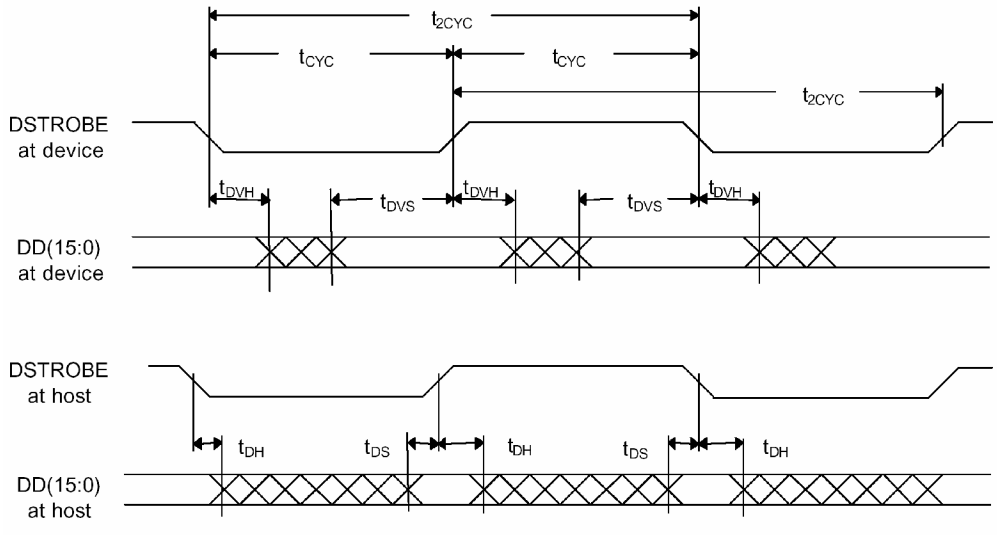


Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 6.22 - Initiating an Ultra DMA Data-Out Burst



Notes:
IODD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the devicet until some time after they are driven by the host.

Figure 6.23 - Sustained Ultra DMA Data-Out Burst

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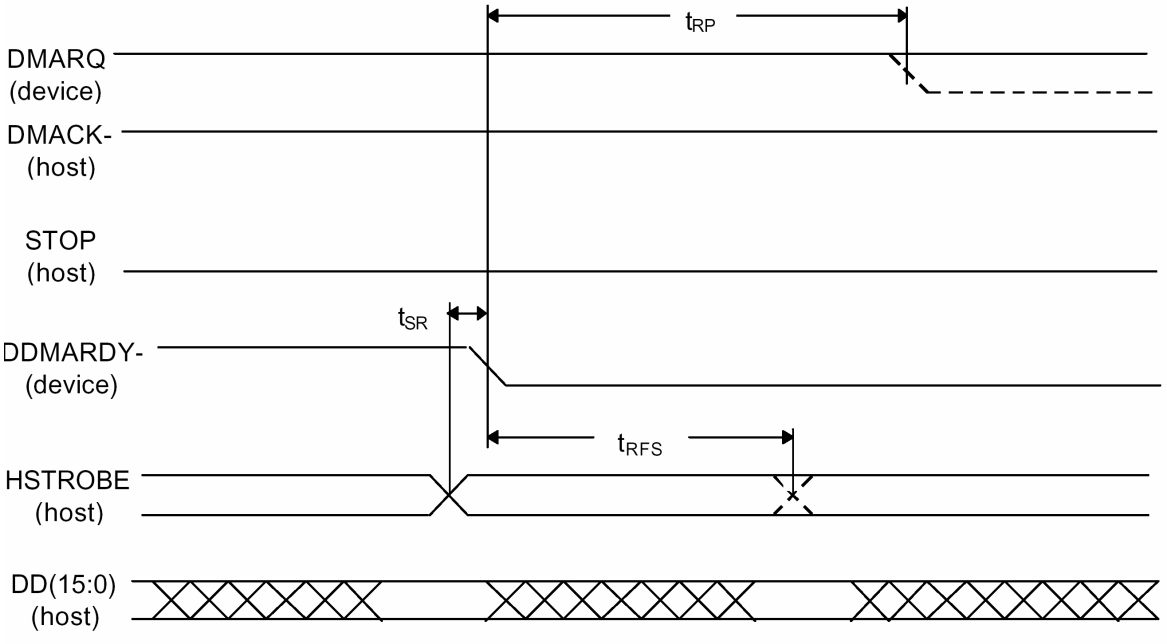

Notes:
1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the device may receive zero, one, or two more data words from the host.

Figure 6.24 - Device Pausing an Ultra DMA Data-Out Burst

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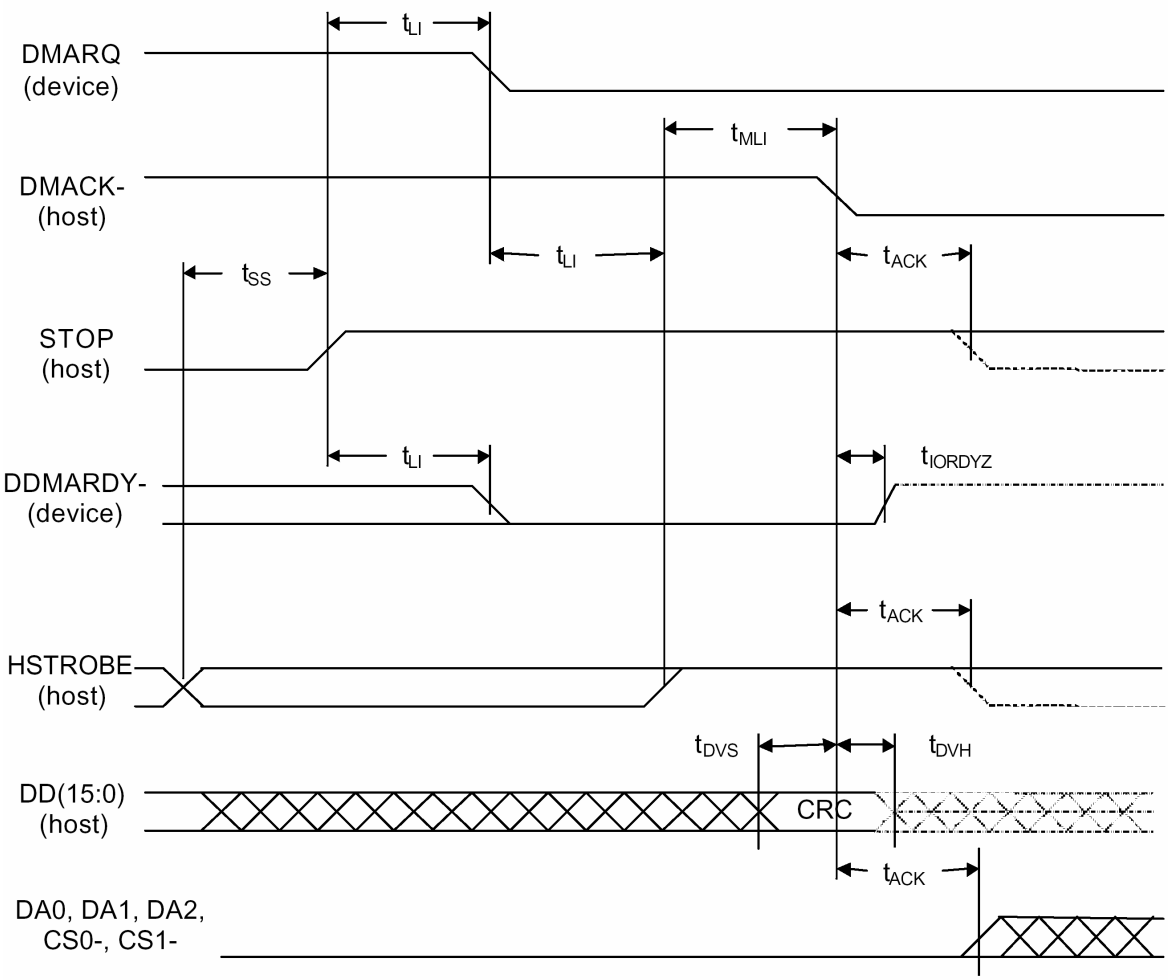

Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.25 - Host terminating an Ultra DMA data-out burst

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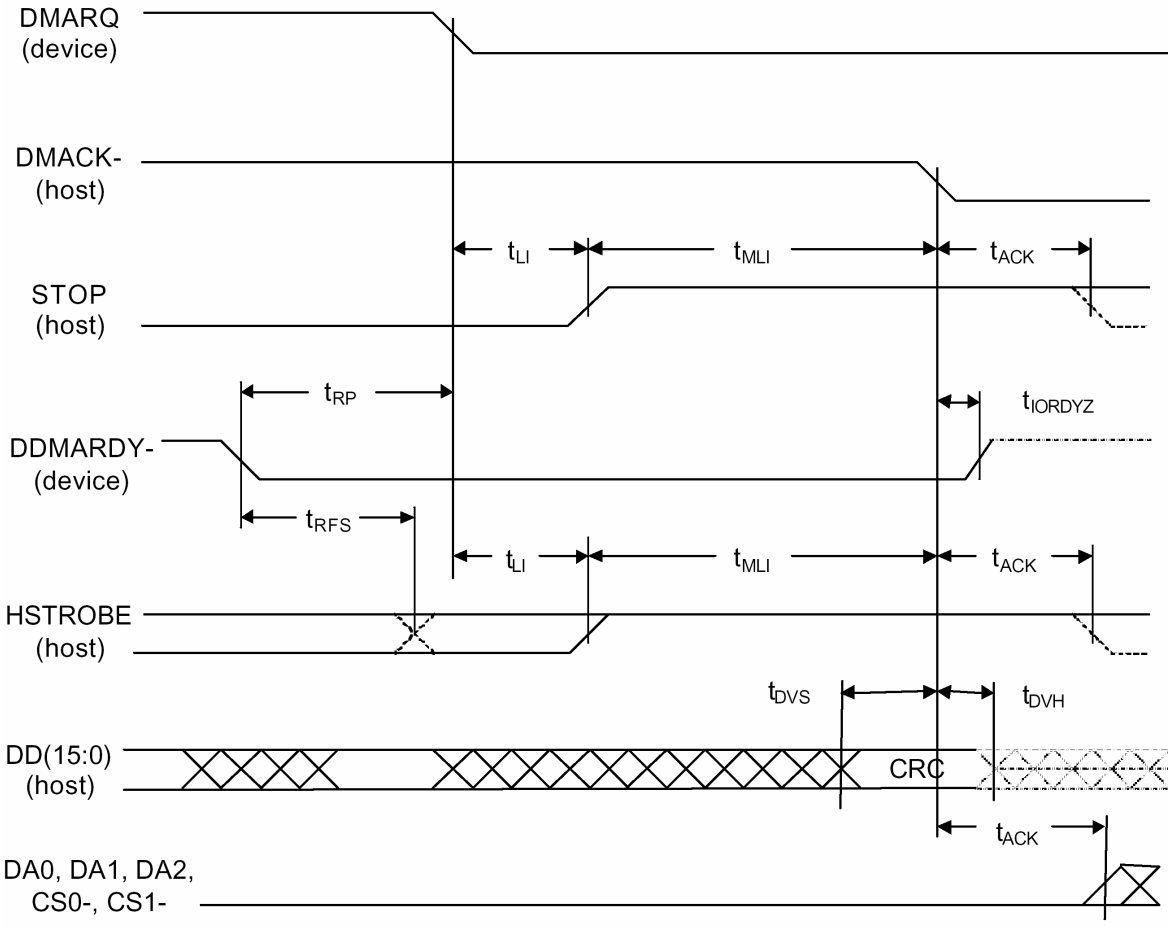

Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.26 - Device Terminating an Ultra DMA Data-Out Burst

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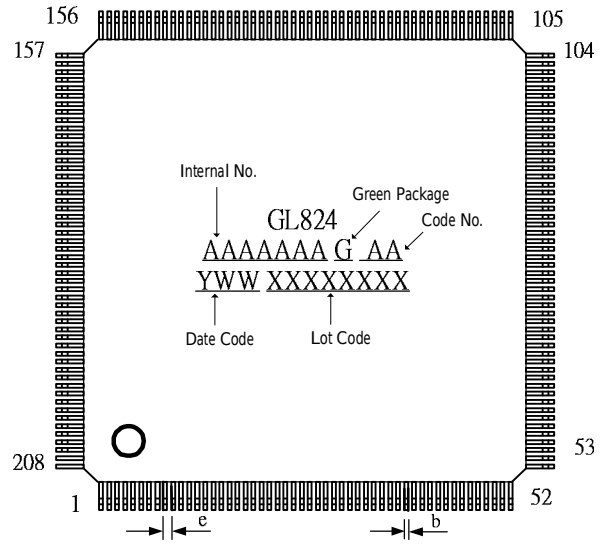
CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	--	--	1.60(63)
A1	0.05(2)	--	0.15(6)
A2	1.35(53)	1.40(55)	1.45(57)
b	0.17(7)	0.22(9)	0.27(11)
c	0.09(4)	--	0.20(8)
D	30.00 (1181) BSC		
D1	28.00 (1102) BSC		
E	30.00 (1181) BSC		
E1	28.00 (1120) BSC		
e	0.50 (20) BSC		
L	0.45(18)	0.60(24)	0.75(30)
L1	1.00 (39) REF		
Y	--	--	0.08(3)
θ	0°	3.5°	7°

NOTE: 1.REFER TO JEDEC MS-026

2.CONTROLLING DIMENSIIONS , MILLIMETER

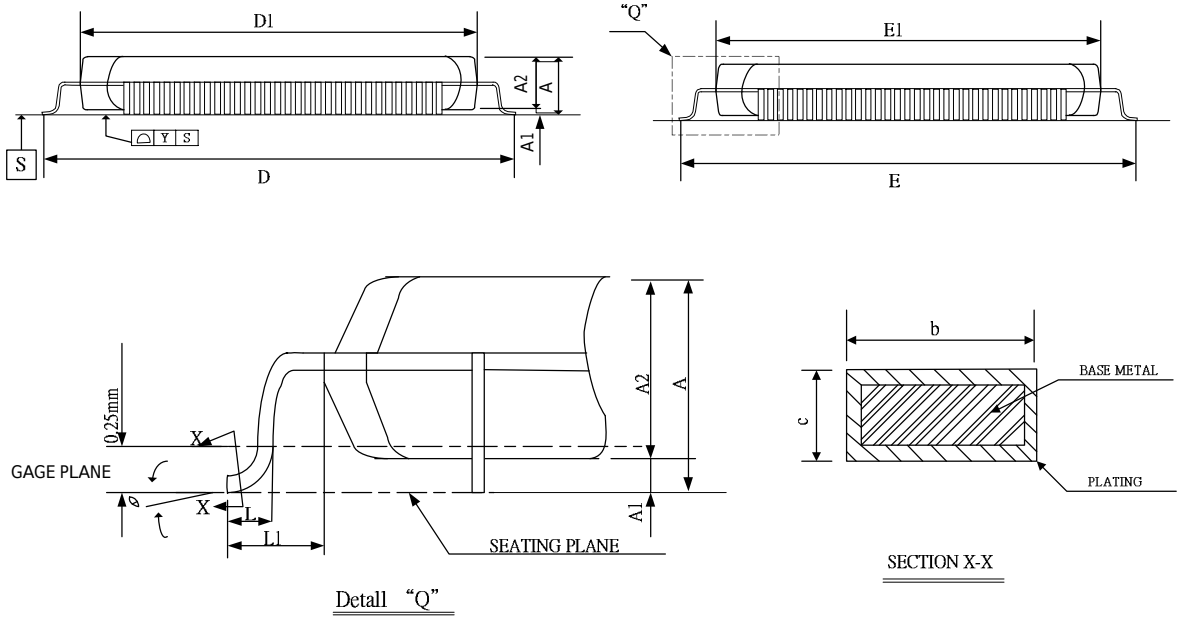


Figure 7.1 - GL824 208 Pin LQFP Package

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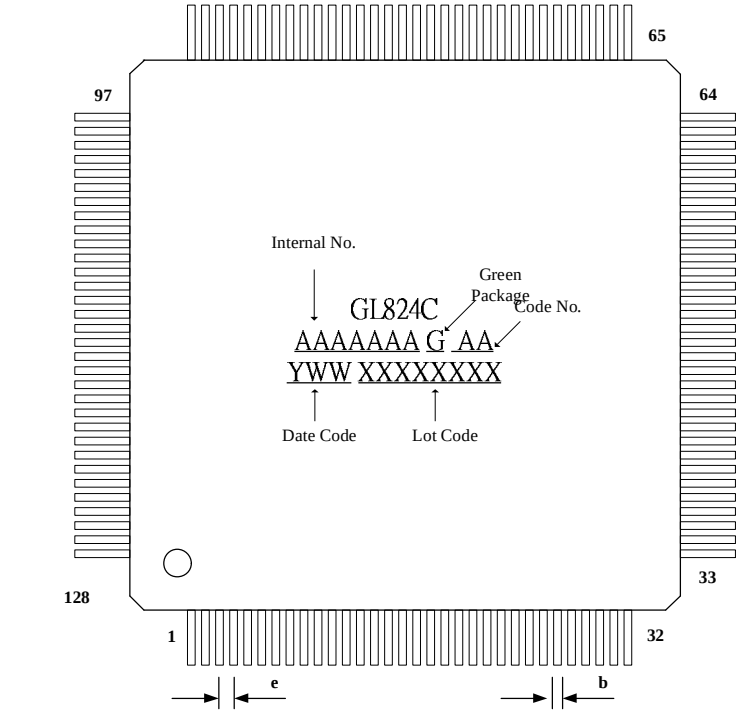
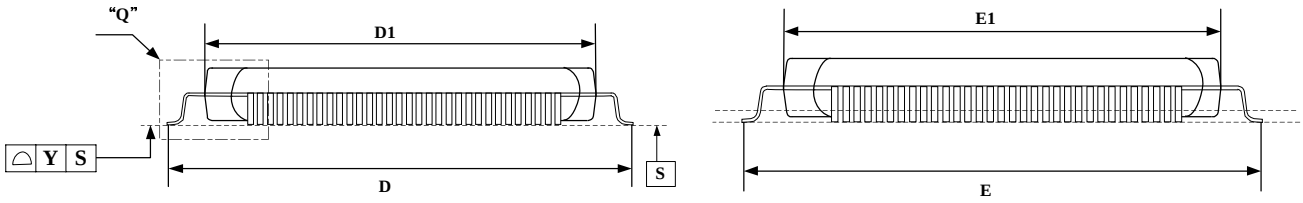
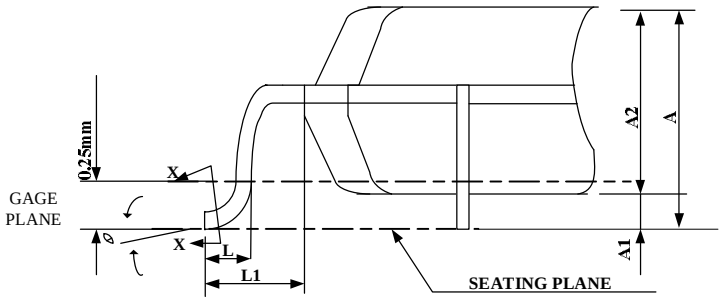


SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60(63)
A1	0.05(2)		0.15(6)
A2	1.35(53)	1.40(55)	1.45(57)
b	0.13(5)	0.18(7)	0.23(9)
c	0.09(4)		0.20(8)
D	16.00 (630) BSC		
D1	14.00 (551) BSC		
E	16.00 (630) BSC		
E1	14.00 (551) BSC		
e	0.40 (16) BSC		
L	0.45(18)	0.60(24)	0.75(30)
L1	1.00 (39) REF		
Y			0.10(4)
θ	0^o	3.5^o	7^o

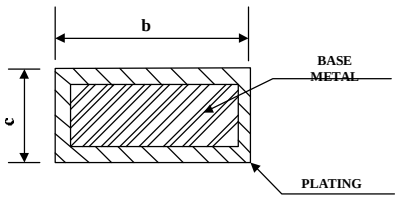
NOTE: 1.REFER TO JEDEC MS-026/BEE REV.B

2.ALL DIMENSIIONS IN MILLIMETERS.





Detall "Q"



SECTION X-X

Figure 7.2 - GL824C 128 Pin LQFP Package

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CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL824-MZGXX	208-pin LQFP	Green Package	XX	Available
GL824C-MXGXX	128-pin LQFP	Green Package	XX	Available

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