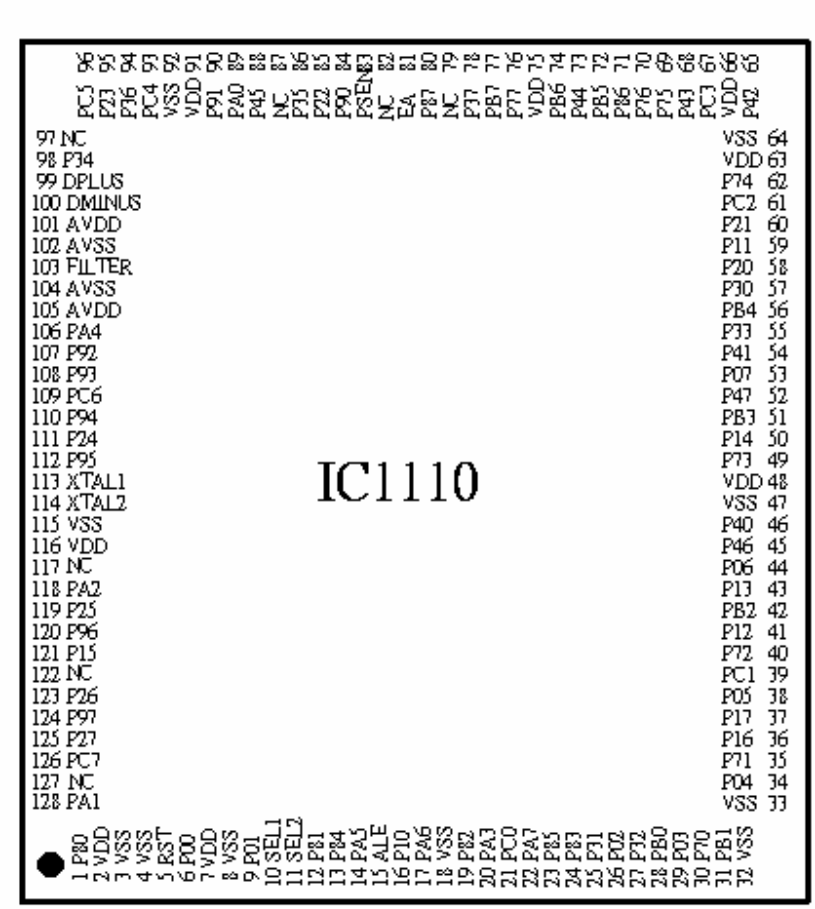
IC1110-F128LQ

USB Flash Card Reader Controller

1. FEATURES

- High speed 8-bit micro-controller with 4 system clocks per machine cycle
- Instruction-set compatible with MCS-51
- Embedded 32K-byte program FLASH ROM for product quick delivery. In System Programming, ISP is supported by either USB or I2C port.
- Built in fixed address 256 bytes data RAM.
- Built in floating address 4608 bytes data RAM
- Optional external floating data RAM space with up to 32M+32K bytes.
- Extra 1K bytes CPU data RAM space available by disable central control block function.
- System power saving mode ready, idle & power down modes.
- Three programmable 16-bit timer/counter and watchdog timer.
- Compliant with USB Specification Rev.1.1 supports full speed (12Mbits/sec), one device address and four endpoints. (Including control, interrupt, bulk in and bulk out endpoints)
- Built in ICSI in-house bi-directional parallel port for quick data transfer. Both master and slave modes are supported.
- Built in SDRAM interface for supporting memory size up to 256M bits.
- Master/Slave IIC and UART/RS-232 interface for external device communication.
- Compact Flash Card and IDE bus interface complies with Compact Flash Specification Rev.1.4 “True IDE Mode”, which is compatible with most hard disk drives and IBM micro drive.
- Smart Media Card/NAND type flash chip interface complies with Smart Media Specification Rev.1.1 and Smart Media Identify Number Specification Version 1.1
- Multi Media Card interface complies with Multi Media Card System Specification Rev. 1.4.
- SD Card interface complies with SD Card System Specification Rev. 1.0
- Memory Stick Card interface compiles with Memory Stick Standard Format Specifications version 1.3
- Built-in hardware ECC (Error Correction Code) check for Smart Media Card/NAND type flash chip.
- Built-in hardware CRC check for MMC and SD cards.
- Dedicated pins reserved for MP3 decoder interface.
- 3.0~3.6V supply.
- 128LQFP packages is available.

2. PIN INFORMATION



2.1.1. PIN FUNCTION DESCRIPTION

Function	Signal Name	IO	Pin Number	Description
Parallel Port	PP_D0	IO_TR	21	Parallel port data bus bit 0. Share with PC0
	PP_D1	IO_TR	39	Parallel port data bus bit 1. Share with PC1
	PP_D2	IO_TR	61	Parallel port data bus bit 2. Share with PC2
	PP_D3	IO_TR	67	Parallel port data bus bit 3. Share with PC3
	PP_D4	IO_TR	93	Parallel port data bus bit 4. Share with PC4
	PP_D5	IO_TR	96	Parallel port data bus bit 5. Share with PC5
	PP_D6	IO_TR	109	Parallel port data bus bit 6. Share with PC6
	PP_D7	IO_TR	126	Parallel port data bus bit 7. Share with PC7
	PP_RW	IO_PU	25	Parallel port read/write trigger, active high. Share with P31
	PP_RDY	IO_PU	57	Parallel port READY signal, active high. Share with P30

Function	Signal Name	IO	Pin Number	Description
	PP_EN	IO_TR	86	Parallel port enable, active high. Share with P35
	PP_DIR	IO_PU	88	Parallel port direction control. Share with P45
CF/IDE Card	CF_D0	IO_TR	30	CF card data bus bit 0. Share with P70
	CF_D1	IO_TR	35	CF card data bus bit 1. Share with P71
	CF_D2	IO_TR	40	CF card data bus bit 2. Share with P72
	CF_D3	IO_TR	49	CF card data bus bit 3. Share with P73
	CF_D4	IO_TR	62	CF card data bus bit 4. Share with P74
	CF_D5	IO_TR	69	CF card data bus bit 5. Share with P75
	CF_D6	IO_TR	70	CF card data bus bit 6. Share with P76
	CF_D7	IO_TR	76	CF card data bus bit 7. Share with P77
	CF_D8	IO_TR	84	CF card data bus bit 8. Share with P90
	CF_D9	IO_TR	90	CF card data bus bit 9. Share with P91
	CF_D10	IO_TR	107	CF card data bus bit 10. Share with P92
	CF_D11	IO_TR	108	CF card data bus bit 11. Share with P93
	CF_D12	IO_TR	110	CF card data bus bit 12. Share with P94
	CF_D13	IO_TR	112	CF card data bus bit 13. Share with P95
	CF_D14	IO_TR	120	CF card data bus bit 14. Share with P96
	CF_D15	IO_TR	124	CF card data bus bit 15. Share with P97
	CF_A0	IO_TR	36	CR card address bit 0. Share with P16
	CF_A1	IO_TR	37	CR card address bit 1. Share with P17
	CF_A2	IO_TR	1	CR card address bit 2. Share with P80
	CF_RDn	IO_TR	41	Read strobe pin to CF card. Share with P12
	CF_WRn	IO_TR	43	Write strobe pin to CF card. Share with P13
	CF_RSTN	IO_TR	59	Reset pin to CF card, active low. Share with P11
	CF_CS0	IO_TR	121	Card select pin 0. Share with P15
	CF_CS1	IO_TR	12	Card select pin 1. Share with P81
	CF_CD1	IO_PU	19	Card detection pin 1. Share with P82
	CF_CD2	IO_PU	24	Card detection pin 2. Share with P83
	CF_INTREQ	IO_TR	16	CF card interrupt request. Share with P10
SM Card	SM_D0	IO_TR	21	SM card data bus bit 0. Share with PC0
	SM_D1	IO_TR	39	SM card data bus bit 1. Share with PC1
	SM_D2	IO_TR	61	SM card data bus bit 2. Share with PC2
	SM_D3	IO_TR	67	SM card data bus bit 3. Share with PC3
	SM_D4	IO_TR	93	SM card data bus bit 4. Share with PC4
	SM_D5	IO_TR	96	SM card data bus bit 5. Share with PC5
	SM_D6	IO_TR	109	SM card data bus bit 6. Share with PC6
	SM_D7	IO_TR	126	SM card data bus bit 7. Share with PC7
	SM_CD1	IO_PU	13	Card detect pin, active low. Share with P84
	SM_CLE	IO_PU	88	Command latch enable, active high. Share with P45
	SM_RNB	IO_PU	45	Ready/Busy. Share with P46
	SM_ALE	IO_PU	52	Address latch enable, active high. Share with P47
	SM_RD	IO_TR	23	Read enable, active low. Share with P85
	SM_WR	IO_TR	71	Write enable, active low. Share with P86
	SM_WP	IO_TR	80	Write protect, active low. Share with P87
MMC/SD Card	MM_DAT0	IO_TR	21	MMC/SD card data bus bit 0. Share with PC0
	MM_DAT1	IO_TR	39	SD card data bus bit 1. Share with PC1
	MM_DAT2	IO_TR	61	SD card data bus bit 2. Share with PC2
	MM_DAT3	IO_TR	67	SD card data bus bit 3. Share with PC3

Function	Signal Name	IO	Pin Number	Description
	MM_CLK	IO_PU	68	MMC/SD card clock. Share with P43
	MM_CMD	IO_PU	73	MMC/SD card command. Share with P44
MS Card	MS_BS	IO_PU	46	MS card bus stat signal. Share with P40
	MS_SCLK	IO_PU	54	MS card clock signal. Share with P41
	MS_INS	IO_PU	65	MS card insertion/extraction detect. Share with P42
	MS_SDIO	IO_TR	93	MS card data bus. Share with PC4
SDRAM	DRM_DQ0	IO_TR	16	I/O data bit0. Share with P10
	DRM_DQ1	IO_TR	59	I/O data bit1. Share with P11
	DRM_DQ2	IO_TR	41	I/O data bit2. Share with P12
	DRM_DQ3	IO_TR	43	I/O data bit3. Share with P13
	DRM_DQ4	IO_TR	50	I/O data bit4. Share with P14
	DRM_DQ5	IO_TR	121	I/O data bit5. Share with P15
	DRM_DQ6	IO_TR	36	I/O data bit6. Share with P16
	DRM_DQ7	IO_TR	37	I/O data bit7. Share with P17
	DRM_A0	IO_TR	30	Address bit 0. Share with P70
	DRM_A1	IO_TR	35	Address bit 1. Share with P71
	DRM_A2	IO_TR	40	Address bit 2. Share with P72
	DRM_A3	IO_TR	49	Address bit 3. Share with P73
	DRM_A4	IO_TR	62	Address bit 4. Share with P74
	DRM_A5	IO_TR	69	Address bit 5. Share with P75
	DRM_A6	IO_TR	70	Address bit 6. Share with P76
	DRM_A7	IO_TR	76	Address bit 7. Share with P77
	DRM_A8	IO_TR	84	Address bit 8. Share with P90
	DRM_A9	IO_TR	90	Address bit 9. Share with P91
	DRM_A10	IO_TR	107	Address bit 10. Share with P92
	DRM_A11	IO_TR	108	Address bit 11. Share with P93
	DRM_A12	IO_TR	110	Address bit 12. Share with P94
	DRM_A13	IO_TR	112	Address bit 13. Share with P95
	DRM_A14	IO_TR	120	Address bit 14. Share with P96
	DRM_CLK	IO_TR	1	Clock output. Share with P80
	DRM_CAS	IO_TR	12	Column address strobe. Share with P81
	DRM_RAS	IO_TR	124	Raw address strobe. Share with P97
	DRM_WE	IO_TR	23	Write enable. Share with P85
	DRM_CSN	IO_TR	71	Chip select. Share with P86
	DRM_CKE	IO_TR	98	Clock enable. Share with P34
	DRM_UDQM	IO_TR	14	Upper byte I/O mask bit. Share with PA5
	DRM_LDQM	IO_TR	17	Lower byte I/O mask bit. Share with PA6
MP3	MP3_D	IO_TR	89	MP3 bit stream output. Share with PA0
	MP3_CLK	IO_TR	118	MP3 bit stream transmits clock. Share with PA2
	MP3_REQ	IO_TR	128	MP3 bit stream request, high active. Share with PA1
Master/Slave IIC	IIC_CL	IO_PU	25	IIC clock. Share with P31
	IIC_DA	IO_PU	57	IIC data. Share with P30
UART	TXD	IO_PU	25	Serial output. Share with P31
	RXD	IO_PU	57	Serial input. Share with P30
EXT ROM/RAM	AD0	IO_PU	6	Address and data for external ROM/RAM. Share with P00

Function	Signal Name	IO	Pin Number	Description
	AD1	IO_PU	9	Address and data for external ROM/RAM. Share with P01
	AD2	IO_PU	26	Address and data for external ROM/RAM. Share with P02
	AD3	IO_PU	29	Address and data for external ROM/RAM. Share with P03
	AD4	IO_PU	34	Address and data for external ROM/RAM. Share with P04
	AD5	IO_PU	38	Address and data for external ROM/RAM. Share with P05
	AD6	IO_PU	44	Address and data for external ROM/RAM. Share with P06
	AD7	IO_PU	53	Address and data for external ROM/RAM. Share with P07
	A8	IO_PU	58	Address for external ROM/RAM. Share with P20
	A9	IO_PU	60	Address for external ROM/RAM. Share with P21
	A10	IO_PU	85	Address for external ROM/RAM. Share with P22
	A11	IO_PU	95	Address for external ROM/RAM. Share with P23
	A12	IO_PU	111	Address for external ROM/RAM. Share with P24
	A13	IO_PU	119	Address for external ROM/RAM. Share with P25
	A14	IO_PU	123	Address for external ROM/RAM. Share with P26
	A15	IO_PU	125	Address for external ROM/RAM. Share with P27
	WR	IO_PU	94	Memory write for external RAM. Share with P36
	RD	IO_PU	78	Memory read for external RAM. Share with P37
Timer/counter	T0	IO_TR	98	External pin for timer 0. Share with P34
	T1	IO_TR	86	External pin for timer 1. Share with P35
	T2	IO_TR	16	External counter clock input for timer 2. Share with P10
	T2EX	IO_TR	59	External counter enable for timer 2. Share with P11
EXT interrupt	INT0	IO_PU	27	External interrupt 0. Share with P32
	INT1	IO_PU	55	External interrupt 1. Share with P33
AUX IO	P50	IO_PU	6	Port 5 bit 0. Share with P00
	P51	IO_PU	9	Port 5 bit 1. Share with P01
	P52	IO_PU	26	Port 5 bit 2. Share with P02
	P53	IO_PU	29	Port 5 bit 3. Share with P03
	P54	IO_PU	34	Port 5 bit 4. Share with P04
	P55	IO_PU	38	Port 5 bit 5. Share with P05
	P56	IO_PU	44	Port 5 bit 6. Share with P06
	P57	IO_PU	53	Port 5 bit 7. Share with P07
	P60	IO_PU	58	Port 6 bit 0. Share with P20
	P61	IO_PU	60	Port 6 bit 1. Share with P21
	P62	IO_PU	85	Port 6 bit 2. Share with P22
	P63	IO_PU	95	Port 6 bit 3. Share with P23
	P64	IO_PU	111	Port 6 bit 4. Share with P24
	P65	IO_PU	119	Port 6 bit 5. Share with P25
	P66	IO_PU	123	Port 6 bit 6. Share with P26
	P67	IO_PU	125	Port 6 bit 7. Share with P27
GPIO	P00	IO_PU	6	Port 0 bit 0.
	P01	IO_PU	9	Port 0 bit 1.
	P02	IO_PU	26	Port 0 bit 2.
	P03	IO_PU	29	Port 0 bit 3.
	P04	IO_PU	34	Port 0 bit 4.
	P05	IO_PU	38	Port 0 bit 5.
	P06	IO_PU	44	Port 0 bit 6.
	P07	IO_PU	53	Port 0 bit 7.

Function	Signal Name	IO	Pin Number	Description
	P10	IO_TR	16	Port 1 bit 0.
	P11	IO_TR	59	Port 1 bit 1.
	P12	IO_TR	41	Port 1 bit 2.
	P13	IO_TR	43	Port 1 bit 3.
	P14	IO_TR	50	Port 1 bit 4.
	P15	IO_TR	121	Port 1 bit 5.
	P16	IO_TR	36	Port 1 bit 6.
	P17	IO_TR	37	Port 1 bit 7.
	P20	IO_PU	58	Port 2 bit 0.
	P21	IO_PU	60	Port 2 bit 1.
	P22	IO_PU	85	Port 2 bit 2.
	P23	IO_PU	95	Port 2 bit 3.
	P24	IO_PU	111	Port 2 bit 4.
	P25	IO_PU	119	Port 2 bit 5.
	P26	IO_PU	123	Port 2 bit 6.
	P27	IO_PU	125	Port 2 bit 7.
	P30	IO_PU	57	Port 3 bit 0.
	P31	IO_PU	25	Port 3 bit 1.
	P32	IO_PU	27	Port 3 bit 2.
	P33	IO_PU	55	Port 3 bit 3.
	P34	IO_PU	98	Port 3 bit 4.
	P35	IO_PU	86	Port 3 bit 5.
	P36	IO_PU	94	Port 3 bit 6.
	P37	IO_PU	78	Port 3 bit 7.
	P40	IO_PU	46	Port 4 bit 0.
	P41	IO_PU	54	Port 4 bit 1.
	P42	IO_PU	65	Port 4 bit 2.
	P43	IO_PU	68	Port 4 bit 3.
	P44	IO_PU	73	Port 4 bit 4.
	P45	IO_PU	88	Port 4 bit 5.
	P46	IO_PU	45	Port 4 bit 6.
	P47	IO_PU	52	Port 4 bit 7.
	P70	IO_TR	30	Port 7 bit 0.
	P71	IO_TR	35	Port 7 bit 1.
	P72	IO_TR	40	Port 7 bit 2.
	P73	IO_TR	49	Port 7 bit 3.
	P74	IO_TR	62	Port 7 bit 4.
	P75	IO_TR	69	Port 7 bit 5.
	P76	IO_TR	70	Port 7 bit 6.
	P77	IO_TR	76	Port 7 bit 7.
	P80	IO_TR	1	Port 8 bit 0.
	P81	IO_TR	12	Port 8 bit 1.
	P82	IO_PU	19	Port 8 bit 2.
	P83	IO_PU	24	Port 8 bit 3.
	P84	IO_PU	13	Port 8 bit 4.
	P85	IO_TR	23	Port 8 bit 5.
	P86	IO_TR	71	Port 8 bit 6.
	P87	IO_TR	80	Port 8 bit 7.
	P90	IO_TR	84	Port 9 bit 0.
	P91	IO_TR	90	Port 9 bit 1.
	P92	IO_TR	107	Port 9 bit 2.

Function	Signal Name	IO	Pin Number	Description
	P93	IO_TR	108	Port 9 bit 3.
	P94	IO_TR	110	Port 9 bit 4.
	P95	IO_TR	112	Port 9 bit 5.
	P96	IO_TR	120	Port 9 bit 6.
	P97	IO_TR	124	Port 9 bit 7.
	PA0	IO_TR	89	Port A bit 0.
	PA1	IO_TR	128	Port A bit 1.
	PA2	IO_TR	118	Port A bit 2.
	PA3	IO_TR	20	Port A bit 3.
	PA4	IO_TR	106	Port A bit 4.
	PA5	IO_TR	14	Port A bit 5.
	PA6	IO_TR	17	Port A bit 6.
	PA7	IO_TR	22	Port A bit 7.
	PB0	IO_TR	28	Port B bit 0.
	PB1	IO_TR	31	Port B bit 1.
	PB2	IO_TR	42	Port B bit 2.
	PB3	IO_TR	51	Port B bit 3.
	PB4	IO_TR	56	Port B bit 4.
	PB5	IO_TR	72	Port B bit 5.
	PB6	IO_TR	74	Port B bit 6.
	PB7	IO_TR	77	Port B bit 7.
	PC0	IO_TR	21	Port C bit 0.
	PC1	IO_TR	39	Port C bit 1.
	PC2	IO_TR	61	Port C bit 2.
	PC3	IO_TR	67	Port C bit 3.
	PC4	IO_TR	93	Port C bit 4.
	PC5	IO_TR	96	Port C bit 5.
	PC6	IO_TR	109	Port C bit 6.
	PC7	IO_TR	126	Port D bit 7.
	PD0	IO_TR	79	Port D bit 0.
	PD1	IO_TR	82	Port D bit 1.
	PD2	IO_TR	87	Port D bit 2.
	PD3	IO_TR	97	Port D bit 3.
	PD4	IO_PU	117	Port D bit 4.
	PD5	IO_TR	122	Port D bit 5.
PLL	FILTER	O	103	External loop filter pin, a capacitor is connected between this pin and analog ground
USB	DPLUS	IO	99	USB DPLUS pin
	DMINUS	IO	100	USB DMINUS pin
XTAL	XTAL1	I	113	XTAL oscillator input pin
	XTAL2	O	114	XTAL oscillator output pin
Power	AVDD	P	101/105	Analog 3.3V
	AVSS	P	102/104	Analog ground
Power	VSS	P	18/47/92/ 115/3/33/ 64/4/8	Digital ground pin

Function	Signal Name	IO	Pin Number	Description
	VDD	P	48/66/91/ 116/32/63/ 75/2/7	Digital 3.3V
	RST	I	5	System reset pin, Shmmit trigger
	ALE	O	15	External address latch enable pin
	EA	I	81	Enable external ROM mode, disable internal FLASH
	PSEN	O	83	External ROM data output enable
SELCLK	SEL1	I	10	CPU clock select pin 1
	SEL2	I	11	CPU clock select pin 2

Note :

- After reset, all extra function is disabling. When extra function enable, that I/O is in input or output mode is dependent on pin function.
- Ports are GPIO and input after reset, and still a GPIO if the extra function does not turn on by software. The initial state of GPIO is High, LOW, or TRI-STATE, which is dependent on I/O cell as IO_PU, IO_PD or IO_TR.
- SEL [2:1]=00, 01, or 10 CPU clock is 12Mhz, 24Mhz or 48Mhz. SEL [2:1]=11 is reserved.
- Connect 1.2 Mohm between XTAL1 and XTAL2.
- Connect 820 pF between FILTER and VSS.

3. FUNCTION DESCRIPTION

IC1110 includes a turbo 80T32 CPU core, 32K-byte internal program Flash-ROM, 5.5-bytes SRAM and many interface blocks. Including USB function, CF/SM/MMC/SD/MS flash card interface, IBM micro drive interface, IDE hard disk interface, UART, NAND type flash chip interface, SDRAM interface, I2C master & slave blocks, high speed parallel port master & slave interface and MP3 decoder interface. If turning on extra function, the data can be shared through central control block as Figure 1. Data can be transferred very effective and result a best performance in card reader and other application.

The IC1110 embedded full speed USB port as major bridges to talk to other host. IC1110 also provides both master and slave parallel port, UART port and I2C port for any extended function usage. For those early development or code always changing environment, IC1110 provides a flexible solution with embedded 32K bytes program Flash-ROM. User can update her/his ROM code by our built in ISP function. IC1110's ISP function gives customer three different choices to take, via USB and I2C.

IC1110 can support CPU data memory space up to 5.5K bytes by turning off central control block. For that huge data RAM consumed application, IC1110 will give customer another external 32Mbytes space via bank access method, 32K bytes for each bank. This extra space can still be accessed by executing "MOVX" command and pins of P0 and P2 are still general I/O. In external ROM/SRAM functions pins of P0 and P2 are still available as address and data. User only needs to take care address map without overlap.

For those more I/O ports required applications, IC1110 can provide up to 94 general I/O pins.

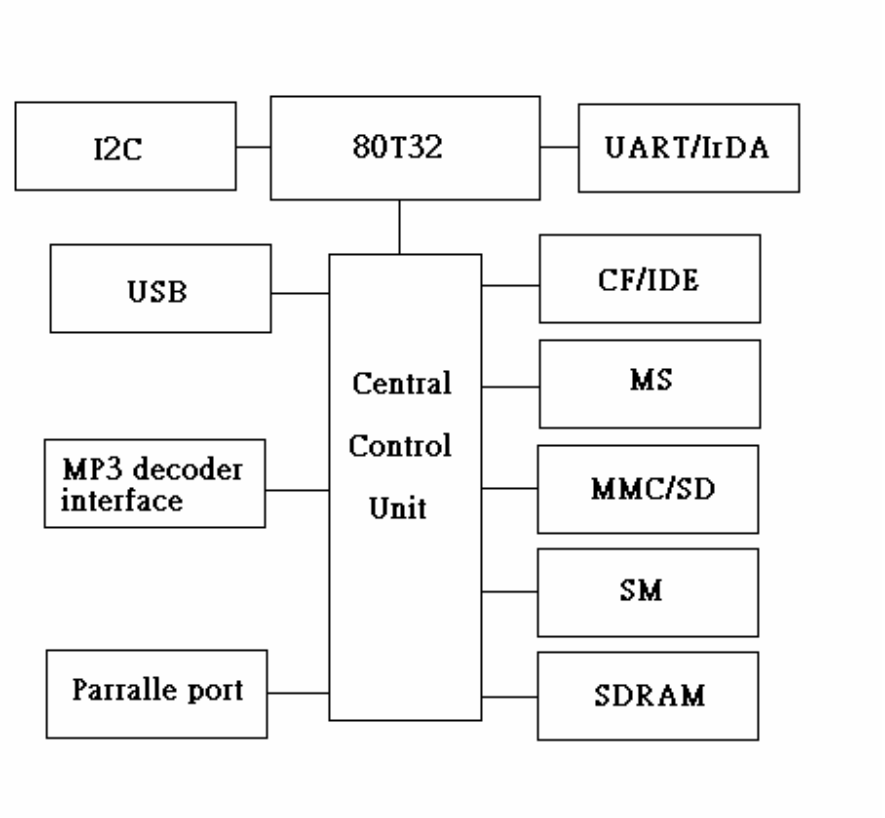


Figure 1. System block diagram

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating temperature under bias	0 to +70	℃ (1)
Storage temperature range	-65 to +125	℃
Voltage on any other pin to VSS	3.0 to 3.6	V (2)

Notes

1. Operating temperature is for commercial product defined by this spec.

2. Minimum D.C. input voltage is -0.5 V. During transitions, inputs may undershoot ,to -2.0 V for periods less than 20 ns. Maximum D.C. voltage on output pins is VCC+0.5 V, which may overshoot to VCC + 2.0 V for periods less than 20 ns.

Warning

Stressing the device beyond the "Absolute Maximum Rating" may cause permanent damage. This is stress rating only. Operation beyond the "operating conditions" is not recommended and extended exposure beyond the "operating conditions" may affect device reliability.

5. OPERATING CONDITION

Recommended Operating Conditions (TA = 0 to 70 C)

Symbol	Parameter	Min	TYP	Max	Unit
VDD	Power supply voltage(reference to VSS PIN)	3.0	3.3	3.6	V
Vil	Input low voltage of all GPIO PAD	-0.5	0	0.8	V
Vih	Input high voltage of all GPIO PAD	2.0	3.3	5.5	V
CLOCK Signal	Clock input frequency at XTAL1	12-30ppm	12	12+30ppm	MHz
Filter Cap	PLL filter capacitor	779	820	861	pF

Operating ranges define those limits between which the functionality of the device is guaranteed.

6. DC ELECTRICAL CHARACTERISTICS

DC Characteristics (3.3V +/- 0.3 V, 12MHz, T_A= 25°C)

Symbol	Parameter	Min	TYP	Max	Unit	Test condition
Vol.	Output low of all GPIO			0.4	V	Iol = 4mA
Voh	Output high of all GPIO	2.4			V	Ioh = 4mA
Vol(USB)	Static OUTPUT Low			0.3	V	RL=1.5K 3.6V
Voh(USB)	Static OUTPUT High	2.8		3.6	V	RL=1.5K 3.6V
Iil,Iih	Input leakage current for All Tri-State GPIO	-10		10	uA	Vin=0 or 3.6 V
Iil	Input leakage current for All IO_PU GPIO			-75	uA	Vin=0
Iih	Input leakage current for All IO_PD GPIO			75	uA	Vin=3.6 V
Ru	IO_PU pull up resistor	50	100	150	K	
Rd	IO_PD pull down resistor	50	100	150	K	
Vdr	Minum voltage to keep RAM data	2			V	

Current Consumption

Icc	Active current 12 MHz 24 MHz 48 MHz		20 30 55		mA	Vcc = 3.6V
Icci	Idle current 12MHz 24MHz 48MHz		18 28 48		mA	Vcc = 3.6V
Ipd	Power down current		80		uA	Vcc = 3.6V

7. AC SPECIFICATION

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{\text{PSEN}}$
Q	Output Data	R	$\overline{\text{RD}}$ signal
V	Valid	W	$\overline{\text{WR}}$ signal
X	No longer a valid state	Z	Tri-state

The following tables are defined under following condition:

Ta=0℃ to 70℃;

Vcc=3.3V ± 10%;

Vss=0V;

Cl for port 0, ALE and $\overline{\textbf{PSEN}}$ Outputs=100 pF;

Cl for other outputs=80 pF

7.1 ECTERNAL MEMORY CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS
Oscillator Frequency	$1/t_{CLCL}$	3.5	40	MHz
ALE Pulse Width	t_{LHLL}	$1.5t_{CLCL}$ - 6	-	ns
Address Valid to ALE Low	t_{AVLL}	$0.5t_{CLCL}$ - 6	-	ns
Address Hold After ALE Low or MOVX $\overline{\text{WR}}$	t_{LLAX}	$0.5t_{CLCL}$ - 6	-	ns
ALE Low to Valid Instruction In	t_{LLIV}	-	$2.5t_{CLCL}$ - 20	ns
ALE Low to $\overline{\text{PSEN}}$ Low	t_{LLPL}	$0.5t_{CLCL}$ - 6	-	ns
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	$2.0t_{CLCL}$ - 6	-	ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In	t_{PLIV}	-	$2.0t_{CLCL}$ - 20	ns
Input Instruction Hold After $\overline{\text{PSEN}}$	t_{PXIX}	0	-	ns
Input Instruction Float After $\overline{\text{PSEN}}$	t_{PXIZ}	-	$1.0t_{CLCL}$ - 6	ns
Address to Valid Instr. In	t_{AVIV}		$3.0t_{CLCL}$ - 20	ns
$\overline{\text{PSEN}}$ Low to Address Float	t_{PLAZ}	-	5	ns

7.2 MOVX CHARACTERISTICS USING STRECH MEMORY CYCLES

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS	STRECH
Address Hold After ALE low for MOVX $\overline{WR}$	t_{LLAX1}	$0.5t_{CLCL} - 6$	- -	ns	$t_{MCS}=0$ $t_{MCS}>0$
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL} - 10$ $t_{MCS} - 10$	-	ns	$t_{MCS}=0$ $t_{MCS}>0$
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL} - 10$ $t_{MCS} - 10$	-	ns	$t_{MCS}=0$ $t_{MCS}>0$
$\overline{RD}$ Low to Valid Data In	t_{RLDV}	-	$2.0t_{CLCL} - 20$ $t_{MCS} - 20$	ns	$t_{MCS}=0$ $t_{MCS}>0$
Data Hold after $\overline{RD}$	t_{RHDX}	0	-	ns	
Data Float after $\overline{RD}$	t_{RHDZ}	-	$t_{CLCL} - 6$ $2.0t_{CLCL} - 6$	ns	$t_{MCS}=0$ $t_{MCS}>0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL} - 20$ $t_{MCS} - 20$	ns	$t_{MCS}=0$ $t_{MCS}>0$
Port 0 or Port 2 Address to Valid Data In	t_{AVDV}		$3.0t_{CLCL} - 20$ $t_{MCS} + 2.0t_{CLCL} - 20$	ns	$t_{MCS}=0$ $t_{MCS}>0$
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL} - 6$ $1.5t_{CLCL} - 6$	$0.5t_{CLCL} + 6$ $1.5t_{CLCL} + 6$	ns	$t_{MCS}=0$ $t_{MCS}>0$
Port 0 or Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	$t_{CLCL} - 10$ $2.0t_{CLCL} - 10$	-	ns	$t_{MCS}=0$ $t_{MCS}>0$
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5 $t_{CLCL} - 10$	-	ns	$t_{MCS}=0$ $t_{MCS}>0$
Data Hold after $\overline{WR}$	t_{WHQX}	$t_{CLCL} - 10$ $2.0t_{CLCL} - 10$	-	ns	$t_{MCS}=0$ $t_{MCS}>0$
$\overline{RD}$ Low to Address Float	t_{RLAZ}	-	$0.5t_{CLCL} - 6$	ns	
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 10$	10 $1.0t_{CLCL} + 10$	ns	$t_{MCS}=0$ $t_{MCS}>0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the stretch value.

M2	M1	M0	MOVX machine cycles	t_{MCS}
0	0	0	2	0
0	0	1	3	4 t_{CLCL}
0	1	0	4	8 t_{CLCL}
0	1	1	5	12 t_{CLCL}
1	0	0	6	16 t_{CLCL}
1	0	1	7	20 t_{CLCL}
1	1	0	8	24 t_{CLCL}
1	1	1	9	28 t_{CLCL}

7.3 SERIAL PORT MODE 0 TIMING CHARACTERISTIC

PARAMETER	SYMBOL	MIN	MAX	UNITS
Serial Port Clock Cycle Time SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XLXL}	$12t_{CLCL}$-10 $4t_{CLCL}$-10	$12t_{CLCL}$+10 $4t_{CLCL}$+10	ns
Output Data Setup to Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{QVXH}	$10t_{CLCL}$-10 $3t_{CLCL}$-10	- -	ns
Output Data Hold to Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHQX}	$2t_{CLCL}$-10 t_{CLCL}-10	- -	ns
Input Data Hold after Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHDX}	t_{CLCL} t_{CLCL}	- -	ns
Clock Ring Edge to Input Data Valid SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHDV}	- -	$11t_{CLCL}$ $3t_{CLCL}$	ns

7.4 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	8	-	-	ns
Clock Low Time	t_{CLCX}	8	-	-	ns
Clock Rise Time	t_{CLCH}	-	-	5	ns
Clock Fall Time	t_{CHCL}	-	-	5	ns

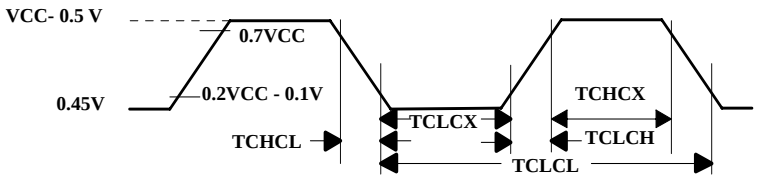


Figure 32. External clock drive waveform

8. TIMING DIAGRAM

8.1 PROGRAM MEMORY READ CYCLE

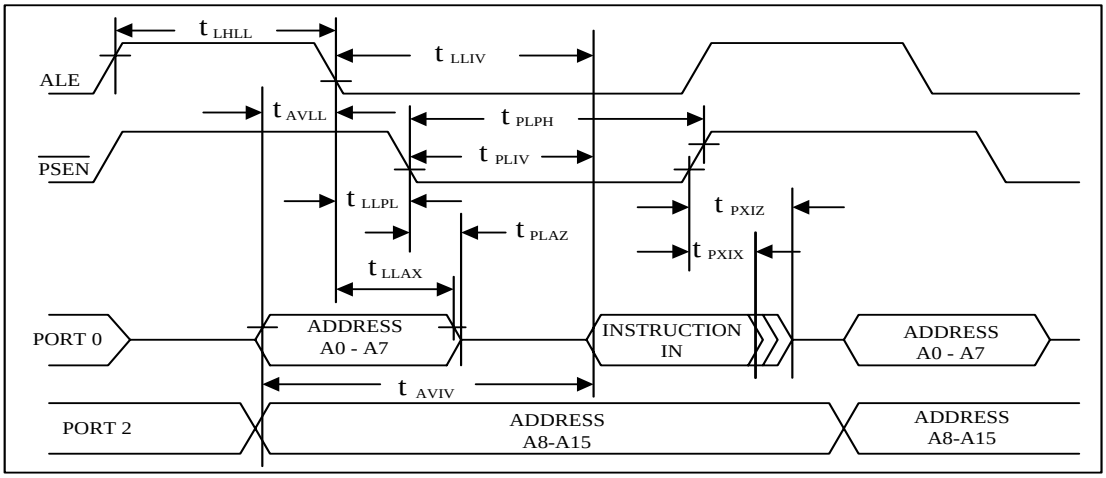


Figure 3. Program memory read cycle

8.2 DATA MEMORY READ CYCLE

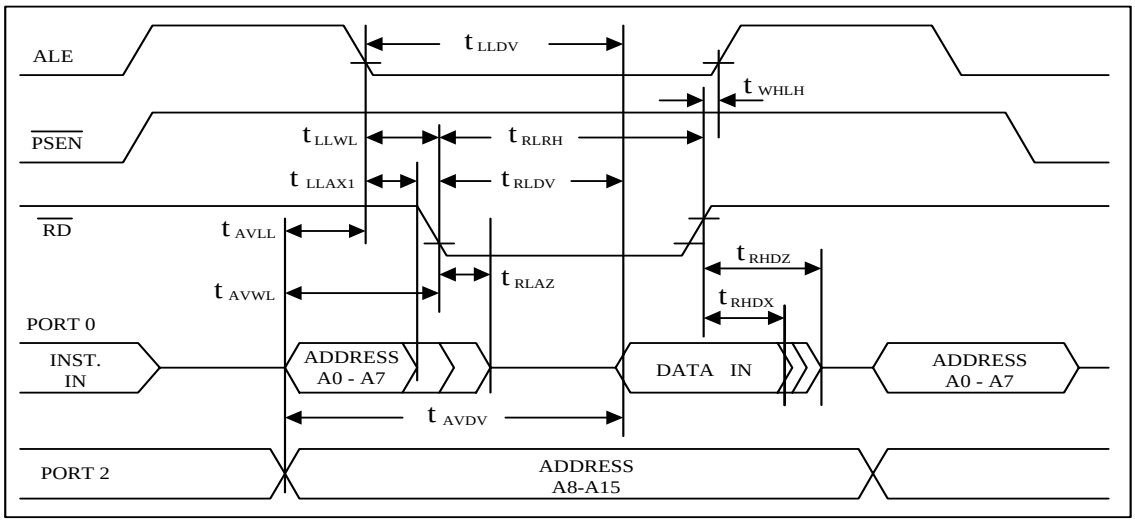


Figure 4. Data memory read cycle

8.3 DATA MEMORY WRITE CYCLE

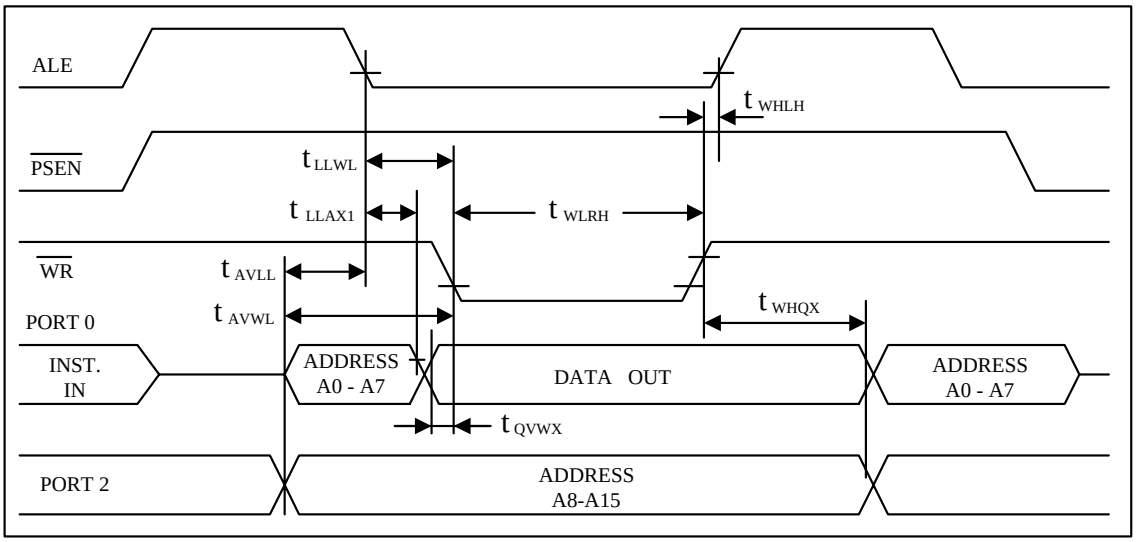


Figure 5. Data memory writes cycle

8.4 DATA MEMORY WRITE WITH STRECH = 0

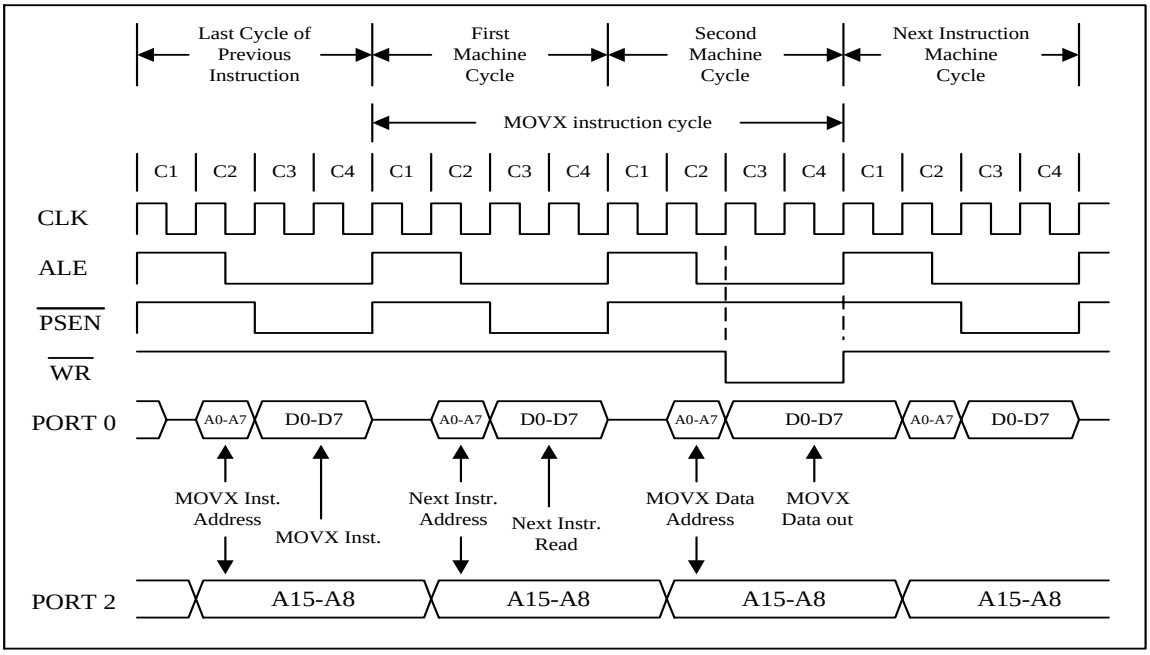


Figure 6. Data memory write with strech=0

8.5 DATA MEMORY WRITE WITH STRECH = 1

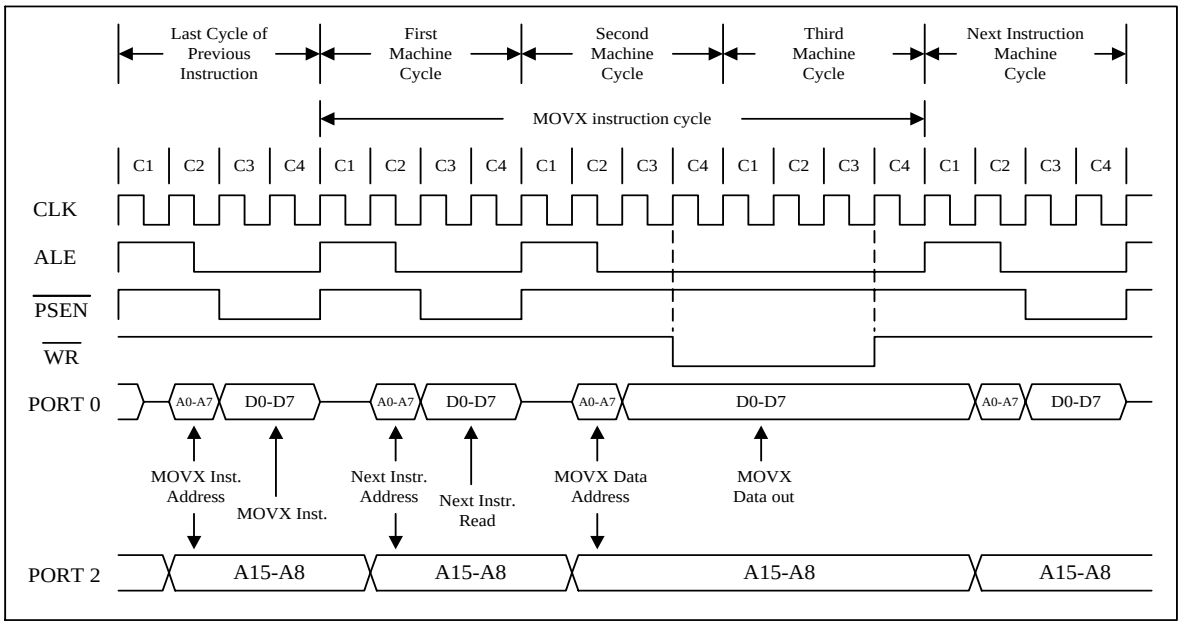


Figure 7. Data memory write with strech=1

8.6 DATA MEMORY WRITE WITH STRECH = 2

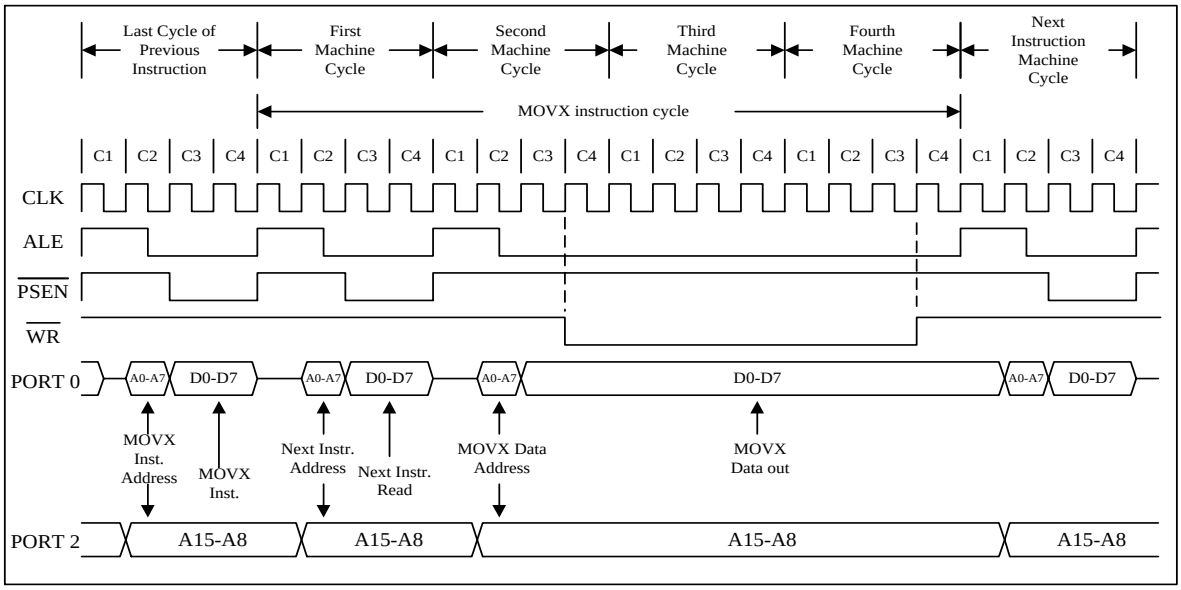


Figure 8. Data memory write with strech=0

8.7 SERIAL PORT MODE 0 TIMING

Serial Port (Synchronous Mode)

High Speed Operation SM2=1 => TxD Clock = XTAL/4

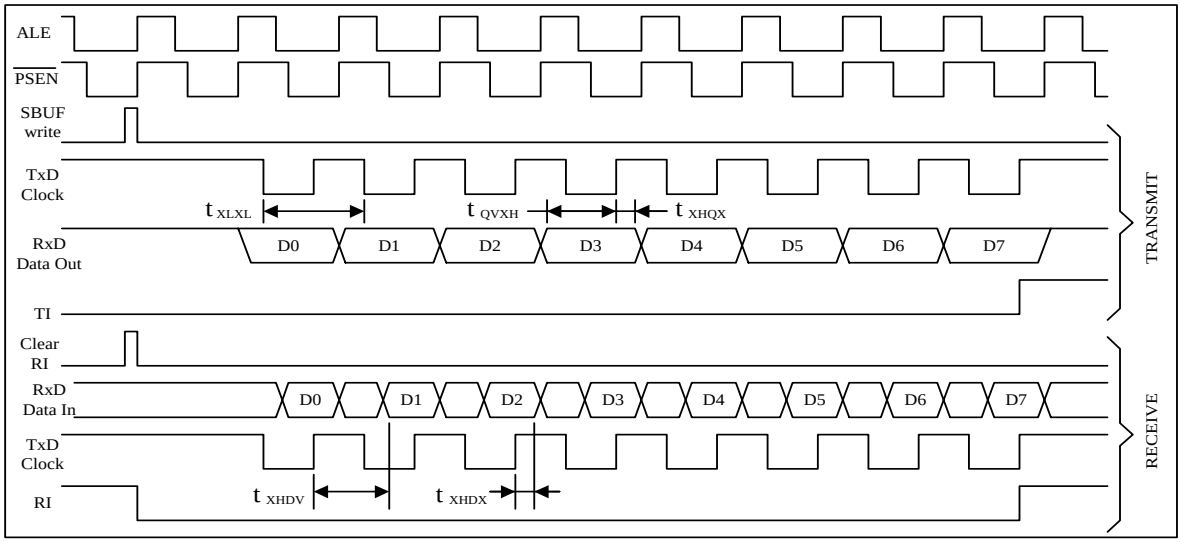


Figure 9. Serial port mode 0 timing at high speed operation

Serial Port (Synchronous Mode)

Standard Operation SM2=1 => TxD Clock = XTAL/12

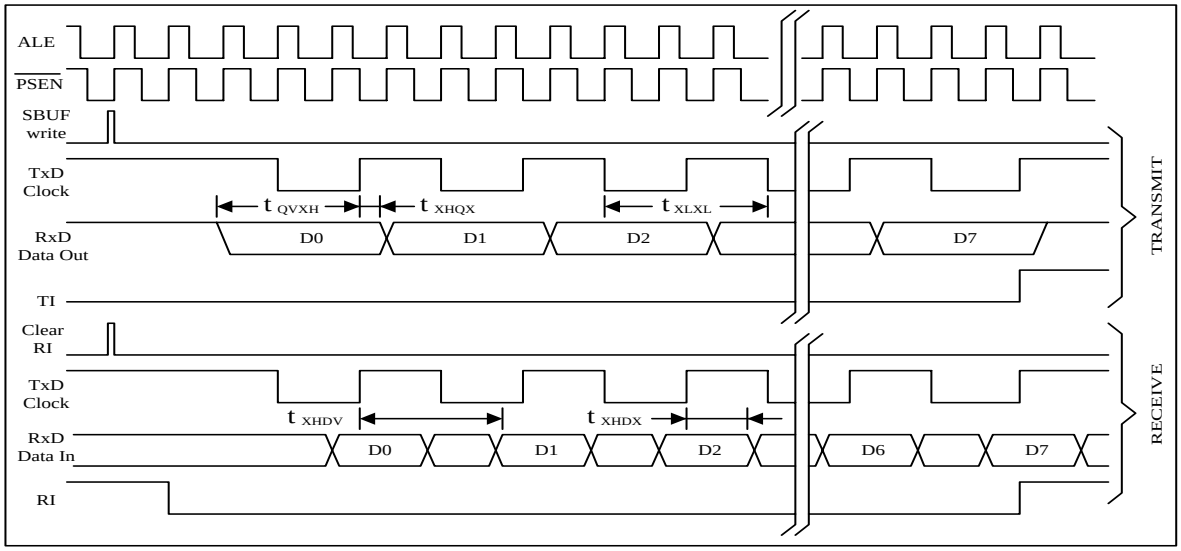


Figure 10. Serial port mode 0 timing at standard operation

8.8 CARD INTERFACE TIMING

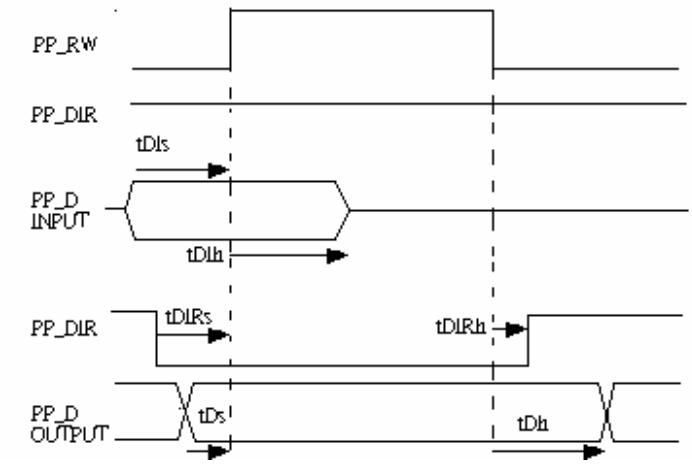


Figure 11 Parallel port read/write timing

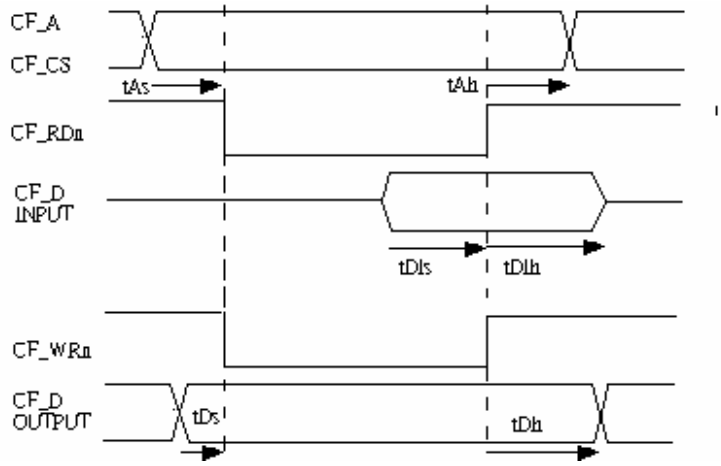


Figure 12 CF card read/write timing

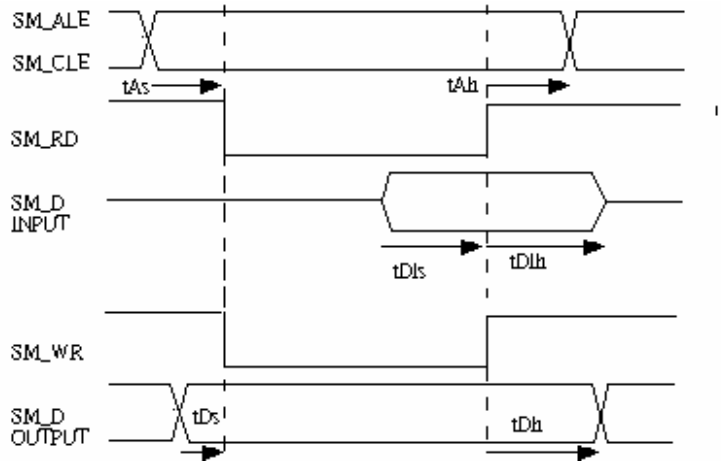


Figure 13 SM card read/write timing

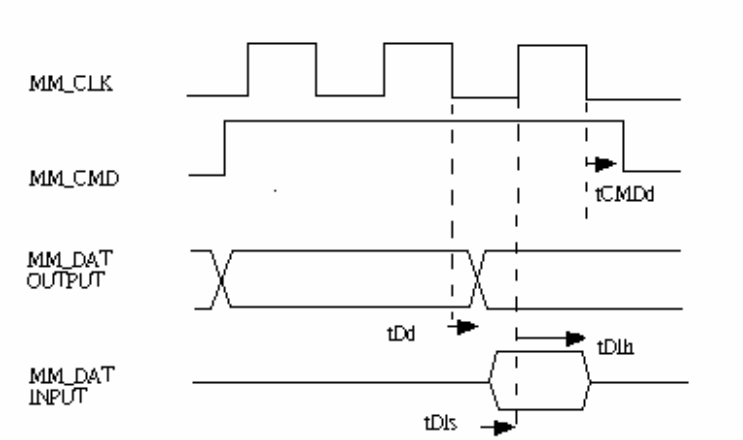


Figure 14 MMC/SD card read/write timing

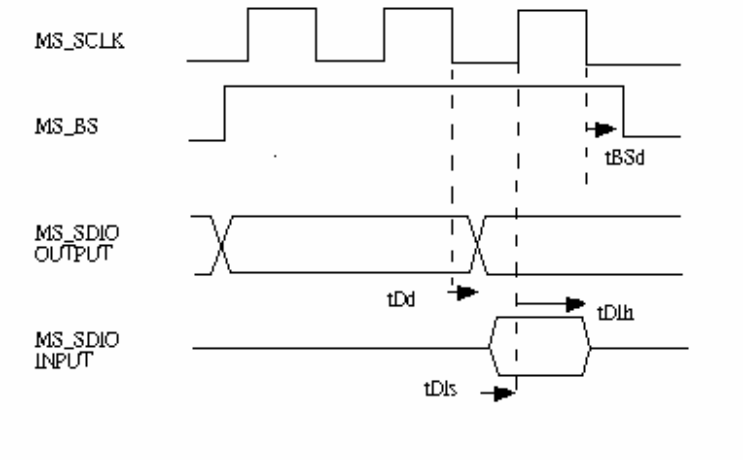


Figure 15 MS card read/write timing

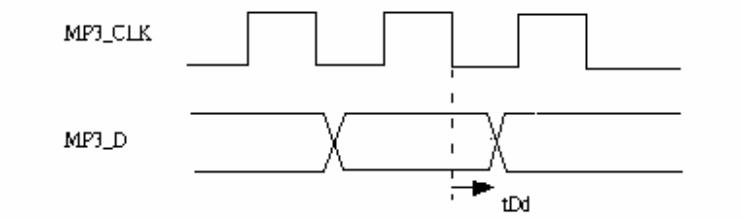


Figure 16 MP3 output timing

ORDERING INFORMATION

COMMERCIAL TEMPERATURE : 0 °C to +70 °C

Order Part Number	Package
IC1110-F128LQ	14*14*1.4mm LQFP

Integrated Circuit Solution Inc.

HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
FAX: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5 TH ROAD
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
http://www.icsi.com.tw