LANSDALE Semiconductor, Inc.

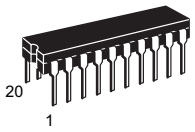
ML145407

5 Volt Only Driver/Receiver

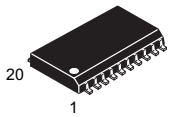
RS232 EIA–232–E and CCITT V.28

Legacy Device: *Motorola MC145407*

The ML145407 is a silicon–gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of RS232 EIA–232–E and CCITT V.28 while operating from a single + 5 V power supply. A voltage doubler and inverter convert the + 5V to ± 10 V. This is accomplished through an on–board 20 kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the ML145407 are virtually identical to those of the ML145406. Therefore, for applications requiring more than three drivers and/or three receivers, an ML145406 can be powered from an ML145407, since the ML145407 charge pumps have been designed to guarantee ± 5 V at the output of up to six drivers. Thus, the ML145407 provides a high–performance, low–power, stand–alone solution or, with the ML145406, a + 5 V only, high–performance two–chip solution.



P DIP 20 = RP
PLASTIC DIP
CASE 738



SOG 20 = -6P
SOG PACKAGE
CASE 751D

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 20	MC145407P	ML145407RP
SOG 20	MC145407DW	ML145407-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

This device offers the following performance features:

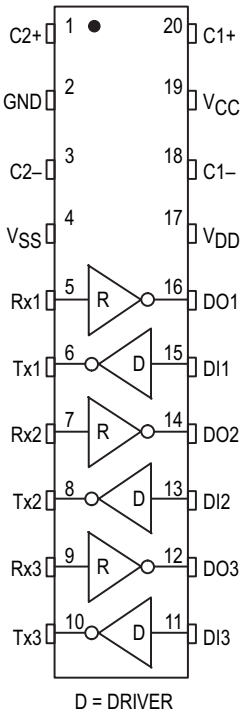
- Operating Temperature Range = T_A –40° to +85°C

Drivers
- ± 7.5 V Output Swing
- 300Ω Power–Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/μs to 30 V/μs

Receivers
- + 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity

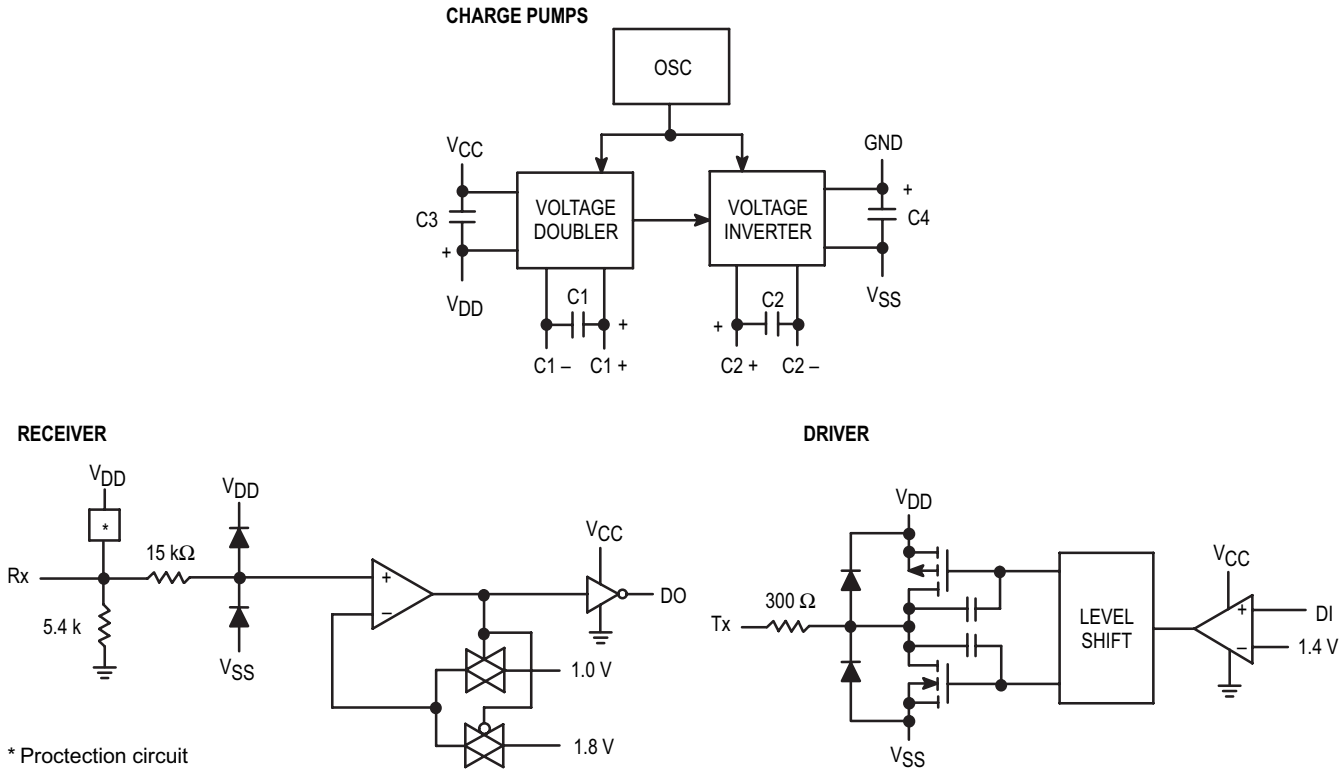
Charge Pumps
- + 5 V to ± 10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On–Chip Drivers and Three Drivers on the ML145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On–Chip 20 kHz Oscillator

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM



MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Range Rx1 – Rx3 Inputs DI1 – DI3 Inputs	V_{IR}	 V_{SS} – 15 to V_{DD} + 15 – 0.5 to (V_{CC} + 0.5)	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{CC} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the Rx pin should be constrained to (V_{SS} – 15 V) ≤ $V_{Rx1 – Rx3}$ ≤ (V_{DD} + 15 V), and Tx should be constrained to V_{SS} ≤ $V_{Tx1 – Tx3}$ ≤ V_{DD}.

Unused inputs must always be tied to appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; C1, C2, C3, C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low)		I_{CC}	—	1.2	3.0	mA
Output Voltage	I_{load} = 0 mA	V_{DD}	8.5	10	11	V
	I_{load} = 5 mA		7.5	9.5	—	
	I_{load} = 10 mA		6	9	—	
	I_{load} = 0 mA	V_{SS}	– 8.5	– 10	–11	
	I_{load} = 5 mA		– 7.5	– 9.2	—	
	I_{load} = 10 mA		– 6	– 8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1, C2, C3, C4 = 10 µF; T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–on Threshold $V_{DO1 – DO3}$ = V_{OL}	Rx1 – Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn–off Threshold $V_{DO1 – DO3}$ = V_{OH}	Rx1 – Rx3	V_{off}	0.75	1.0	1.25	V
Input Threshold Hysteresis (V_{on} – V_{off})	Rx1 – Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance	Rx1 – Rx3	R_{in}	3.0	5.4	7.0	kΩ
High–Level Output Voltage $V_{Rx1 – Rx3}$ = – 3 V to – 25 V I_{OH} = – 20 µA I_{OH} = – 1 mA	DO1 – DO3	V_{OH}	 V_{CC} – 0.1 V_{CC} – 0.7	 — 4.3	 — —	V
Low–Level Output Voltage $V_{Rx1 – Rx3}$ = + 3 V to + 25 V I_{OL} = + 20 µA I_{OL} = + 1.6 mA	DO1 – DO3	V_{OL}	 — —	 0.01 0.5	 0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V: V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = –40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2.0	—	—	
Input Current GND ≤ $V_{DI1 – DI3}$ ≤ V_{CC}	DI1 – DI3	I_{in}	—	—	± 1.0	μA
Output High Voltage	Tx1 – Tx3	V_{OH}	6	7.5	—	V
$V_{DI1 – DI3}$ = Logic 0, R_L = 3.0 kΩ	Tx1 – Tx6*		5	6.5	—	
Output Low Voltage	Tx1 – Tx3	V_{OL}	– 6	– 7.5	—	V
$V_{DI1 – DI3}$ = Logic 1, R_L = 3.0 kΩ	Tx1 – Tx6*		– 5	– 6.5	—	
Off Source Impedance (Figure 1)	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short–Circuit Current	Tx1 – Tx3	I_{SC}				mA
V_{CC} = + 5.5 V	Tx1 – Tx3 shorted to GND**		—	—	± 60	
	Tx1 – Tx3 shorted to ± 15 V***		—	—	± 100	

* Specifications for an ML145407 powering an ML145406 with three additional drivers/receivers.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V ± 10%; C1, C2, C3, C4 = 10 μF; T_A = – 40 to + 85°C; See Figures 2 and 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{PLH}				μs
Low–to–High						
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
High–to–Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
Output Slew Rate	Tx1 – Tx3	SR				V/μs
Minimum Load: R_L = 7 kΩ, C_L = 0 pF			—	9.0	± 30	
Maximum Load: R_L = 3 kΩ, C_L = 2500 pF			4.0	—	—	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1 – DO3					μs
Low–to–High		t_{PLH}	—	—	1	
High–to–Low		t_{PHL}	—	—	1	
Output Rise Time	DO1 – DO3	t_r	—	250	400	ns
Output Fall Time	DO1 – DO3	t_f	—	40	100	ns

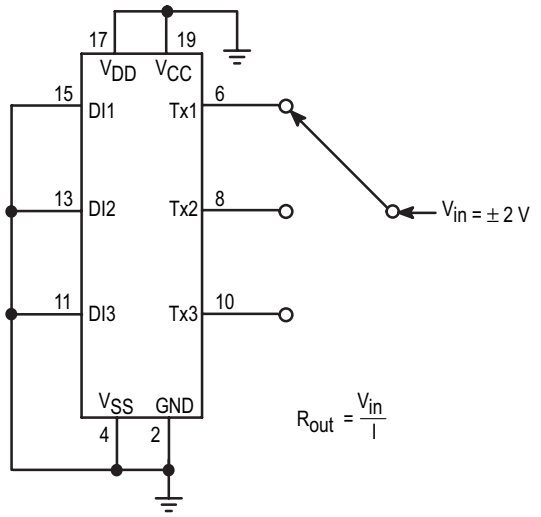


Figure 1. Power–Off Source Resistance

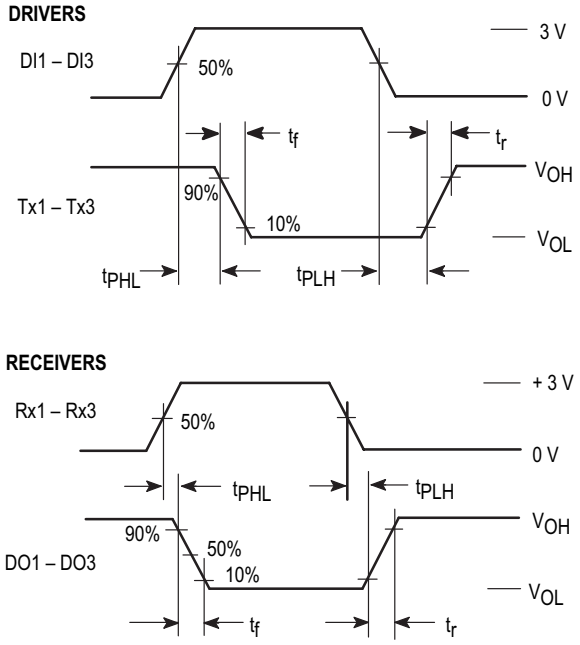


Figure 2. Switching Characteristics

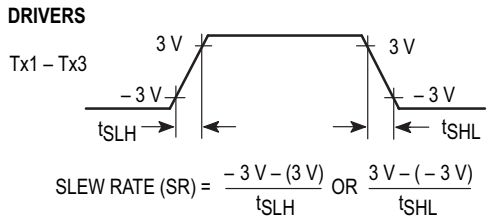


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply (Pin 19)

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND
Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply (Pin 17)

This is the positive output of the on–chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply (Pin 4)

This is the negative output of the on–chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2–, C1–, C1+
Voltage Doubler and Inverter (Pins 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the VDD and VSS voltages.

Rx1, Rx2, Rx3
Receive Data Input (Pins 5, 7, 9)

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to VCC.

DO1, DO2, DO3
Data Output (Pins 16, 14, 12)

These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 15, 13, 11)

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 6, 8, 10)

These are the EIA–232–E transmit signal output pins,which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD}. The actual levels and slew rate achieved will depend on the output loading (RL\\CL).

ESD CONSIDERATIONS

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply busses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 7 shows a technique which will clamp the ESD voltage at approximately + 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the 0.1 μF capacitors.

OPERATION WITH SMALLER VALUE CHARGE PUMP CAPS

The ML145407 is characterized in the electrical tables using 10 μF charge pump caps to illustrate its capability in driving a companion ML145406 or ML145403. If there is no requirement to support a second interface device and/or the charge pump is not being used to power any other components, the ML145407 is capable of complying with EIA–232–E and V.28 with smaller value charge pump caps.Table 1 summarizes driver performance with both 2.2 μF and1.0μF charge pump caps.

Table 1. Typical Performance

Parameter	2.2 μF	1.0 μF
Tx V_{OH} @ 25°C	7.3	7.2
Tx V_{OH} @ 85°C	7.2	7.1
Tx V_{OL} @ 25°C	– 6.5	– 6.4
Tx V_{OL} @ 85°C	– 6.1	– 6.0
Tx Slew Rate @ 25°C	8.0 V/μs	8.0 V/μs
Tx Slew Rate @ 85°C	7.0 V/μs	7.0 V/μs

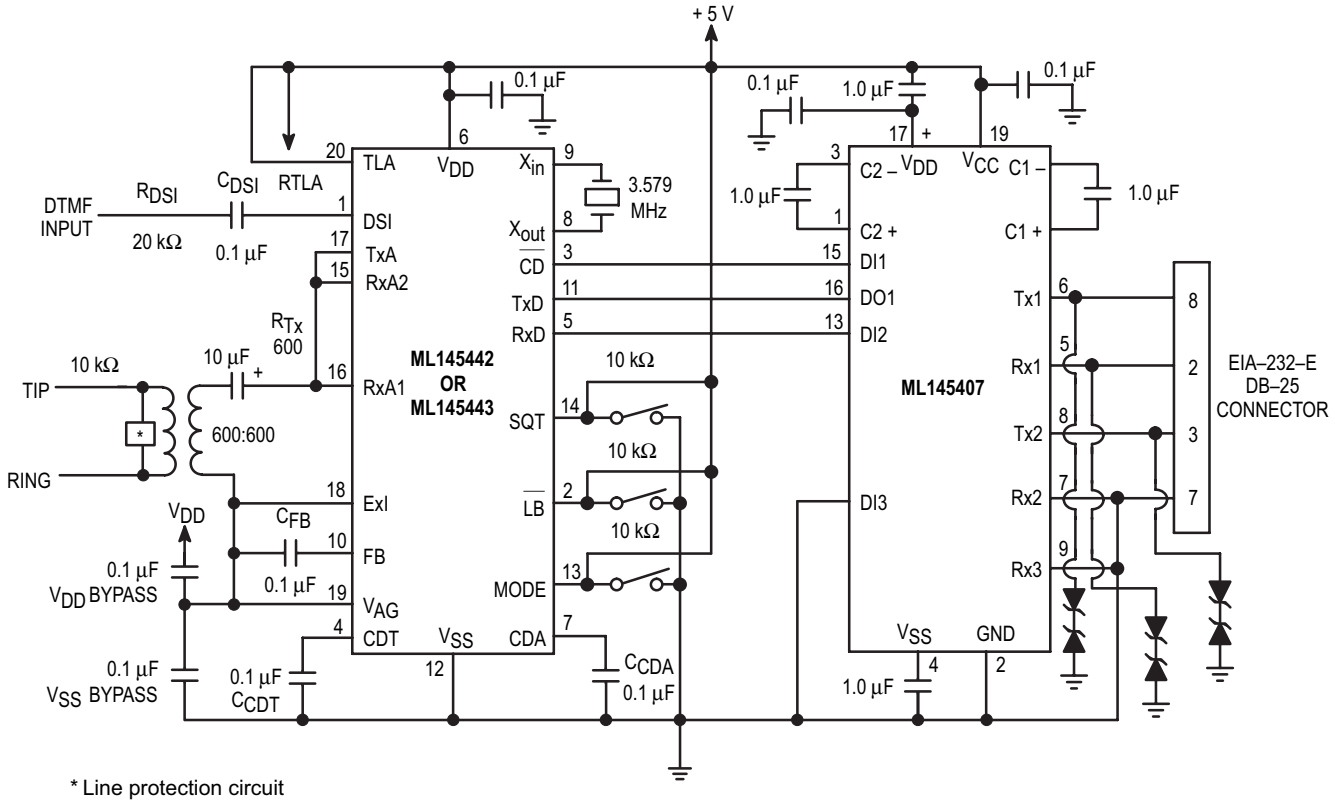


Figure 4. 5 V, 300 Baud Modem with EIA–232–E Interface

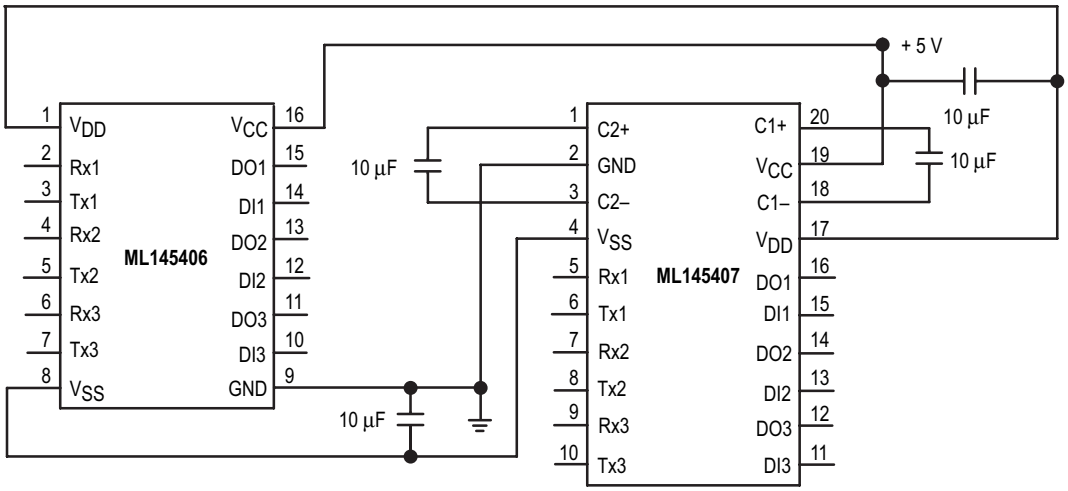


Figure 5. ML145406/ML145407 5 V Only Solution for up to Six EIA–232–E Drivers and Receivers

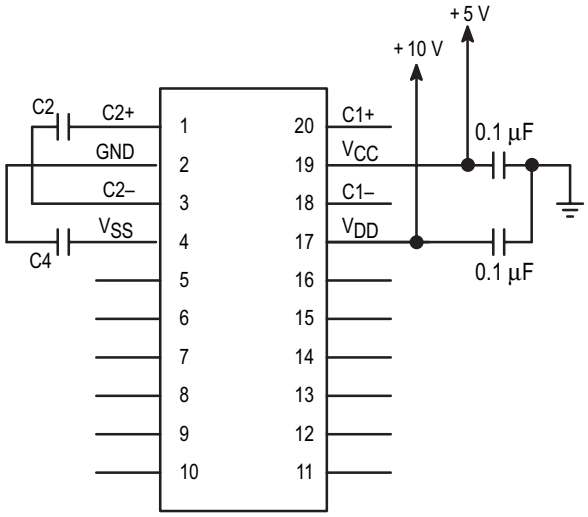


Figure 6. Two Supply Configuration (ML145407 Generates V_{SS} Only)

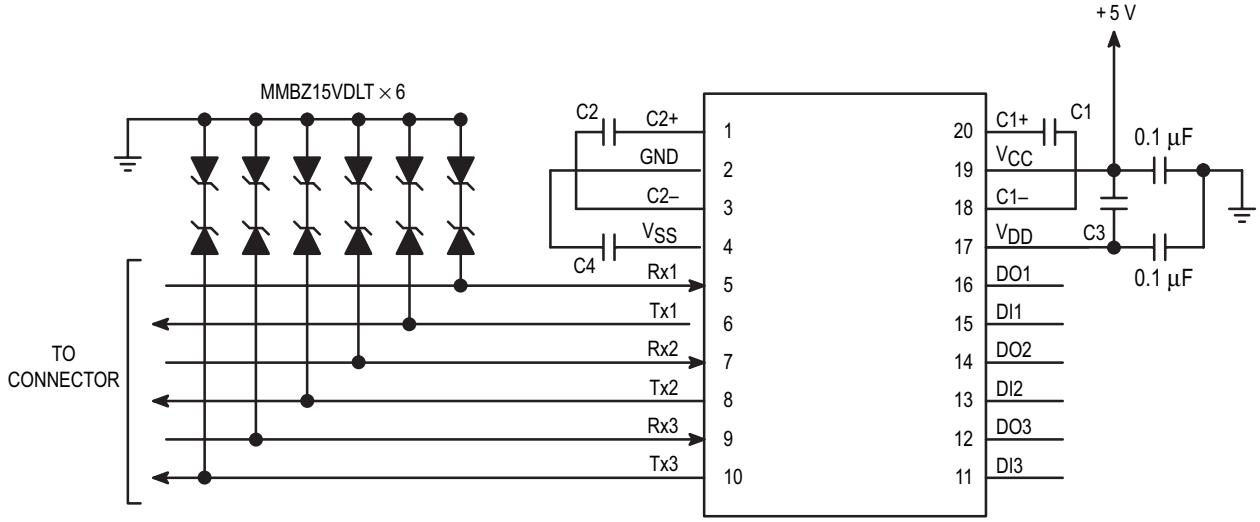
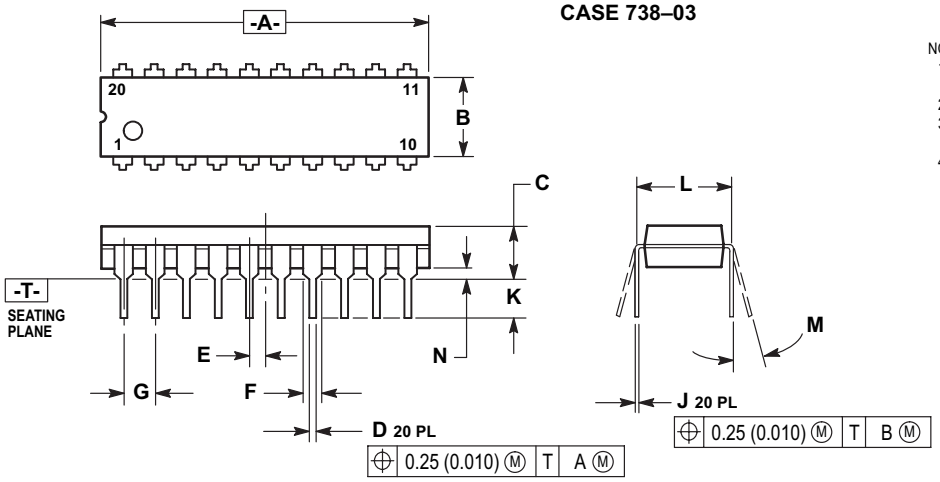


Figure 7. ESD Protection Scheme

OUTLINE DIMENSIONS

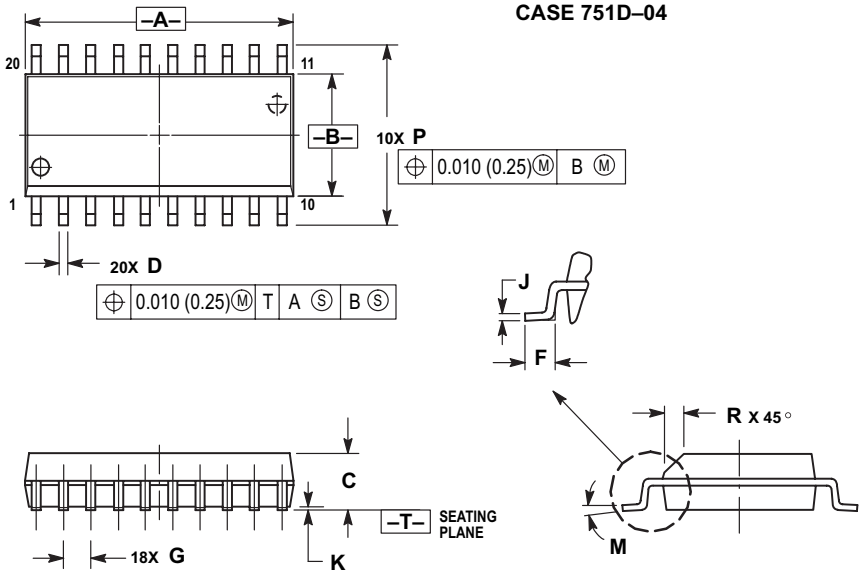
P DIP 20 = RP
(ML145407RP)
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOG 20 = -6P
(ML145407-6P)
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029