

*Version : 1.0*

<p>TECHNICAL SPECIFICATION</p> <p>MODEL NO. : PA040XS1</p>
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Customer's Confirmation

Customer \_\_\_\_\_

Date \_\_\_\_\_

By \_\_\_\_\_

PVI's Confirmation

Confirmed By \_\_\_\_\_

Prepared By \_\_\_\_\_

**FOR MORE INFORMATION:**  
AZ DISPLAYS, INC.  
75 COLUMBIA, ALISO VIEJO, CA, 92656  
[Http://www.AZDISPLAYS.com](http://www.AZDISPLAYS.com)

Date : Mar 10, 2005

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## 1. Application

This technical specification applies to 4" color TFT-LCD module , PA040XS1.

The applications of the panel are car TV, portable DVD, GPS, door phone, multimedia applications and others AV system..

## 2. Features

.Amorphous silicon TFT-LCD panel with B/L unit.

. Compatible with NTSC & PAL system

. Pixel in stripe configuration

. Slim and compact

. Image Reversion : Up/Down and Left/Right  
(With PVI timing controller : PVI-1004D)

## 3. Mechanical Specifications

<b>Parameter</b>	<b>Specifications</b>	<b>Unit</b>
Screen Size	4 (diagonal)	inch
Display Format	960×234	dot
Active Area	81.12(H)× 61.78(V)	mm
Dot Pitch	0.0845(H)× 0.264 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	96(W)× 75.98(H)× 6.2(D)(typ.)	mm
Surface Treatment	Anti – Glare	
Weight	74±5	g



**5. Input / Output Terminals**

TFT-LCD Module Connector

FPC Down Connect , 28Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	STH1	I/O	Start pulse for source driver	Note 5-1
2	AV <sub>SS</sub>	I	Analog GND for source driver	
3	AV <sub>DD</sub>	I	Analog power input for source driver	Note 5-3
4	V <sub>B</sub>	I	Video Input B	
5	V <sub>G</sub>	I	Video Input G	
6	V <sub>R</sub>	I	Video Input R	
7	V <sub>SS</sub>	I	Digital GND	
8	V <sub>DD</sub>	I	Digital power input	Note 5-4
9	CPH1	I	Sampling and shift clock for source driver	
10	CPH2	I	Sampling and shift clock for source driver	
11	CPH3	I	Sampling and shift clock for source driver	
12	STH2	I/O	Start pulse for source driver	Note 5-1
13	N/C	-	Not connector	
14	OE	I	Output enable for source driver	
15	R/L	I	Left/Right Control for source driver	Note 5-1
16	V <sub>COM</sub>	I	Common electrode voltage	Note 5-5
17	V <sub>COM</sub>	I	Common electrode voltage	
18	XOE	I	Output enable for gate driver	
19	CPV	I	Clock input for gate driver	
20	U/D	I	Up/Down Control for gate driver	Note 5-2
21	STVU	I/O	Vertical start pulse	
22	STVD	I/O	Vertical start pulse	
23	V <sub>GL</sub>	I	Gate off voltage(alternative every 1-H)	Note 5-6
24	N/C	-	Not connector	
25	V <sub>SS</sub>	I	GND	
26	V <sub>CC</sub>	I	Logic power for gate driver	Note 5-4
27	V <sub>GH</sub>	I	Gate on voltage	Note 5-7
28	GND	-	B/L case GND	

**Note 5-1**

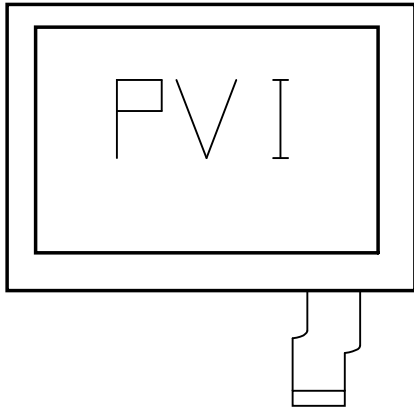
R/L	STH1	STH2	scanning direction
V <sub>CC</sub>	output	input	left to right
GND	input	output	right to left

### Note 5-2

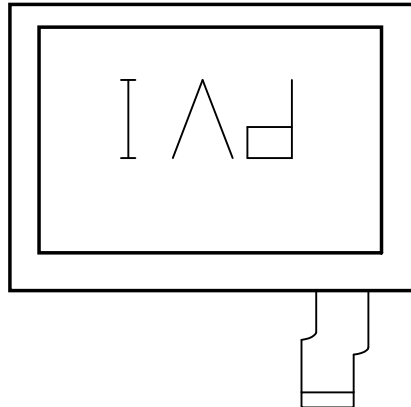
U/D	STVD	STVU	scanning direction
V <sub>CC</sub>	input	output	down to up
GND	output	input	up to down

The definitions of Note 5-1,5-2

U/D(PIN 12)=Low R/L(PIN 28)=High



U/D(PIN 12)=High R/L(PIN 28)=Low



Note 5-3 :  $AV_{DD} = +5V$  (Typ.)

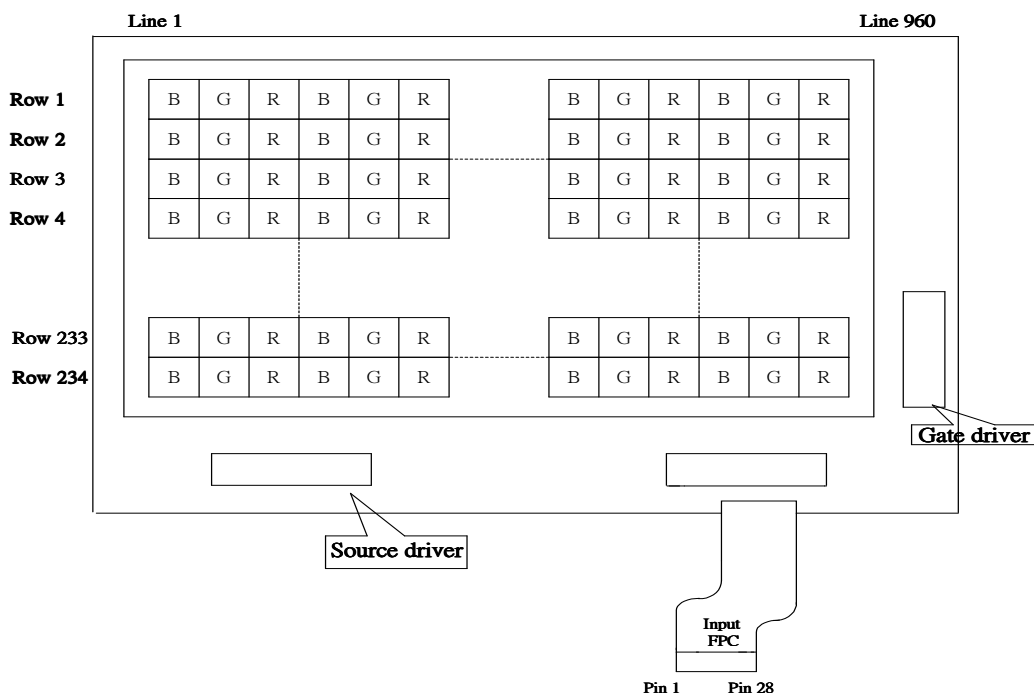
Note 5-4 :  $V_{DD}, V_{CC} = +3.3$  (Typ.)

Note 5-5 :  $V_{COM} = 6V_{PP}$ .

Note 5-6 :  $V_{GL} = -12V$  (Typ.).

Note 5-7 :  $V_{GH} = +17V$  (Typ.).

### 6. Pixel Arrangement and input connector pin NO.



**7. Absolute Maximum Ratings :**

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

$$GND = 0 V, T_a = 25 \text{ }^\circ\text{C}$$

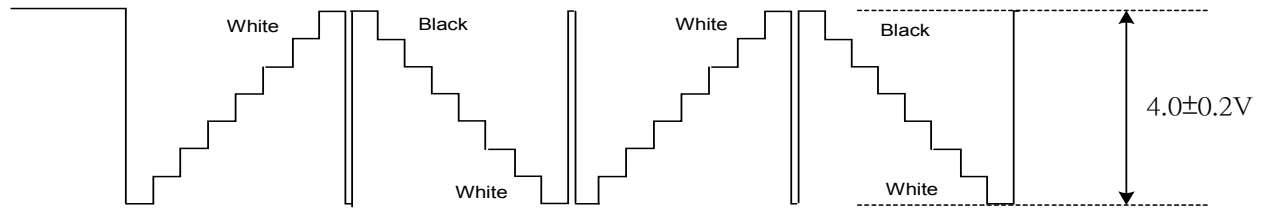
Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver	$AV_{DD}$	-0.3	+5.8	V	
	$V_{DD}$	-0.3	+7.0	V	
Supply Voltage For Gate Driver	$V_{CC}$	-0.3	+7.0	V	
	$V_{GH}-V_{GL}$	-0.3	+45.0	V	
	H Level $V_{GH}$	-0.3	+32.0	V	
	L Level $V_{GL}$	-22	+0.3	V	
Analog Signal Input Level	$V_R, V_G, V_B$	-0.2	$AV_{DD}+0.2$	V	
Operation Temperature		0	+60	$^\circ\text{C}$	
Storage Temperature		-30	+80	$^\circ\text{C}$	

**8. Electrical Characteristics**
**8-1) Operating Condition**

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	$AV_{DD}$	+4.5	+5.0	+5.5	V	
	Logic	$V_{DD}$	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H level	$V_{GH}$	+15	+17	+19	V	
	L level	$V_{GL DC}$	-13	-12	-10.5	V	DC Component of $V_{GL}$
		$V_{GL AC}$	-	+6.0	-	$V_{P-P}$	AC Component of $V_{GL}$
	Logic	$V_{CC}$	+3.0	+3.3	+3.6	V	
Video Signal ( $V_R, V_G, V_B$ )		$V_i AC$	-	+4.0	-	$V_{P-P}$	AC Component
		$V_i DC$	-	+2.5	-	V	DC Component
Digital input voltage	H level	$V_{IH}$	$0.7 V_{DD}$	-	$V_{DD}$	V	
	L level	$V_{IL}$	0	-	$0.3 V_{DD}$	V	
Digital output voltage	H level	$V_{OH}$	$V_{DD}-0.4$	-	$V_{DD}$	V	
	L level	$V_{OL}$	0	-	0.4	V	
$V_{COM}$		$V_{COM AC}$	-	+6.0	-	$V_{P-P}$	AC Component of $V_{COM}$
		$V_{COM DC}$		1.5		V	DC Component of $V_{COM}$ Note 8 -1

Note 8-1 : PVI strongly suggests that the  $V_{COM DC}$  level shall be adjustable , and the adjustable level range is  $1.5V \pm 1V$  , every module's  $V_{COM DC}$  level shall be carefully adjusted to show a best image performance.

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



8-2) Recommended driving condition for back light:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	$V_L$	290	316	345	Vrms	$I_L=5mA$
Lamp current	$I_L$	2.0	5.0	5.5	mA	
Lamp frequency	$P_L$	20	38	60	KHz	Note 8-3 $I_L=5mA$
Kick-off voltage(25°C)	$V_s$		480	530	Vrms	Note 8-4
Kick-off voltage(0°C)	$V_s$		560	615	Vrms	

Note 8-3 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-4 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 8-5 : The Kick-off times  $\geq 1$ sec.

Back Light Connector : JST BHSR-02VS-1, Pitch : 3.5 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 8-6

Note 8-6 : Low voltage side of back light inverter connects with Ground of inverter circuit.

8-3) Current Consumption (GND=0V)

$T_a = 25^\circ C$

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply current for Source Driver(Analog)	$I_{AVDD}$	$AV_{DD}=+5V$	7.0	10.0	mA	
Supply current for Source Driver(Digital)	$I_{VDD}$	$V_{DD}=+3.3V$	1.2	3.0	mA	
Supply current for Gate Driver (Low level)	$I_{GL}$	$V_{GL}=-12V$	0.3	0.45	mA	$V_{GL}$ center voltage
Supply current for Gate Driver (Digital)	$I_{CC}$	$V_{CC}=+3.3V$	0.03	0.05	mA	
Supply current for Gate Driver (Hi level)	$I_{GH}$	$V_{GH}=+17V$	0.2	0.5	mA	
LCD Panel Power Consumption			45	70	mW	Note 8-7
Back Light Lamp Power Consumption			1.58	1.725	W	Note 8-8 $I_L=5mA$
Total Power Consumption			1.625	1.795	W	

Note 8-7 : The power consumption for back light is not included.

Note 8-8 : Backlight lamp power consumption is calculated by  $I_L \times V_L$ .



**8-4) Timing Characteristics Of Input Signals**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	$t_r$	-	-	10	ns	
Falling time	$t_f$	-	-	10	ns	
High and low level pulse width	$t_{CPH}$	147	156	166	ns	CPH1
CPH pulse duty	$t_{CWH}$	30	50	70	%	CPH1
STH setup time	$t_{SUH}$	20	-	-	ns	STH1,STH2
STH hold time	$t_{HDH}$	20	-	-	ns	STH1,STH2
STH pulse width	$t_{STH}$	-	1	-	$t_{CPH}$	STH1,STH2
STH period	$t_H$	61.5	63.5	65.5	$\mu s$	STH1,STH2
OEH pulse width	$t_{OEH}$	-	1.6	-	$\mu s$	OEH
Sample and hold disable time	$t_{DIS1}$	-	4.4	-	$\mu s$	
OEV pulse width	$t_{OEV}$	-	12	-	$\mu s$	OEV
CKV pulse width	$t_{CKV}$	-	32	-	$\mu s$	CPV
Clean enable time	$t_{DIS2}$	-	6	-	$\mu s$	
Horizontal display timing range	$t_{DH}$	-	320	-	$t_{CPH}/3$	
STV setup time	$t_{SUV}$	400	-	-	ns	STVU,STVD
STV hold time	$t_{HDV}$	400	-	-	ns	STVU,STVD
STV pulse width	$t_{STV}$	-	-	1	$t_H$	
Horizontal lines per field	$t_V$	256	262	268	$t_H$	
Vertical display start	$t_{SV}$		3	-	$t_H$	
Vertical display timing range	$t_{DV}$		234	-	$t_H$	
VCOM rising time	$t_{rCOM}$		-	5	$\mu s$	
VCOM falling time	$t_{fCOM}$		-	5	$\mu s$	
VCOM delay time	$t_{DCOM}$		-	3	$\mu s$	
RGB delay time	$t_{DRGB}$		-	1	$\mu s$	

8-5) Signal Timing Waveforms

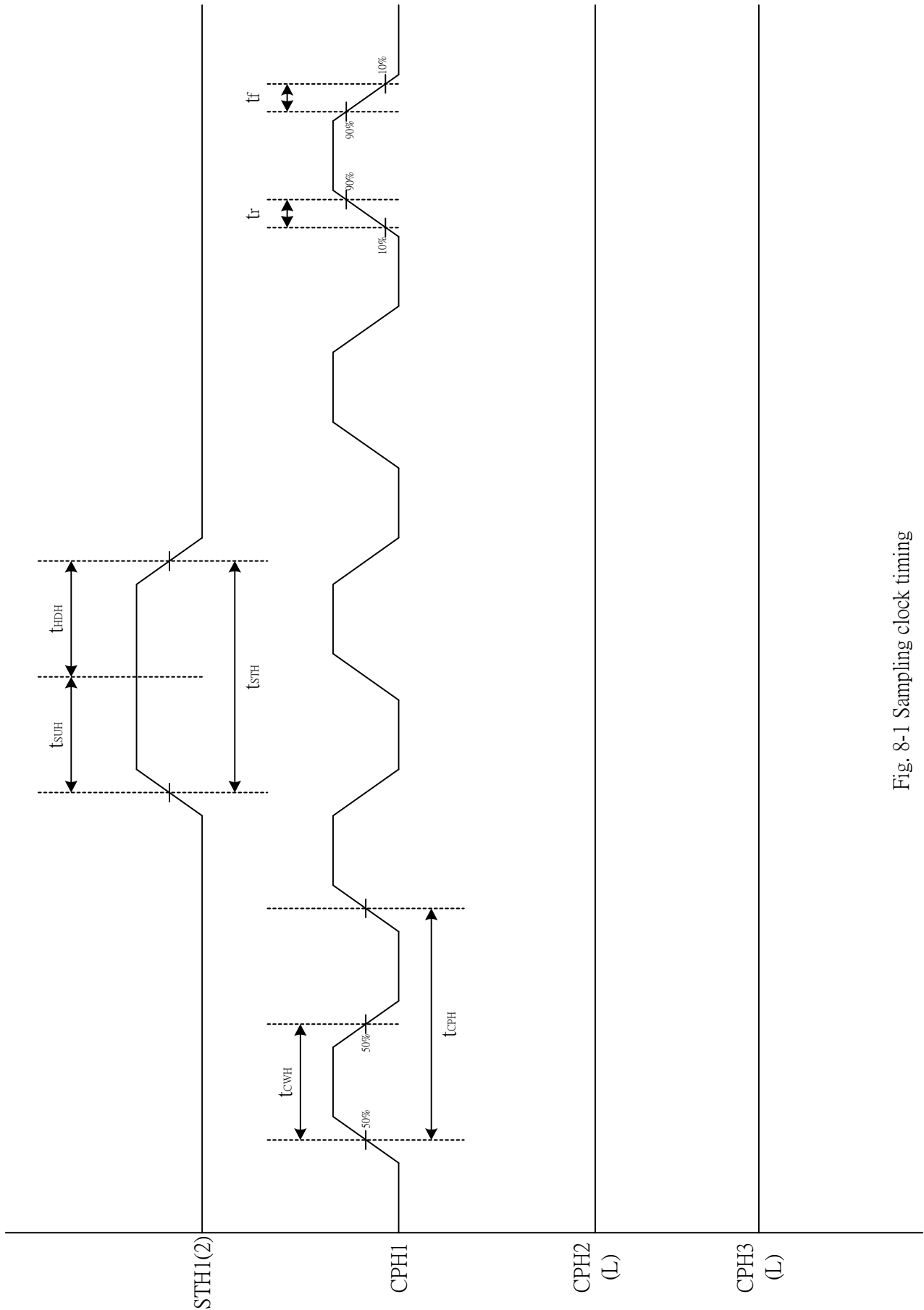


Fig. 8-1 Sampling clock timing

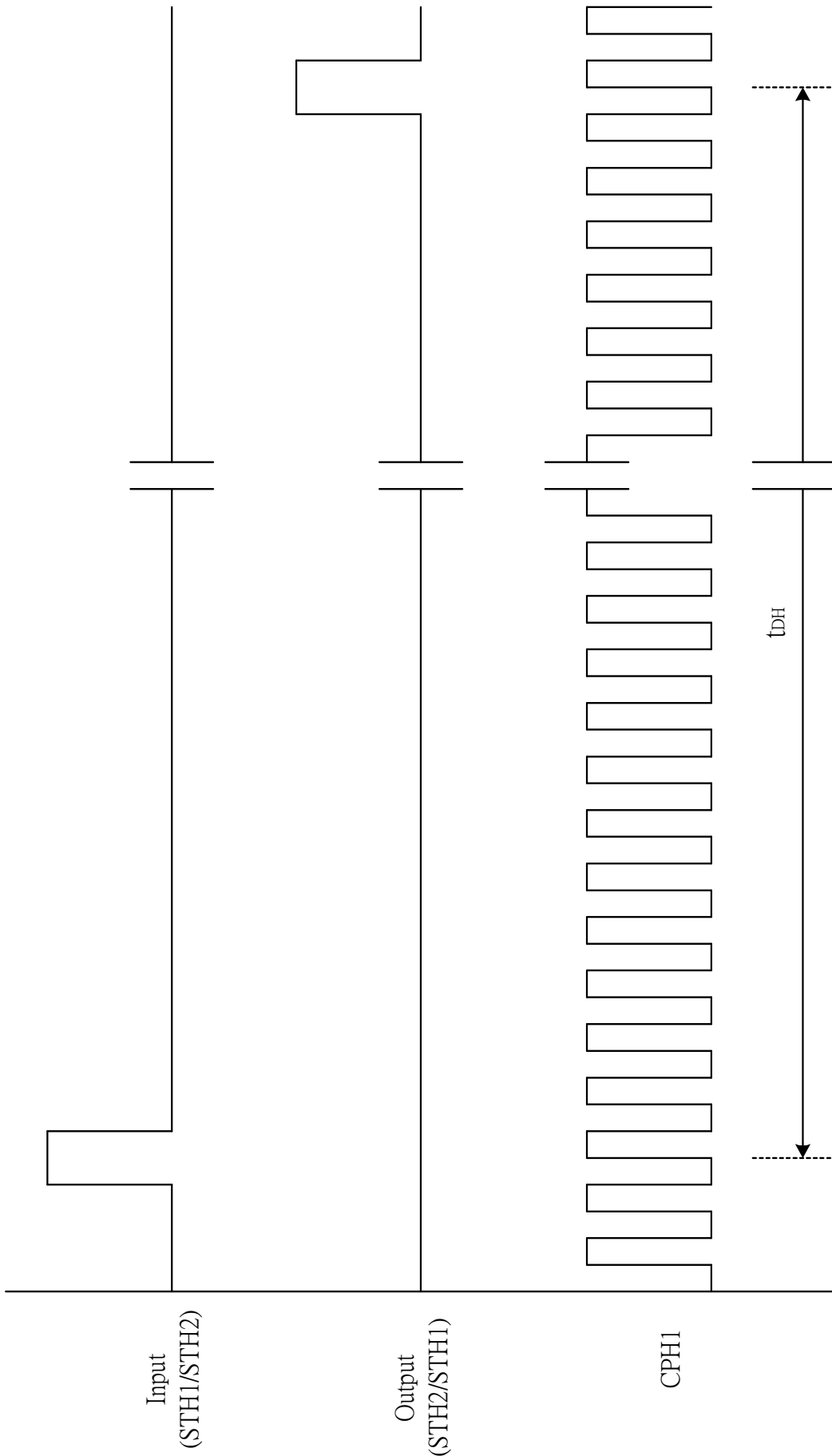


Fig. 8-2 Horizontal display timing range

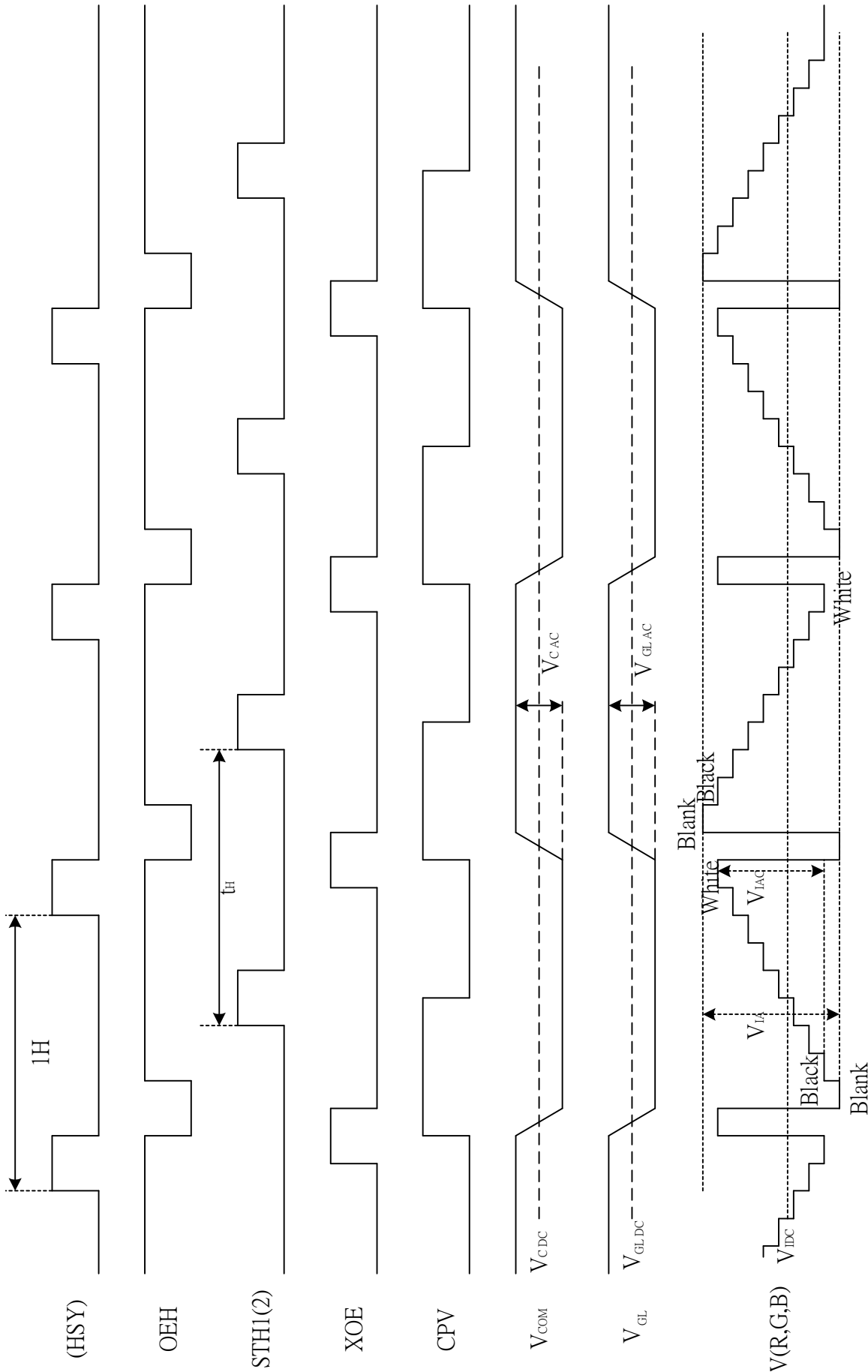
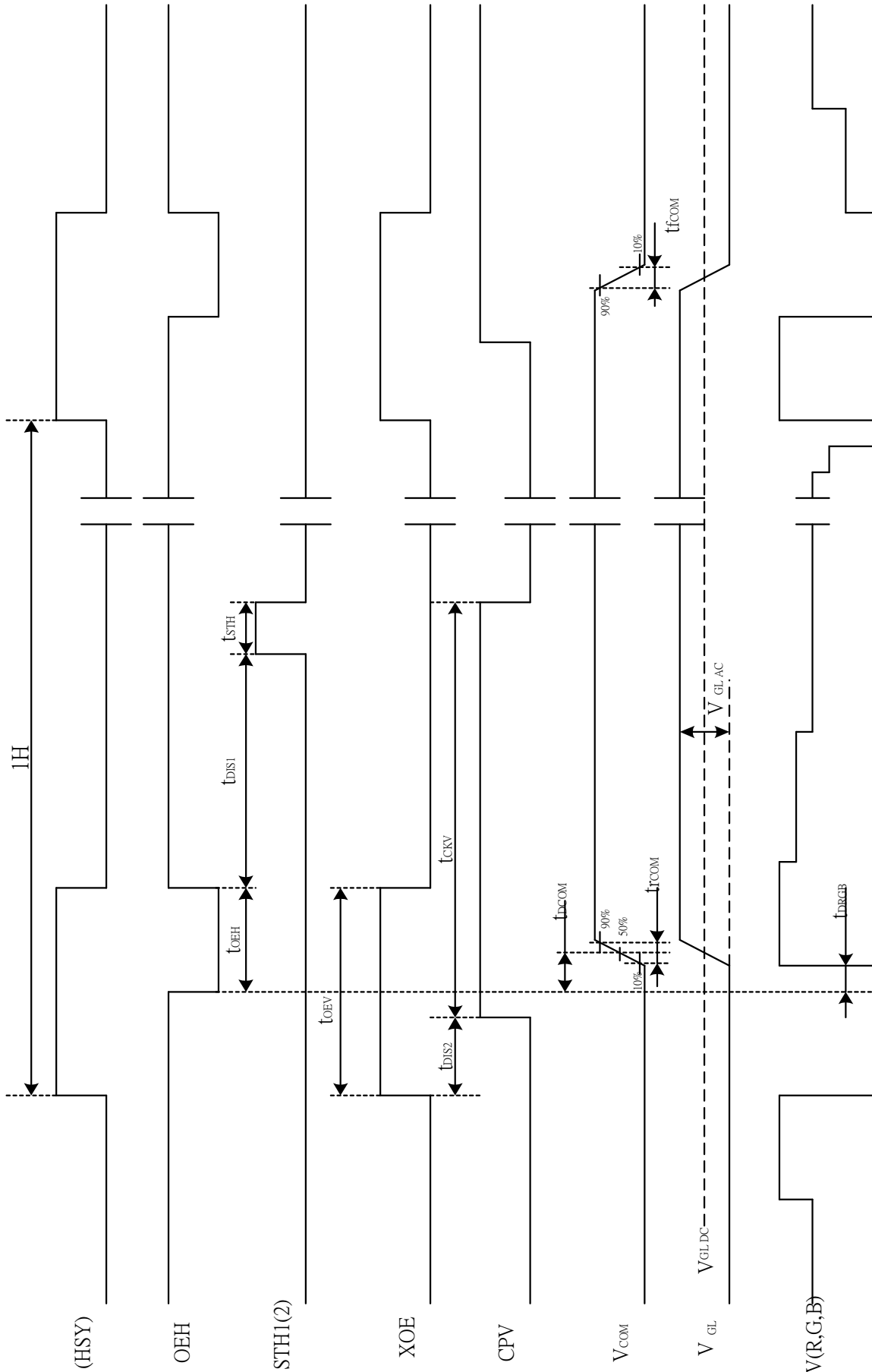


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEH should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

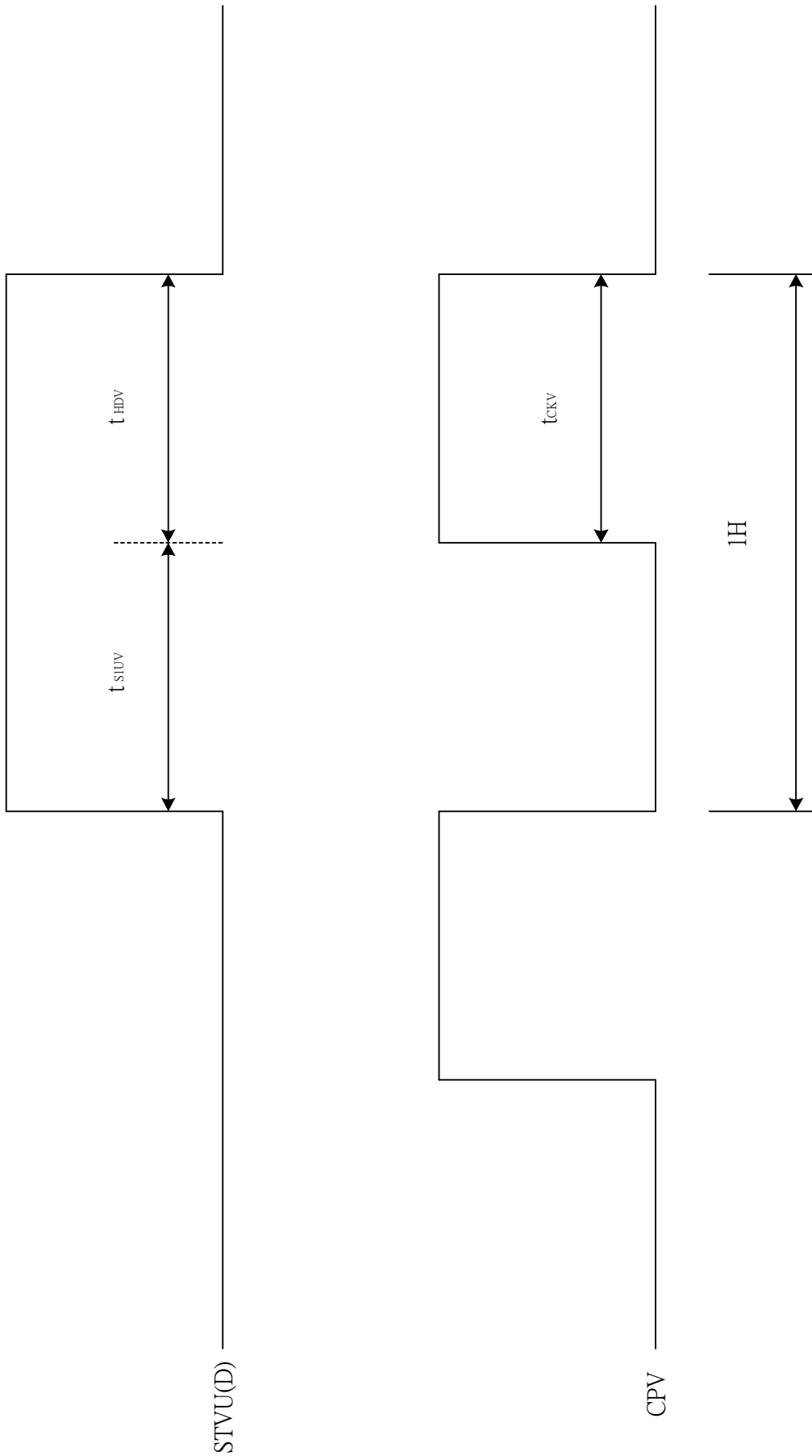


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

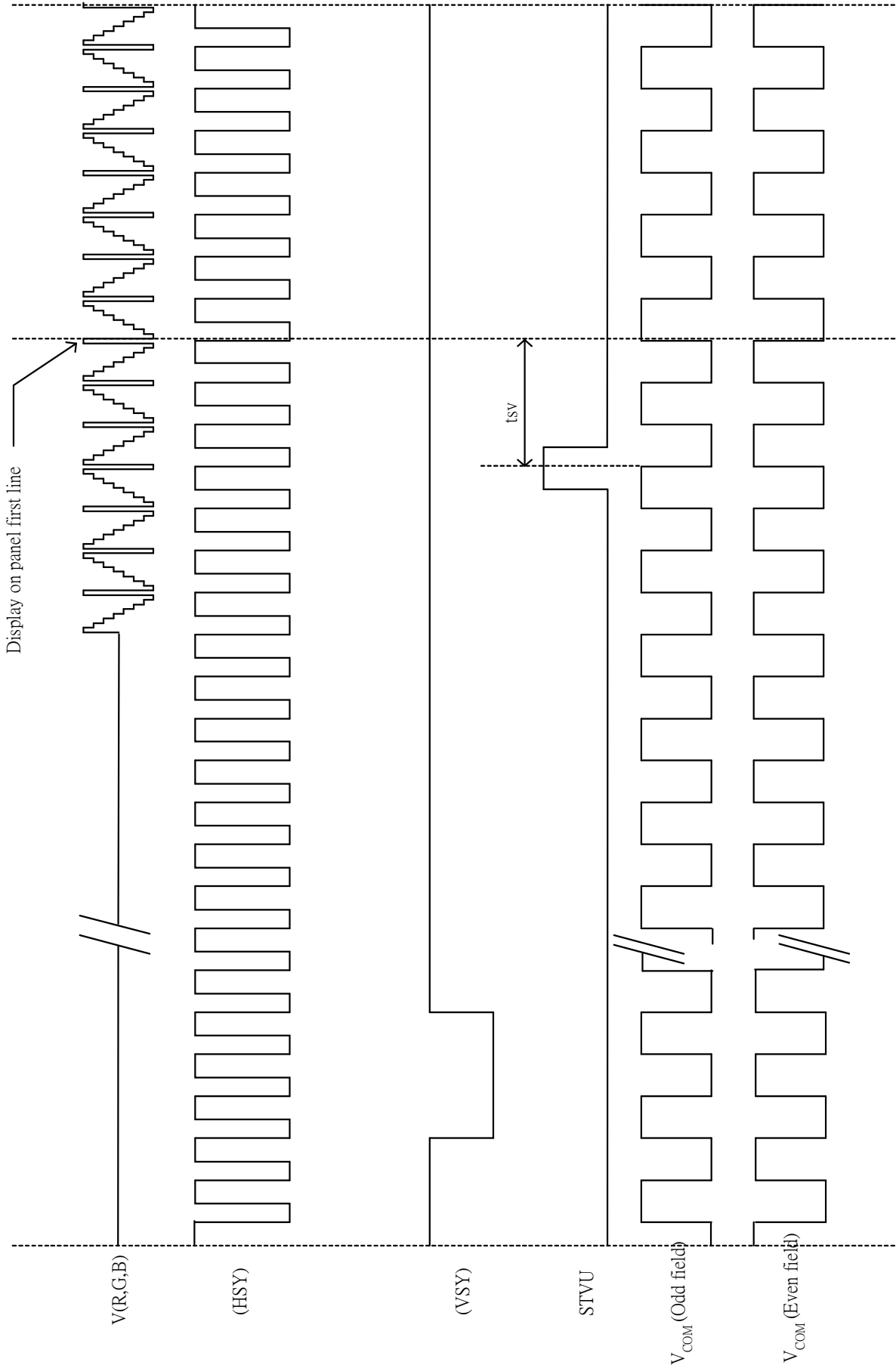


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

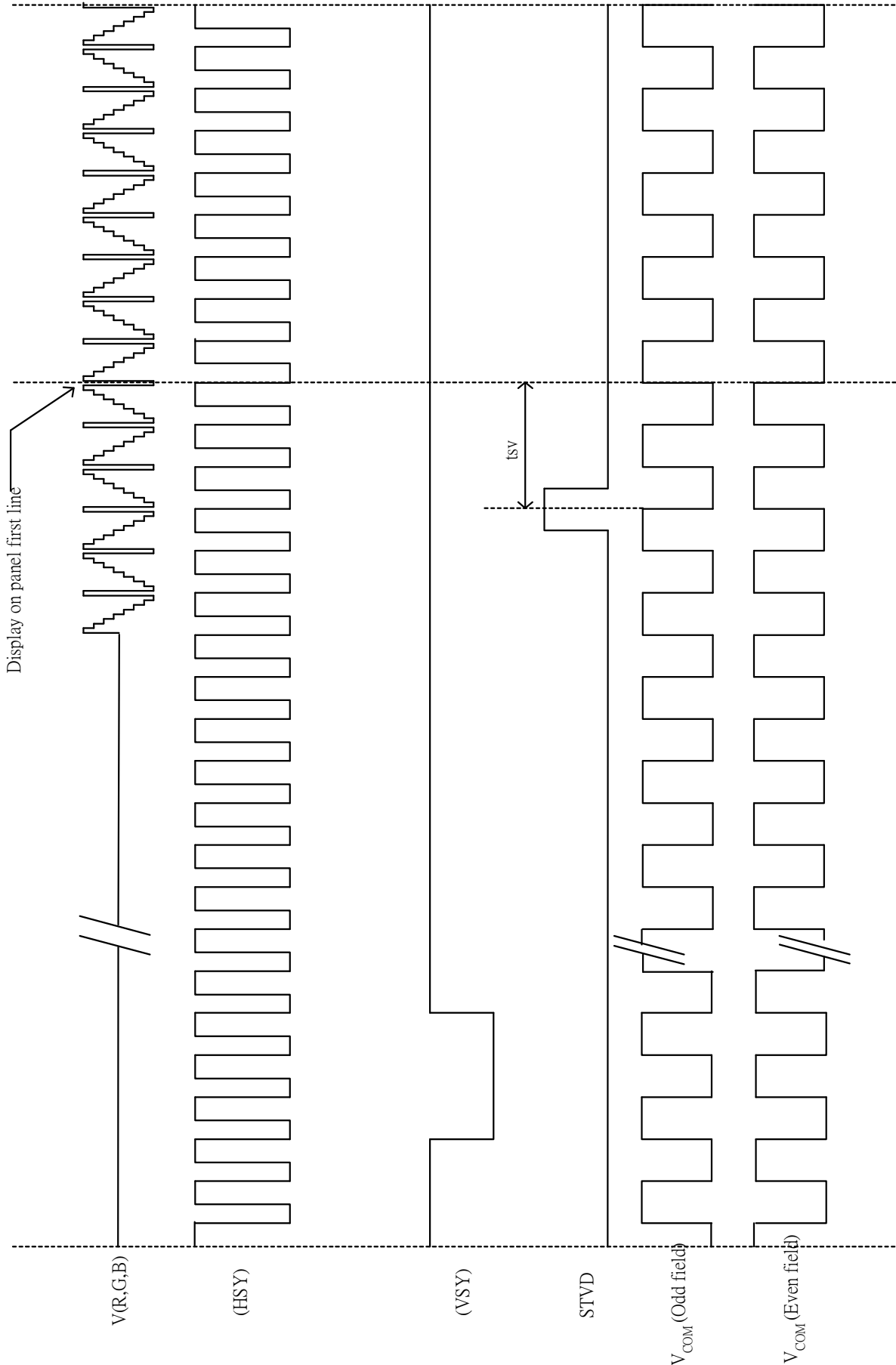
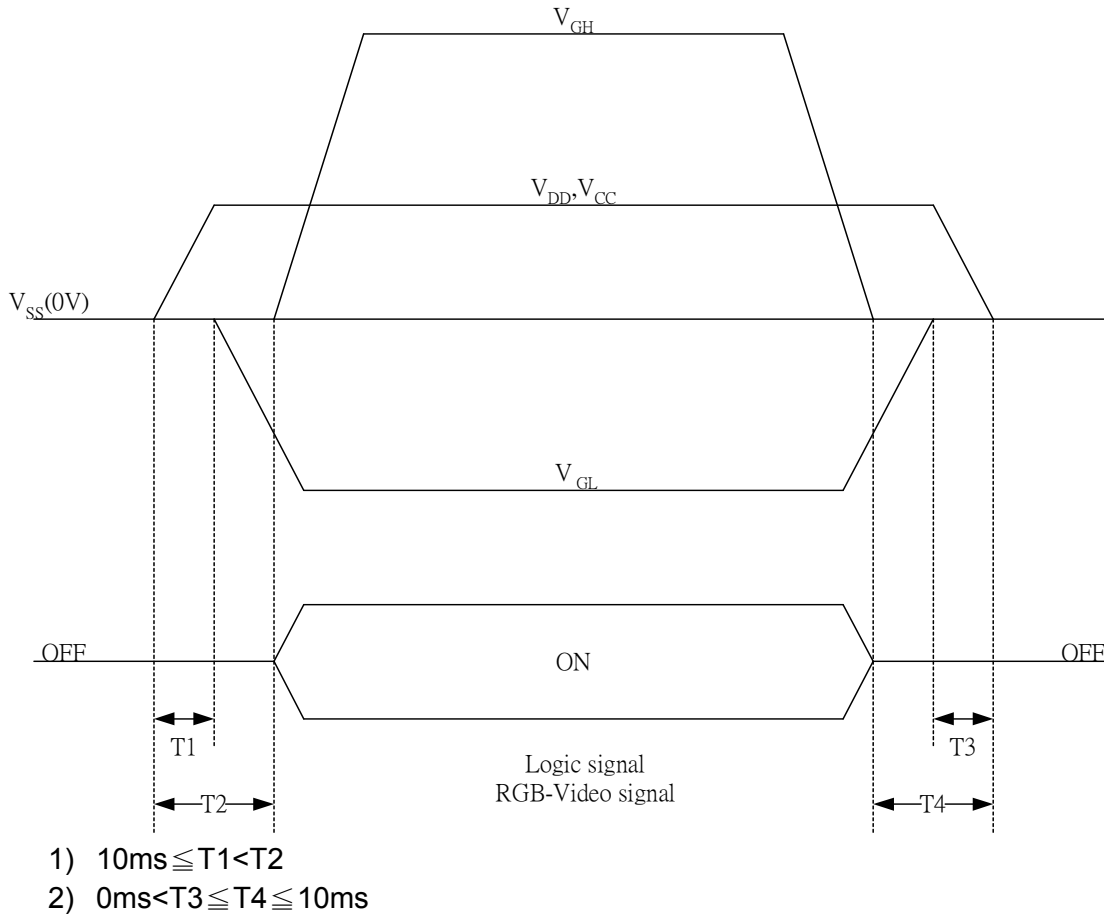


Fig. 8-5 (b) Vertical timing (From Down to Up)



9. Power On Sequence

The Power on Sequence only effect by  $V_{CC}, V_{SS}, V_{DD}, V_{GL}$  and  $V_{GH}$ , the others do not care.



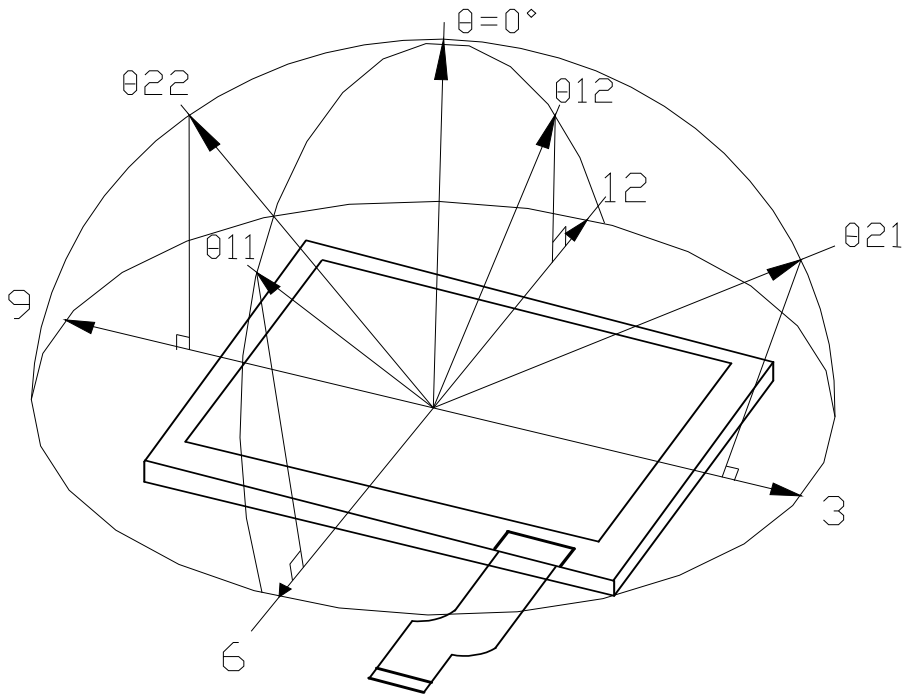
10. Optical Characteristics

10-1) Specification:

$T_a = 25^\circ C$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
Viewing Angle	Horizontal	$CR \geq 10$	45	50	---	deg	Note 10-1	
	Vertical		$\theta 11$	30	35	---		deg
			$\theta 12$	10	15	---		deg
Contrast Ratio	CR	At optimized Viewing angle	200	350	---		Note 10-2	
Response time	Rise	$\theta = 0^\circ$	---	15	30	ms	Note 10-4	
	Fall		---	25	50	ms		
Uniformity	U		70	80	---	%	Note 10-5	
Brightness			300	350	---	cd/m <sup>2</sup>	Note 10-3	
White	x	$\theta = 0^\circ$	0.28	0.31	0.34			
Chromaticity	y	$\theta = 0^\circ$	0.30	0.33	0.36			
Lamp Life Time		$+25^\circ C$	---	10000	---	Hr		

Note 10-1 : The definitions of viewing angles



Note 10-2 :  $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

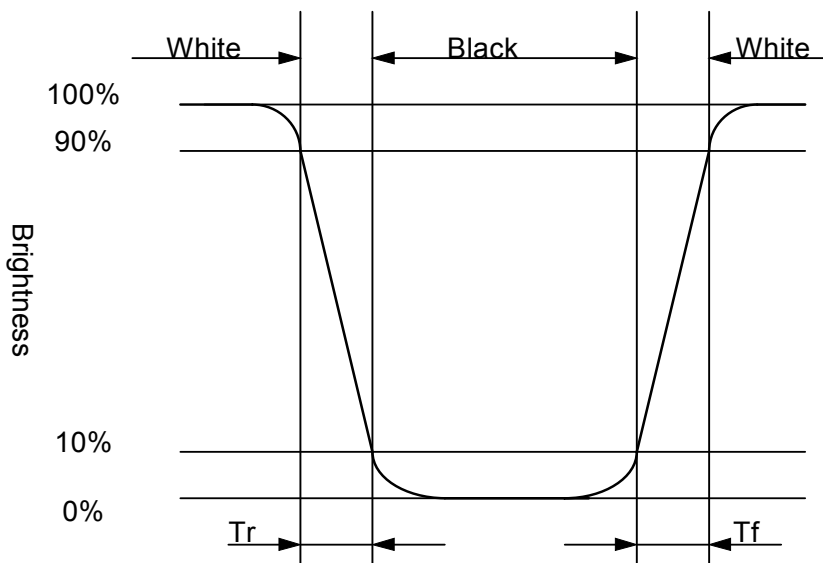
(Testing configuration see 10-2 )

Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 5mA

Note 10-4 : The definition of response time :



Note 10-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

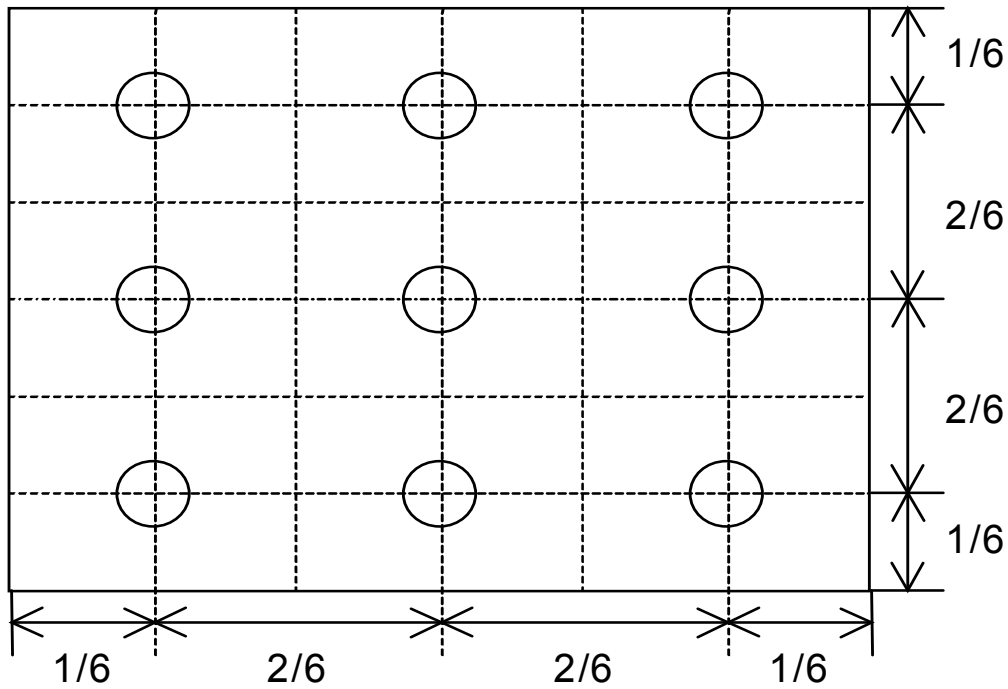
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

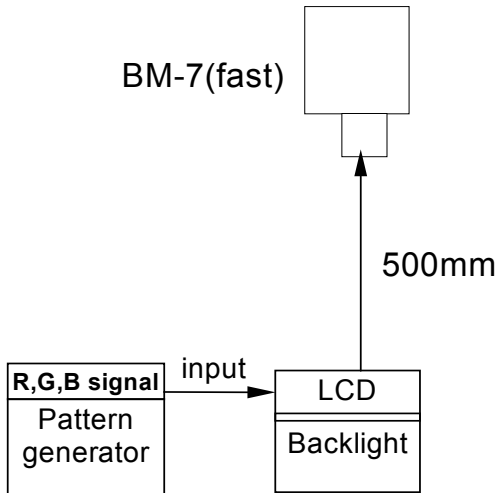
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

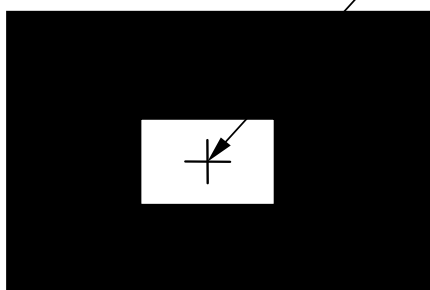


10-2) Testing configuration

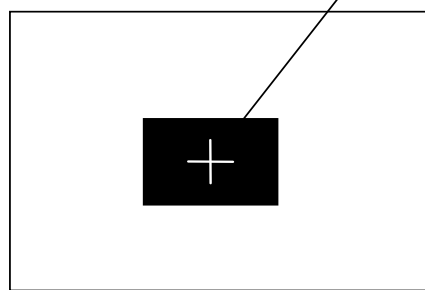


Caution: 1. Environmental illumination  $\leq 1$  lux  
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display

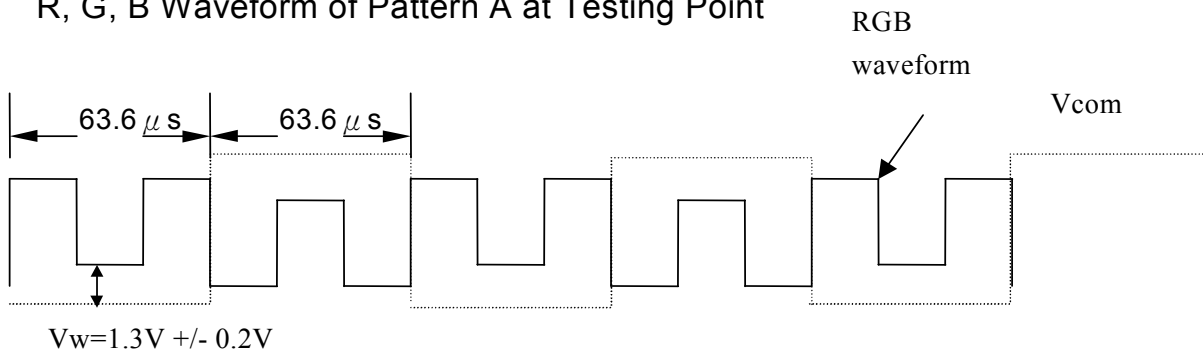


Pattern A

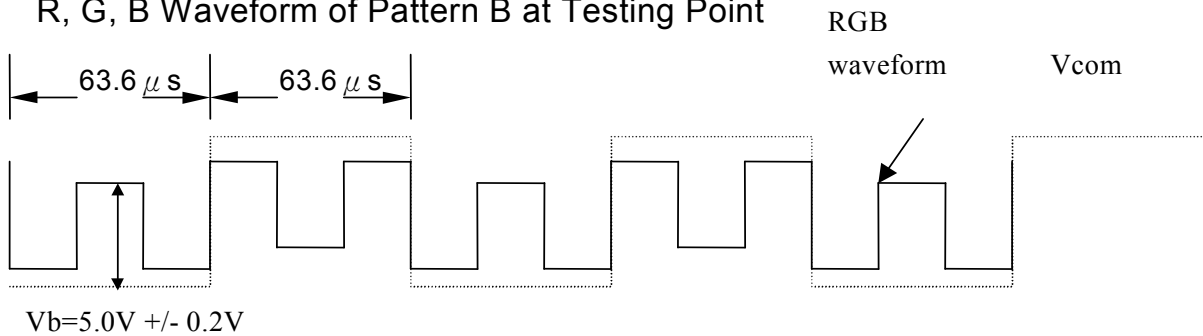


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



**11. Handling Cautions****11-1) Mounting of module**

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
  - 1. The noise from the backlight unit will increase.
  - 2. The output from inverter circuit will be unstable.
  - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

**11-2) Precautions in mounting**

- a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

**11-3) Others**

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.

## 12. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80°C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	Low Temperature Operation Test	Ta = 0°C, 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs
5	Thermal Cycling Test (non-operating)	-20°C → +70°C, 200 Cycles 30 min 30 min
6	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.5 mm Sweep time: 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
7	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
8	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

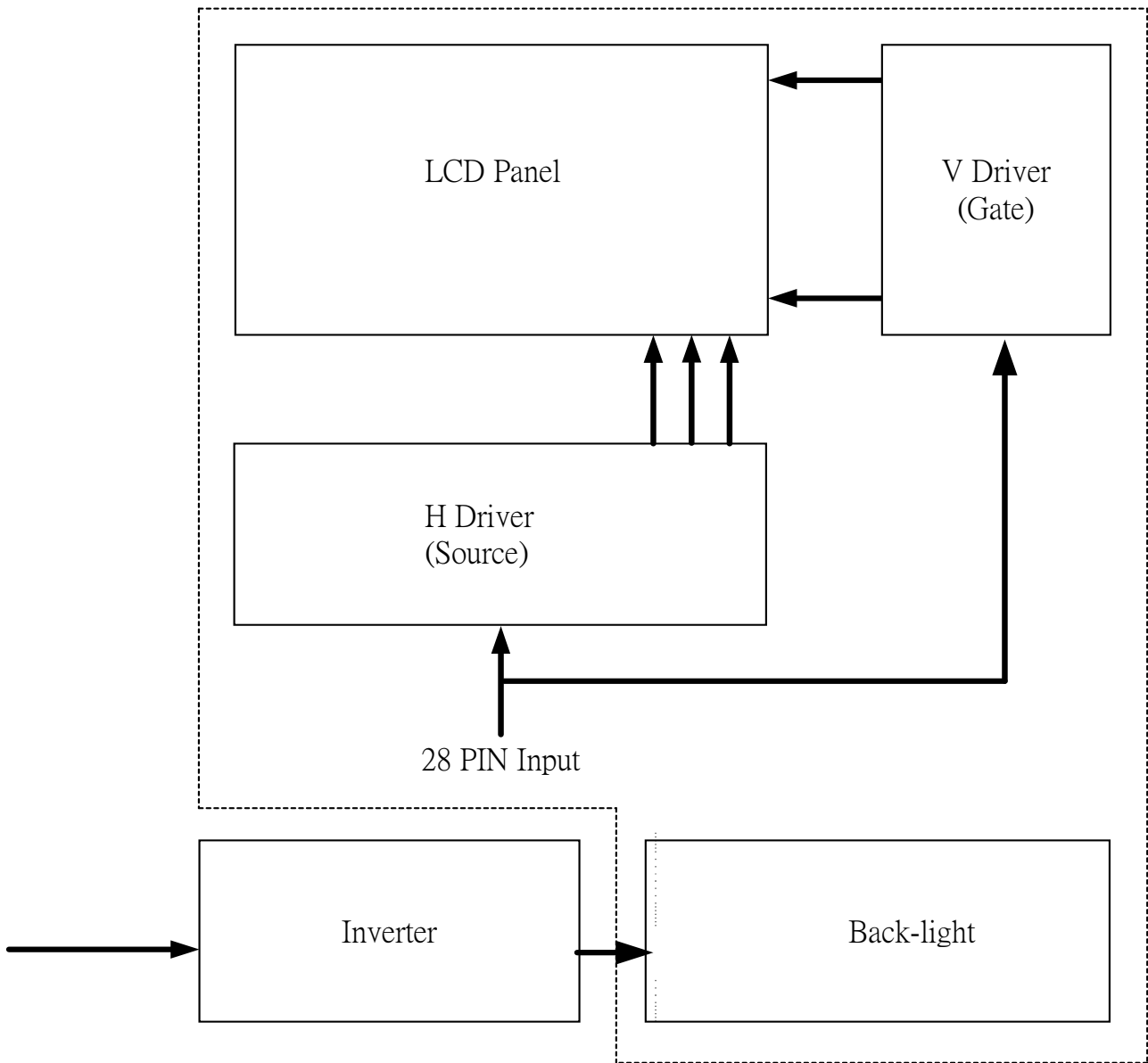
Ta: ambient temperature

Note : The protective film must be removed before temperature test.

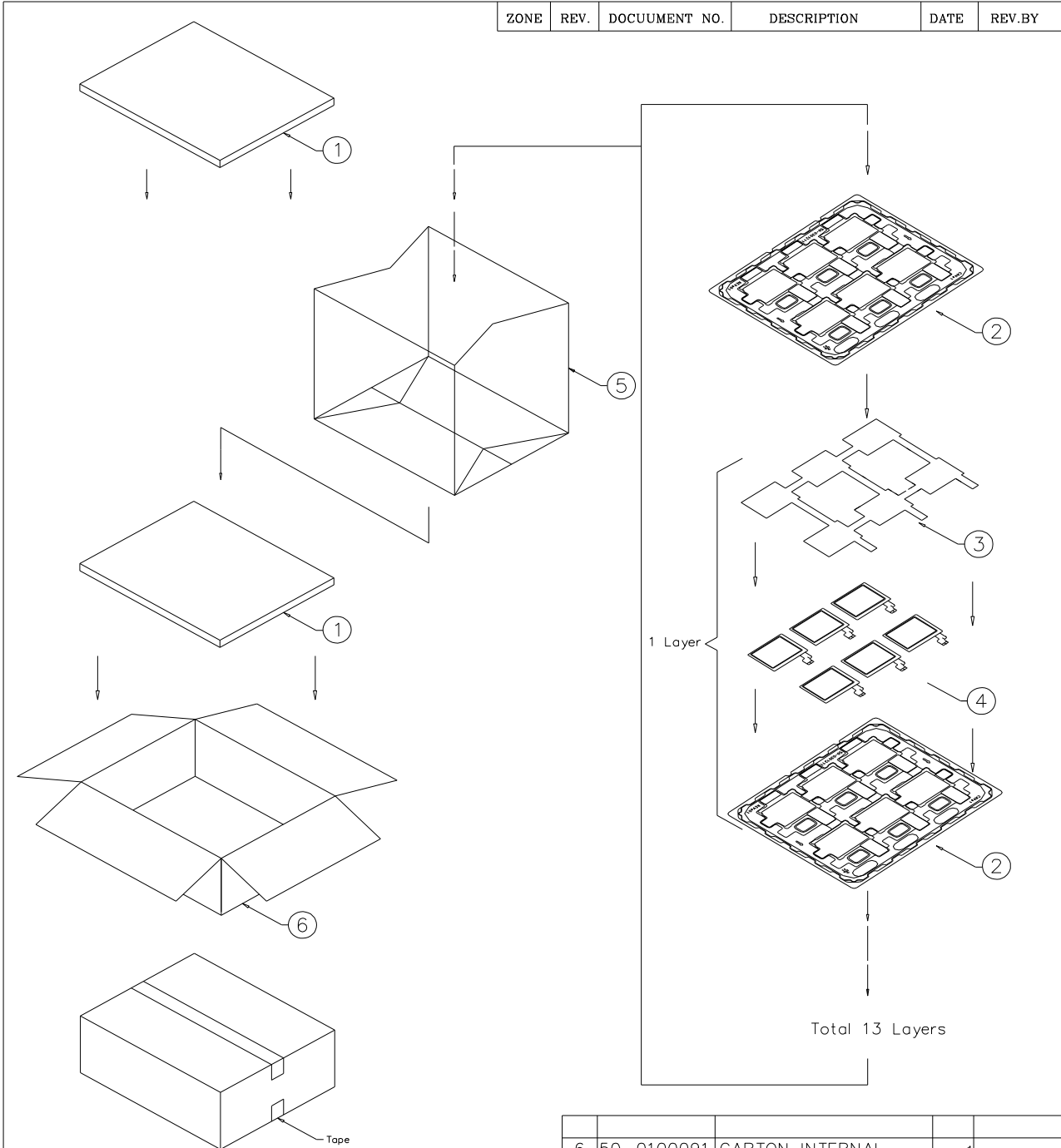
[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



14. Packing



**NOTE:**

1. One layer include: 1 piece of cushion sheet, 6 pcs panel & 1 piece of tray.
2. Q'TY: 42 pcs panel/carton.
3. Dimension: 455\*375\*190mm
4. Weight: 5.3 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PA040XS1	42	
3	50-0200061	EPE CUSHION SHEET	7	抗靜電
2	50-0301211	TRAY	8	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.		UNSPECIFIED TOL'S		REMARK		<b>元太科技股份有限公司</b> Prime View International Co.,Ltd.	
		ANGLE					
		ROUGHNESS				DWG.TITLE	
APPROVE		SCALE	UNIT	SHEET	PA040XS1 PACKING Dim		
CHECK				1 OF 2			
DESIGN	David	'05.03.10		MTL.NO.	DWG.NO.	REV. 01	A4 SIZE



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### Revision History

Rev.	Issued	Date	Revised	Contents
1.0		Mar 10 , 2005	New	