普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT8214 is an 8-bit D/A Converter IC with operational amplifier output buffers. It supports up to a maximum of 36 channels and provides two reference voltages which enable its 36 channels to be used as 12 and 24 independent channels. Digital data are inputted in serially and is controlled by the CLK and STB Pins making a cascading connection between devices. Available in 48 pins, LQFP package, PT8214 is capable of large current drive since each channel has an operational amplifier output buffer. Pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS technology
- Very low power consumption: Type 1.1mW/channel
- Max. 2.5MHz serial data input
- Separate supply voltages for digital and analog blocks
- R-2R resistor ladder conversion method
- On-chip operational amplifier output buffers: Max. +1.0/-1.0mA analog output sink/source current capability
- Analog data output range: 0 to Vcc (V)
- Two analog output reference voltage
- Analog data can be outputted in different reference voltages
- Available in 48 pins, LQFP package

APPLICATIONS

- Digital equipment
- V8
- CD ROM/VCD
- MPEG
- Sound card
- Replacement for potentiometers

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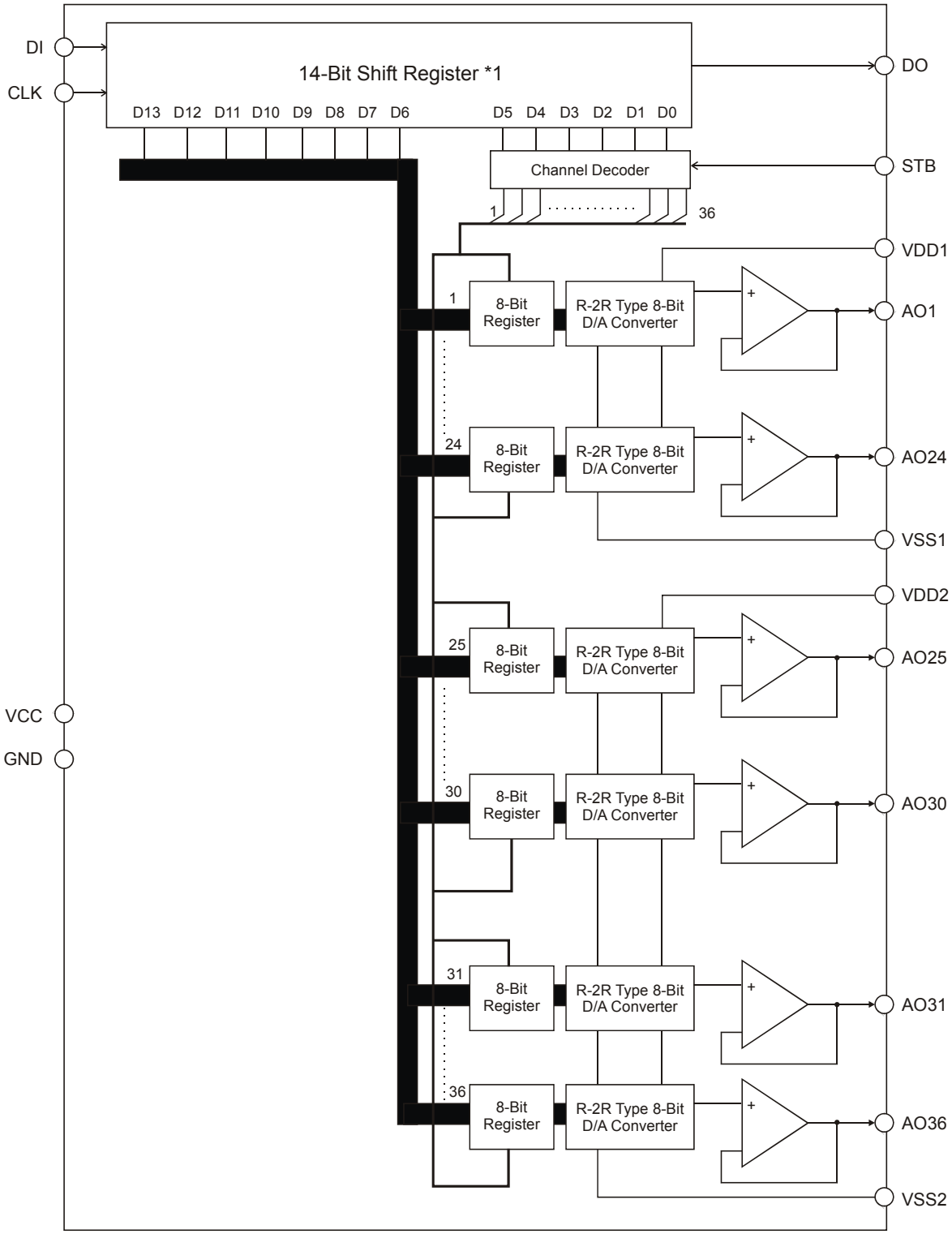
BLOCK DIAGRAM



Note: *1=14-Bit Shift Register with an MSB-First format.

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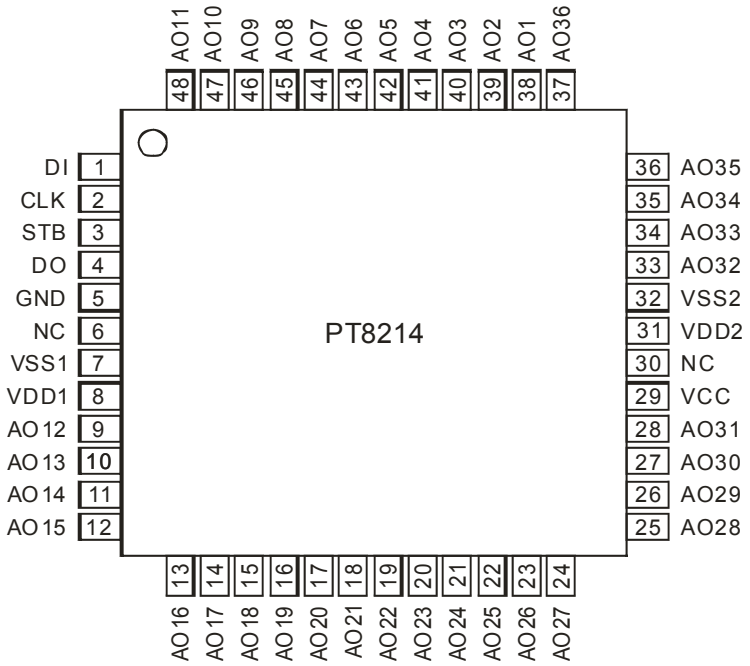
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
DI*	I	Serial data input pin	1
CLK*	I	Shift clock input pin Serial data input from the DI pin are inputted to the internal shift register at the rising edge of the CLK signal.	2
STB*	I	Load strobe input pin When this pin is “High”, the shift register contents are loaded into the decoder and 8-bit register.	3
DO	O	Serial data output pin The serial data in the shift register are outputted from this pin. This pin allows a cascade connection.	4
GND	-	Ground	5
NC	-	No connection	6, 30
VSS1	-	D/A converter ground pin (for AO1 to AO24 outputs)	7
VDD1	-	D/A converter supply voltage (for AO1 to AO24 outputs)	7
AO12 to AO24	O	D/A converter output pin #1	9 to 21
AO25 to AO27	O	D/A converter output pin #2	22 to 24
AO28 to AO31	O	D/A converter output pin #2	25 to 28
VCC	-	Digital block & operational amplifier output buffer supply voltage (for AO25 to AO36 outputs)	29
VSS2	-	D/A converter ground pin (for AO25 to AO36 outputs)	32
AO32 to AO36	O	D/A converter output pin #2	33 to 37
AO1 to AO11	O	D/A converter output pin #1	38 to 48

Note: *=DI, CLK & STB must be fixed at low level when there is no data transfer.

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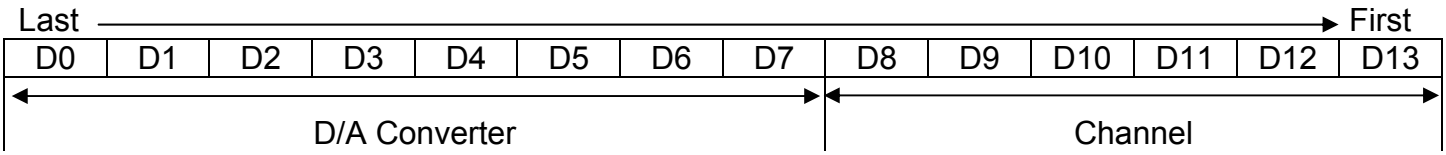
FUNCTION DESCRIPTION

PT8214 is an 8-bit D/A Converter IC which provides 14 bits shift register for digital data storage and channel selection. The 14 bits shift register are shown below.



The D/A converter output are given in the table below.

Input data								
D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	$\cong V_{SS}$
1	0	0	0	0	0	0	0	$\cong VREF/256x1+V_{SS}$
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$\cong VREF/256x254+V_{SS}$
1	1	1	1	1	1	1	1	$\cong VREF/256x255+V_{SS}$

Note: $VREF=VDD-V_{SS}$

The channel selection table is given below.

Input data						
D8	D9	D10	D11	D12	D13	Selected channel
0	0	0	0	0	0	Not selected
0	0	0	0	0	1	AO1 to AO30 selected
0	1	1	1	1	0	
0	1	1	1	1	1	AO31 to AO36 selected
1	0	0	1	0	0	
1	0	0	1	0	1	Not selected
1	1	1	1	1	1	

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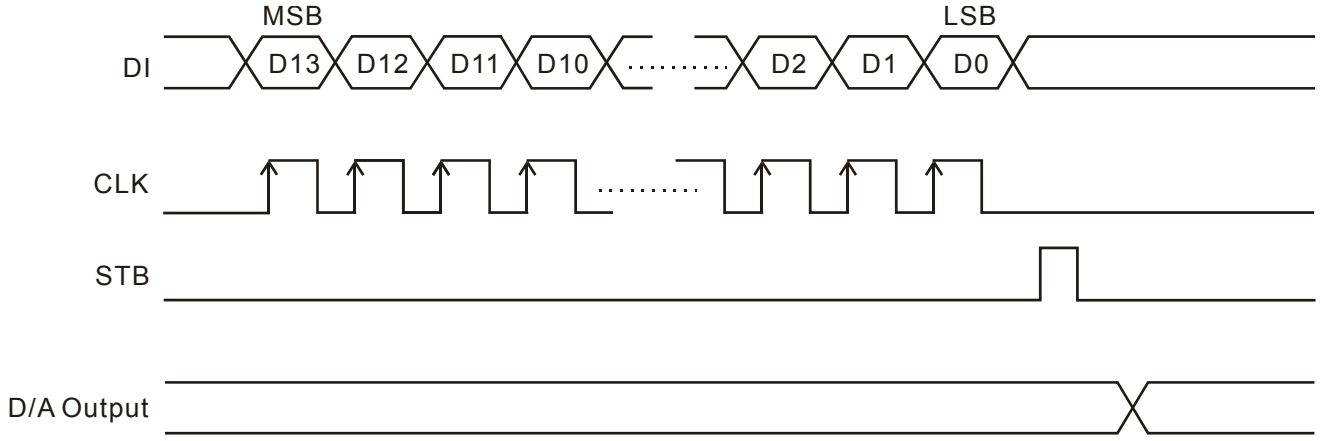
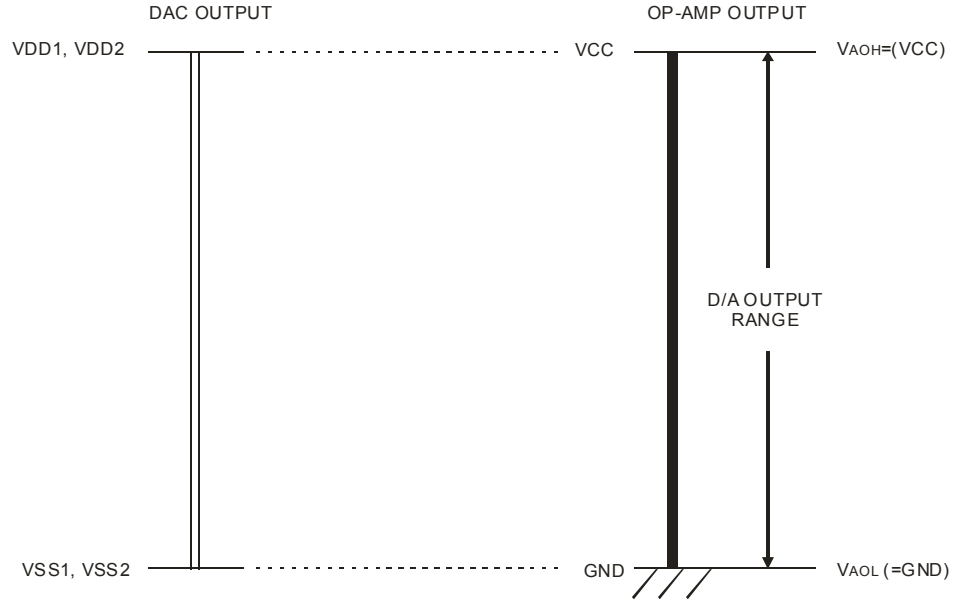
TIMING GIAGRAM



ANALOG OUTPUT VOLTAGE RANGE



VSS1=VDD1=VDD2
GND=VSS1=VSS2

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Ta=+25℃ GND=0V, $V_{DD1} \leq VCC$, $V_{DD2} \leq VCC$	-0.3	-	7.0	V
	V_{DD1}, V_{DD2}		-0.3	-	7.0	
Input voltage output voltage	V_{IN}	Ta=+25℃ GND=0V, should not exceed V_{CC}+0.3V	-0.3	-	V_{CC}+0.3	V
	V_{OUT}		-0.3	-	V_{CC}+0.3	
Power dissipation	P_D	-	-	-	250	mW
Operating temperature	Topr	-	-45	-	+85	℃
Storage temperature	Tstg	-	-65	-	+150	℃

RECOMMANDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (MCU interface/OP-AMP block)	V_{CC}	$V_{CC}>V_{DD}$	4.5	5.0	5.5	V
	GND		-	0	-	
Power supply voltage (Analog block)*	V_{DD1}, V_{DD2}	V_{DD1}-$V_{SS1} \geq 2.0V$ V_{DD2}-$V_{SS2} \geq 2.0V$	2.0	-	V_{CC}	V
	V_{SS1}, V_{SS2}		GND	-	V_{CC}-2.0	
Analog output source current	I_{AL}	-	-	-	-1.0	mA
Analog output sink current	I_{AH}	-	-	-	+1.0	mA
Analog output load capacitance (OSC limit)	C_{AL}	-	-	-	1.0	μF

Note: *=Except Operational Analog Amplifier Output Buffer Block. V_{DD1} (V_{SS1}), V_{DD2} (V_{SS2}) can be independently set.

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DIGITAL BLOCK DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Active supply current (VCC)*	I_{CC}	CLK=1MHz Unloaded	-	2.0	8.0	mA
Input leakage current (CLK, DI, STB)	I_{ILK}	V_{IN}=0 to V_{CC}	-10	-	+10	μA
Low level input voltage	V_{IL}		-	-	$0.2V_{CC}$	V
High level input voltage (CLK, DI, STB)	V_{IH}		$0.5V_{CC}$	-	-	V
Low level output voltage (DO)	V_{OL}	I_{OL}=2.5mA	-	-	0.4	V
High level output voltage (DO)	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V

Note: *=Supply current to the operational amplifier block included.

ANALOG BLOVK DC ELECTRICAL CHARACTERISTICS

(D/A CONVERTERS WITH OPERATIOPNAL AMPLIFIER OUTPUT BUFFERS)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current VDD1, VDD2*	IDD	Unloaded IDD is the total current value for the DAC output pin #1 & #2	-	1	6.0	mA
Minimum analog output voltage 1 (AOn)	VAOL1	$V_{DD1}=V_{DD2}=V_{CC}$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AL}=0\mu A$ Digital data=#00H	V_{SS1} V_{SS2}	-	$V_{SS1}+0.1$ $V_{SS2}+0.1$	V
Minimum analog output voltage 2 (AOn)	VAOL2	$V_{DD1}=V_{DD2}=V_{CC}=5.0V$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AL}=500\mu A$ Digital data=#00H	$V_{SS1}-0.2$ $V_{SS2}-0.2$	V_{SS1} V_{SS2}	$V_{SS1}+0.2$ $V_{SS2}+0.2$	V
Minimum analog output voltage 3 (AOn)	VAOL3	$V_{DD1}=V_{DD2}=V_{CC}=5.0V$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AH}=500\mu A$ Digital data=#00H	V_{SS1} V_{SS2}	-	$V_{SS1}+0.2$ $V_{SS2}+0.2$	V
Minimum analog output voltage 4 (AOn)	VAOL4	$V_{DD1}=V_{DD2}=V_{CC}=5.0V$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AL}=1.0mA$ Digital data=#00H	$V_{SS1}-0.3$ $V_{SS2}-0.3$	V_{SS1} V_{SS2}	$V_{SS1}+0.3$ $V_{SS2}+0.3$	V
Minimum analog output voltage 5 (AOn)	VAOL5	$V_{DD1}=V_{DD2}=V_{CC}=5.0V$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AH}=1.0mA$ Digital data=#00H	V_{SS1} V_{SS2}	-	$V_{SS1}+0.3$ $V_{SS2}+0.3$	V
Maximum analog output voltage 1 (AOn)	VAOH1	$V_{DD1}=V_{DD2}=V_{CC}$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AL}=0\mu A$ Digital data=#FFH	$V_{SS1}-0.1$ $V_{SS2}-0.1$	-	V_{DD1} V_{DD2}	V
Maximum analog output voltage 2 (AOn)	VAOH2	$V_{DD1}=V_{DD2}=V_{CC}=5.0V$ $V_{SS1}=V_{SS2}=GND=0V$ $I_{AL}=500\mu A$ Digital data=#FFH	$V_{SS1}-0.2$ $V_{SS2}-0.2$	-	V_{DD1} V_{DD2}	V

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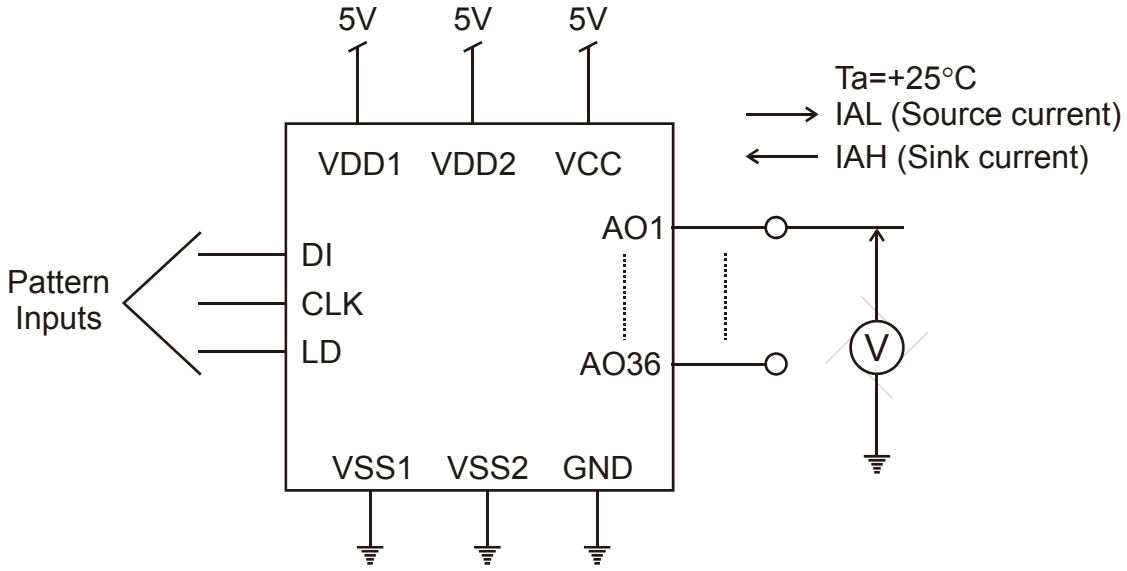
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum analog output voltage 3 (AOn)	VAOH3	V_{DD1}=V_{DD2}=V_{CC}=5.0V V_{SS1}=V_{SS2}=GND=0V I_{AH}=500μA Digital data=#FFH	V_{SS1}-0.2 V_{SS2}-0.2	V_{DD1} V_{DD2}	V_{SS1}+0.2 V_{SS2}+0.2	V
Maximum analog output voltage 4 (AOn)	VAOH4	V_{DD1}=V_{DD2}=V_{CC}=5.0V V_{SS1}=V_{SS2}=GND=0V I_{AL}=1.0mA Digital data=#FFH	V_{SS1}-0.3 V_{SS2}-0.3	-	V_{DD1} V_{DD2}	V
Maximum analog output voltage 5 (AOn)	VAOH5	V_{DD1}=V_{DD2}=V_{CC}=5.0V V_{SS1}=V_{SS2}=GND=0V I_{AH}=1.0mA Digital data=#FFH	V_{SS1}-0.3 V_{SS2}-0.3	V_{DD1} V_{DD2}	V_{SS1}+0.3 V_{SS2}+0.3	V
Resolution (AOn)	Res		-	8	-	bit
Linearity error (AOn)	LE	Unloaded V_{DD}≤V_{CC}-0.1V V_{SS}≥0.1V	-1.5	-	1.5	LSB
Different linearity (AOn)	DLE	Unloaded	-1.0	-	1.0	LSB

Note: *=Supply current to the operational amplifier block not included.

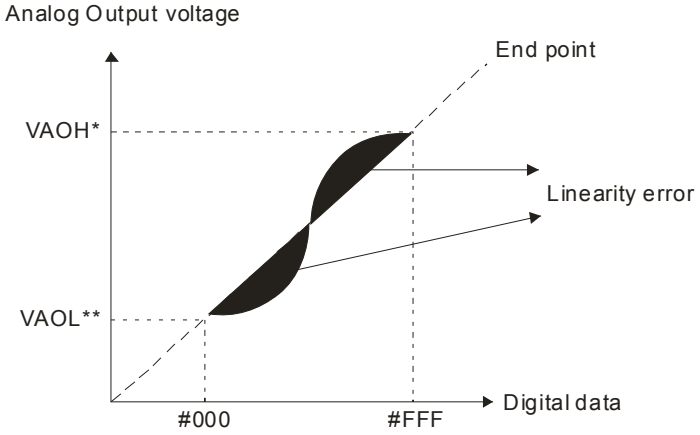


AC CHARACTERISTICS

(Unless otherwise specified, recommended operation conditions prevail)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock low time	tCLK		200	-	ns
Clock high time	tCKH		200	-	ns
Clock rise time	tCR		-	200	ns
Clock fall time	tCF		-	200	ns
Data setup time	tDCH		30	-	ns
Data hold time	tCHD		60	-	ns
Load strobe high time	tSTBH		100	-	ns
Load strobe setup time	tCHL		200	-	ns
Load strobe hold time	tSTBC		100	-	ns
DAC output setting time	tSTBD	RAL=10KΩ, CAL=50pF (note 1)	-	100	μs
Data output delay time	tDO	CL=20pF(min.), 100pF (max.) (note 2)	70	350	ns

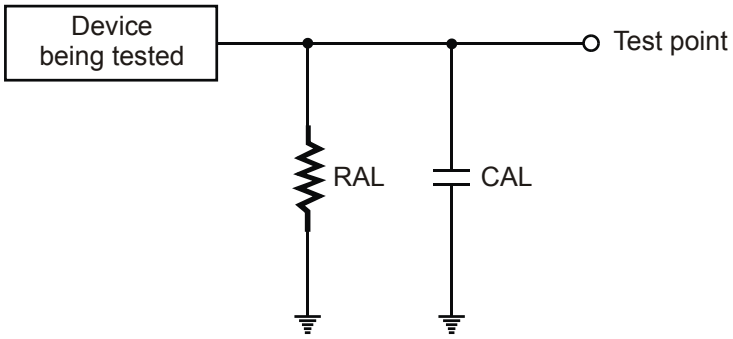
NONLINEARITY ERROR DEFINITION



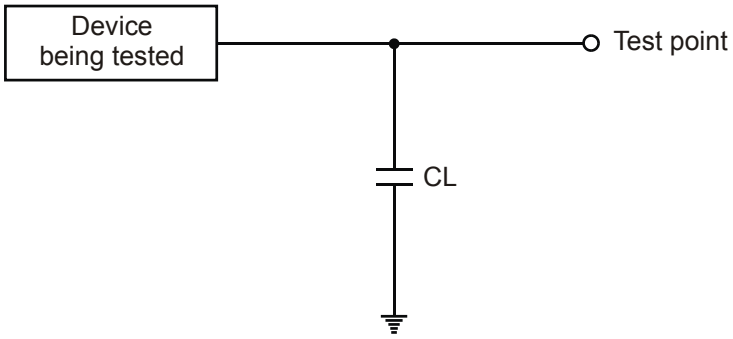
Note:
1. *=VAOH is not always equal to VDD.
2. **=VAOL is not always equal to VSS.

AC TEST CONDITIONS

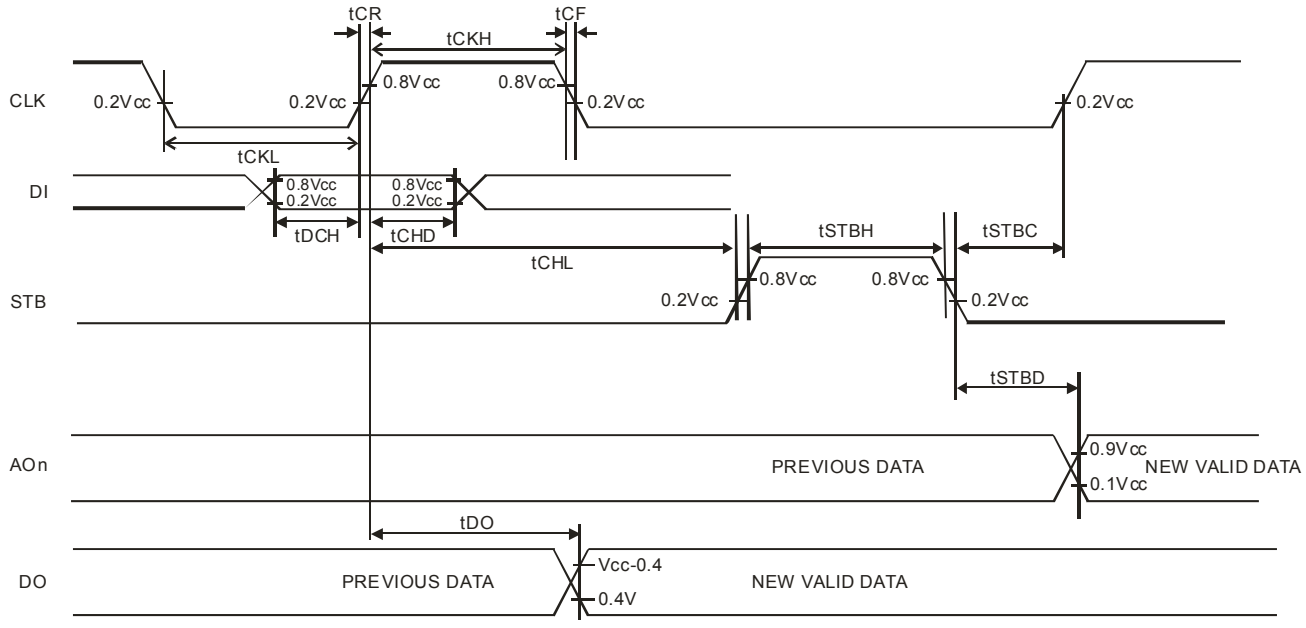
DAC OUTPUT SETTING TIME



DAC OUTPUT DELAY TIME



INPUT/OUTPUT TIMING



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ORDER INFORMATION

Valid Part No.	Package Type	Top Code
PT8214	48 pins, LQFP	PT8214
PT8214 (L)	48 pins, LQFP	PT8214

Notes:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the date code.

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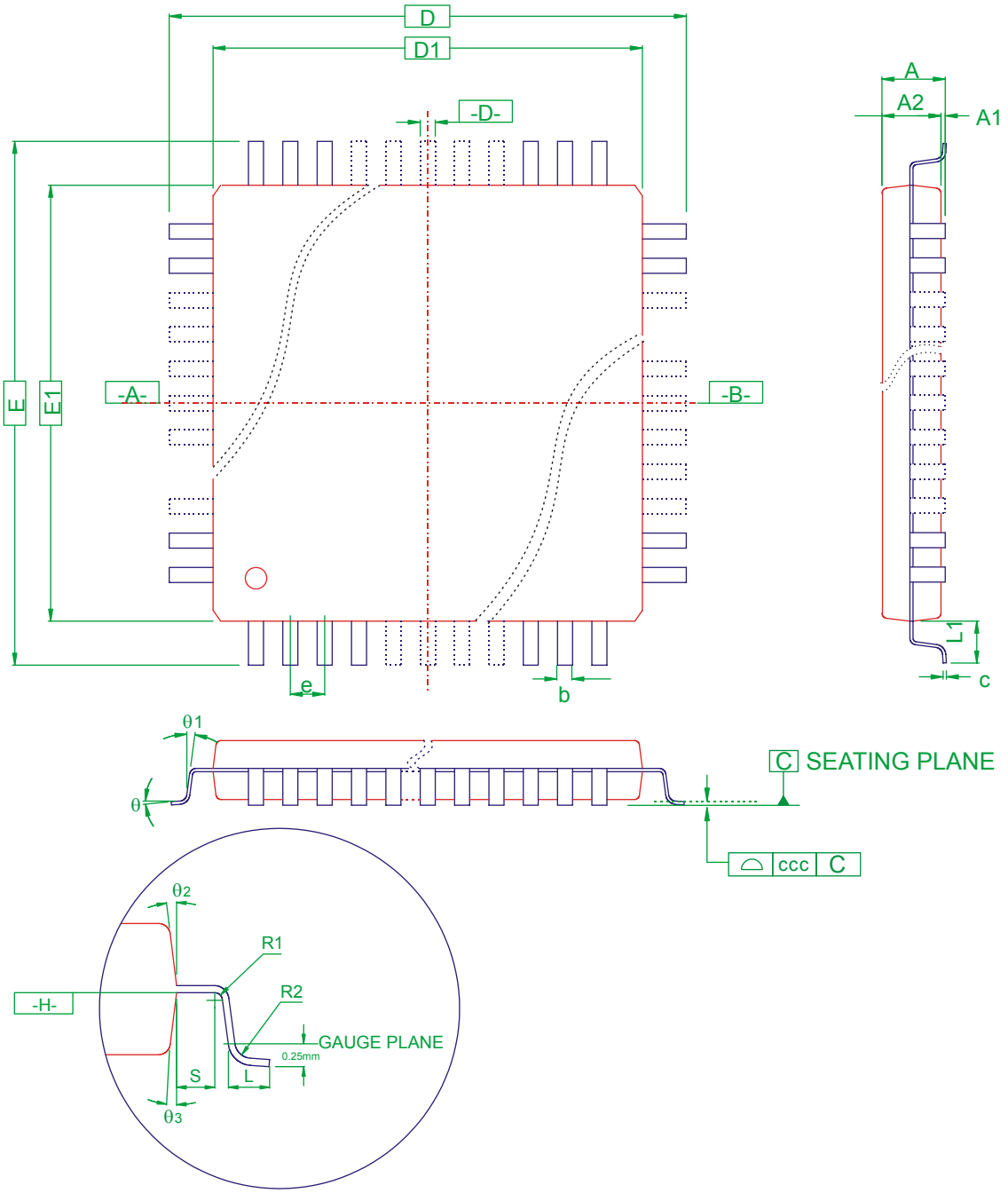
48 PINS, LQFP (BODY SIZE: 7 X 7MM, PITCH SIZE: 0.50, THK BODY: 1.40MM)



Symbol	Min.	Typ.	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		9.00 BSC	
D1		7.00 BSC	
e		0.50 BSC	
E		9.00 BSC	
E1		7.00 BSC	
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
C	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
ccc		0.08	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. The top package body size may be smaller than the bottom package size by as much as 0.15mm.
3. Datum A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling Dimension: MILLIMETER
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between the protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm PITCH Package.
7. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Details of pin 1 identifier are optional but must be located within the zone identified.
10. Dimension D2 and E2 show the minimum allowed for the optional exposed heat slug. The maximum allowed is equal to the package body size (D1 and E1). However, the size of the exposed heat slug is variable depending on the device function (die size). End users should verify the actual size or either top or bottom exposed thermal pad for specific device application.
11. Refer to JEDEC MS-026 Variation BBC.

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