

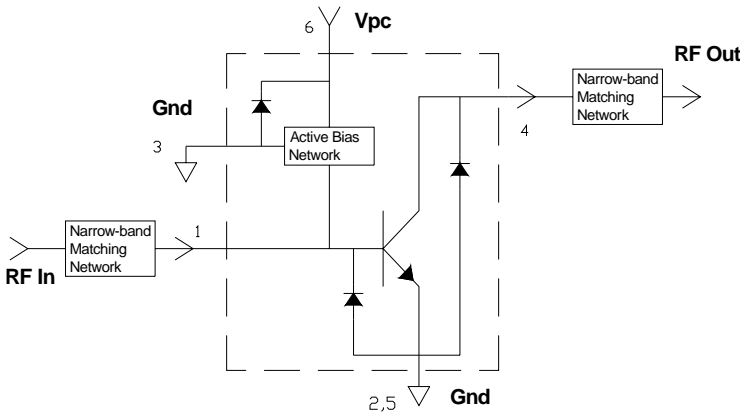


Product Description

Sirenza Microdevices' SGL-0363Z is a low power, low noise amplifier. It is designed for 2.7 to 3.3V battery operation. The matching networks are implemented externally which allows for optimum narrow-band performance with 20dB typical gain and 1.1dB noise figure from 200-900MHz. This RFIC uses the latest Silicon Germanium HBT process.

The matte tin finish on Sirenza's lead-free "Z" package is applied using a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. The package body is manufactured with green molding compounds that contain no antimony trioxide or halogenated fire retardants.

Simplified Device Schematic



Preliminary

SGL-0363Z



5-2000 MHz Low Noise Amplifier Silicon Germanium



Product Features

- Lead Free, RoHS Compliant & Green Package
- Low Power Consumption, 5.7mA @ 3.3V
- External Input Noise Match
- High Gain and Low Noise, 20dB and 1.1dB respectively @ 900MHz
- Operates from 2.7 to 3.3V
- Power Shutdown Capability using V_{PC}
- 500V ESD, Class 1B
- Small Package: SOT-363
- High input overdrive capability, +18dBm

Applications

- Low Power LNA for ISM, Cellular and Mobile Communications

Symbol	Parameters	Units	Frequency	Min.	Typ.	Max.
S ₂₁	Small Signal Gain	dB	200 MHz	17	21	23
			450 MHz		20	
			900 MHz		20	
P _{1dB}	Output Power at 1dB Compression	dBm	200 MHz		1.1	
			450 MHz		2.2	
			900 MHz		2.5	
IIP ₃	Input Third Order Intercept Point	dBm	200 MHz		-3.8	
			450 MHz		-2.4	
			900 MHz		-7.1	
NF	Noise Figure	dBm	200 MHz		1.0	
			450 MHz		1.1	
			900 MHz		1.1	
IRL	Input Return Loss	dBm	200 MHz		14	
			450 MHz		12	
			900 MHz		15	
ORL	Output Return Loss	dBm	200 MHz		20	
			450 MHz		19	
			900 MHz		12	
S12	Reverse Isolation	dBm	200 MHz		24	
			450 MHz		25	
			900 MHz		27	
I _D	Device Operating Current	mA		4.8	5.7	6.6
R _{TH, j-l}	Thermal Resistance (junction - lead)	°C/W			173	

Test Conditions: V_S = 3.3V I_D = 5.7mA Typ. IIP₃ Tone Spacing = 1MHz, Pout per tone = -15 dBm
T_L = 25°C Z_S = Z_L = 50 Ohms Different Application Circuit per Band

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Absolute Maximum Ratings

Parameter	Absolute Limit
Max Device Current (I _D)	20mA
Max Device Voltage (V _D)	5.5 V
Max. RF Input Power* (See Note)	+18 dBm
Max. Junction Temp. (T _J)	+150°C
Operating Temp. Range (T _L)	-40°C to +85°C
Max. Storage Temp.	+150°C

***Note:** Load condition 1, Z_L = 50 Ohms
 Load condition 2, Z_L = 10:1 VSWR

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

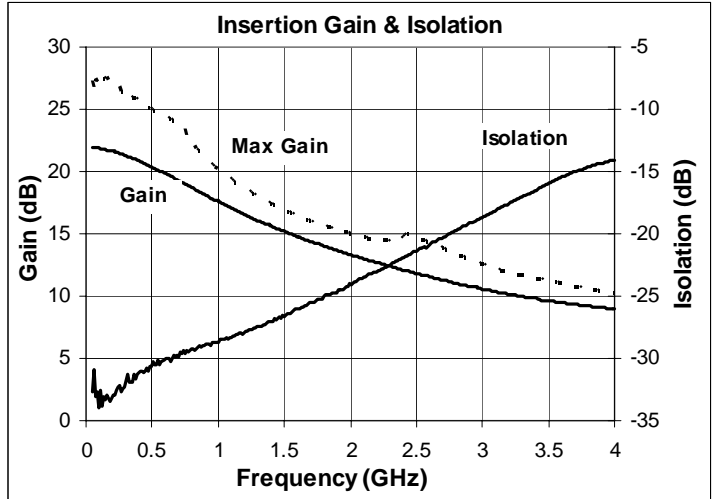
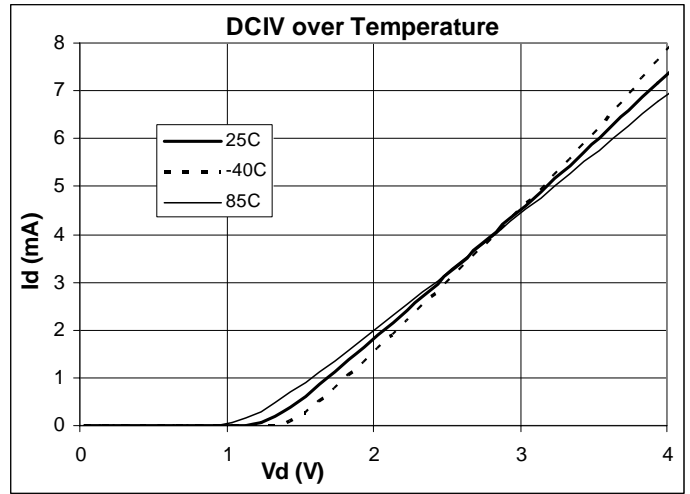
Bias Conditions should also satisfy the following expression:
 $I_D V_D < (T_J - T_L) / R_{TH} + j - T_L = T_{LEAD}$

Reliability & Qualification Information	
Parameter	Rating
ESD Rating - Human Body Model (HBM)	Class 1B
Moisture Sensitivity Level	MSL 1

This product qualification report can be downloaded at www.sirenza.com



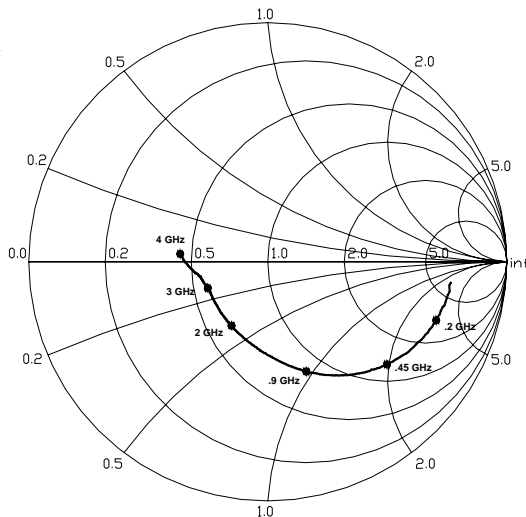
Caution: ESD Sensitive
 Appropriate precautions in handling, packaging and testing devices must be observed.



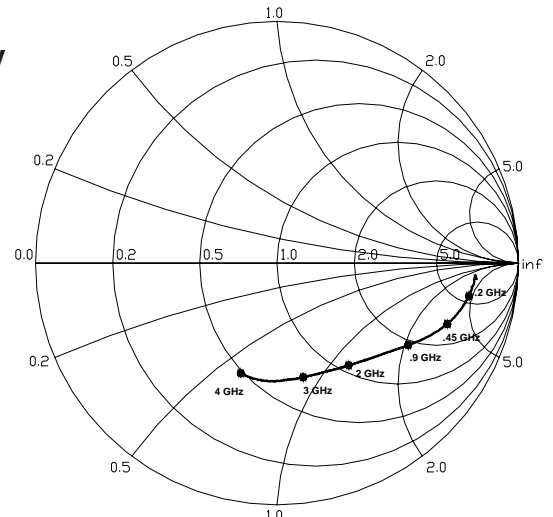
Typical Performance - De-embedded S-parameters

Note: S-parameters are de-embedded to the device leads with Z_S=Z_L=50Ω. The device was mounted on eval. board 125390-B and grounded like 900MHz application circuit. De-embedded S-parameters can be downloaded from our website (www.sirenza.com)

S11 Vs. Frequency



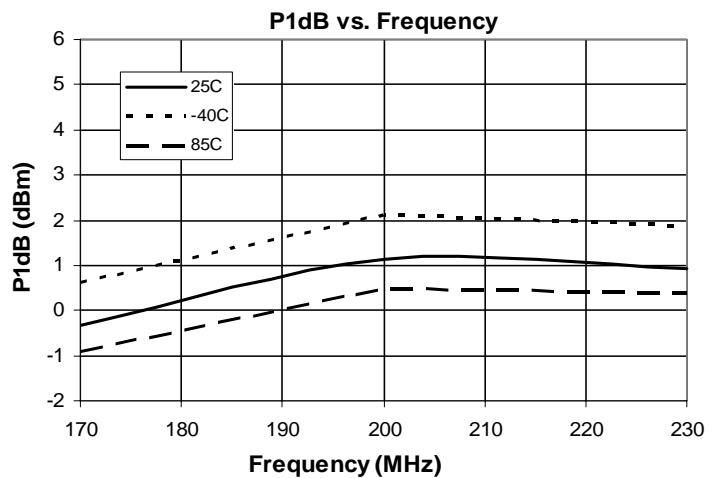
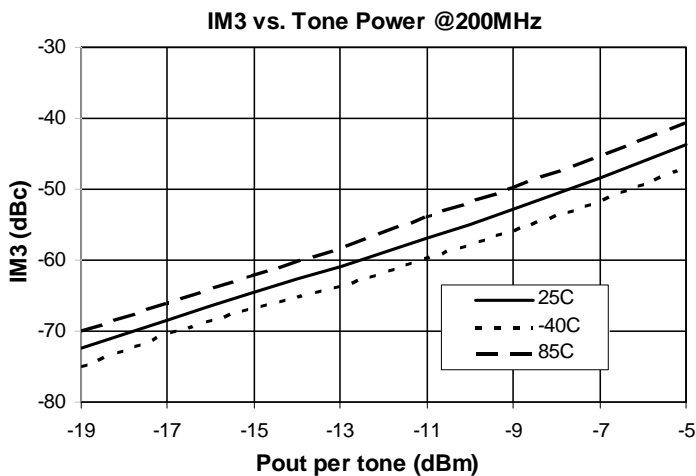
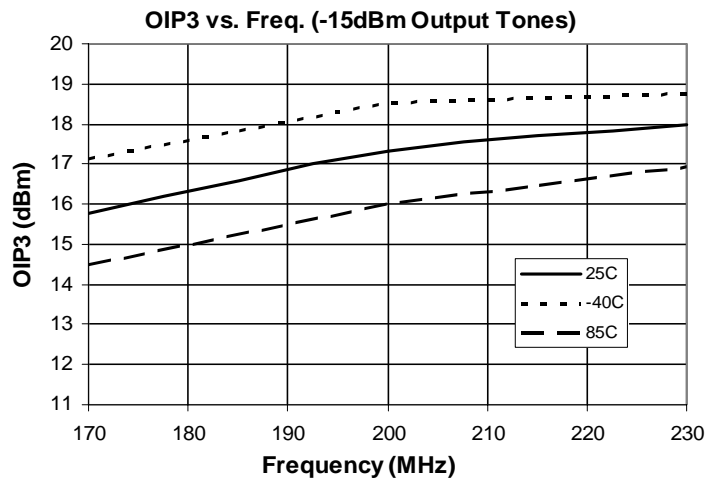
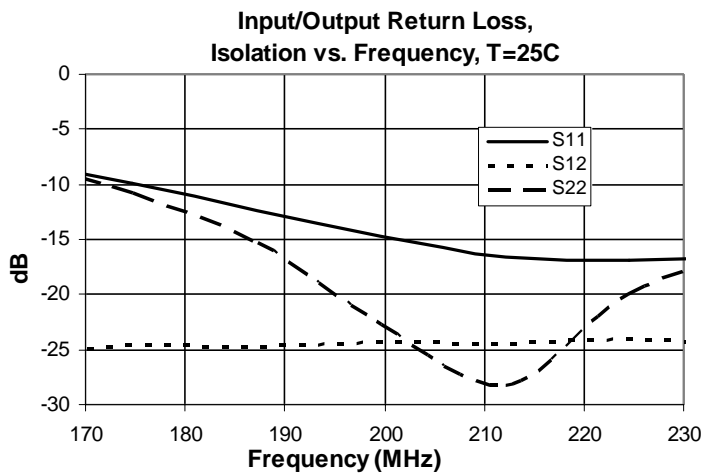
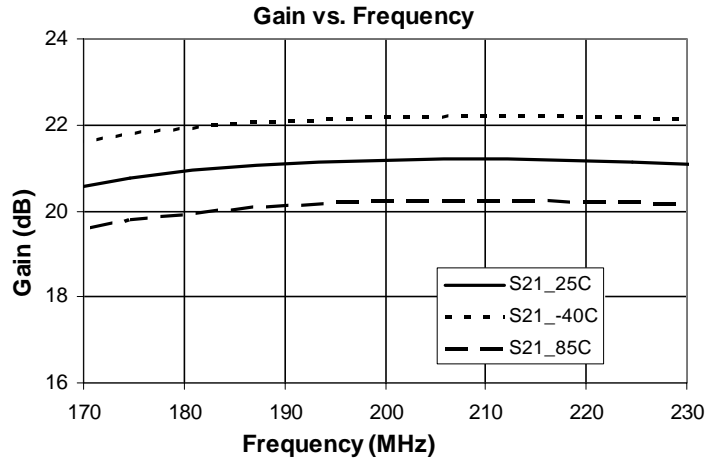
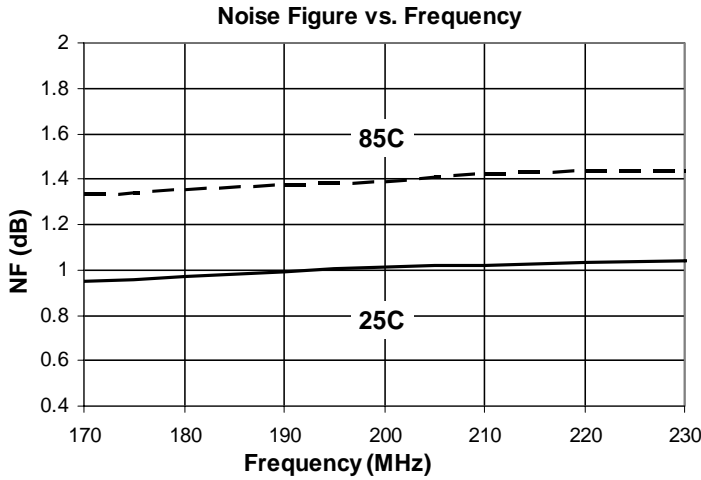
S22 Vs. Frequency





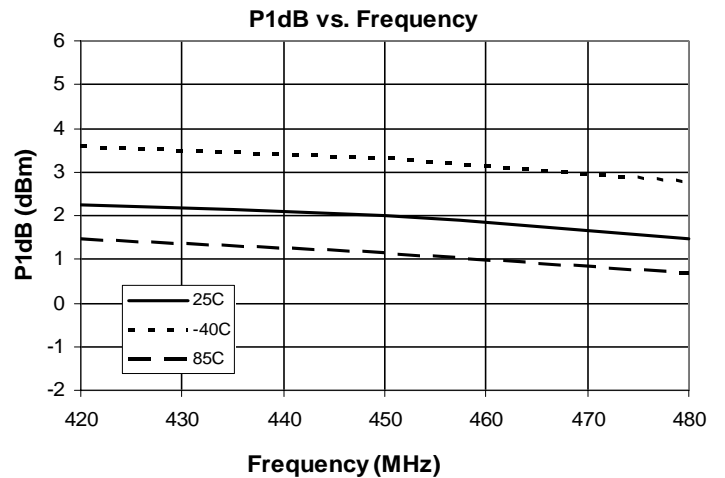
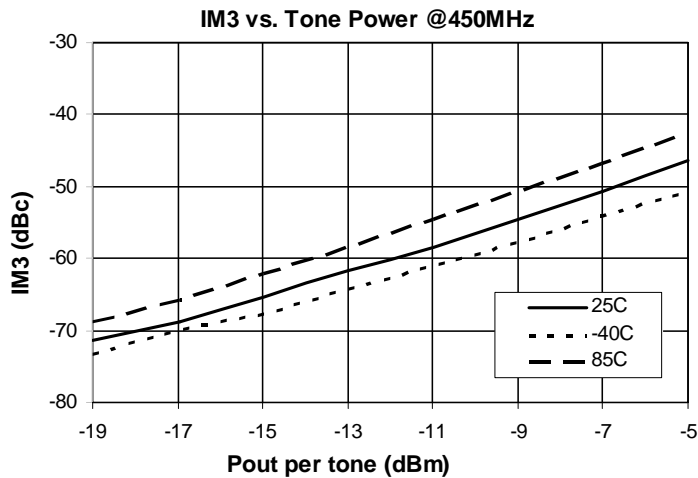
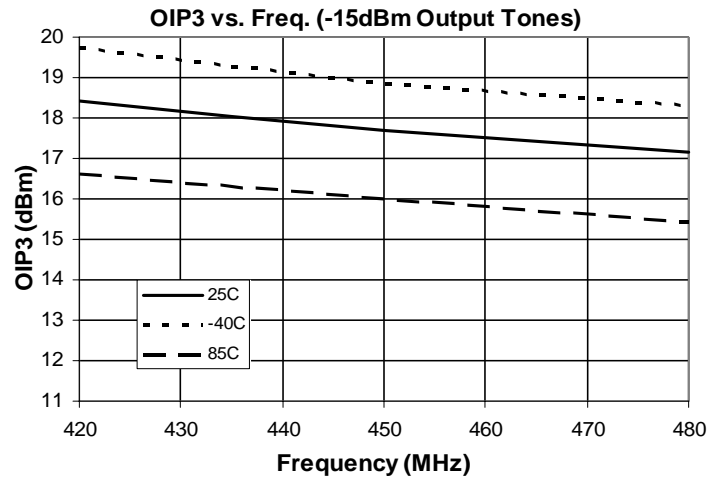
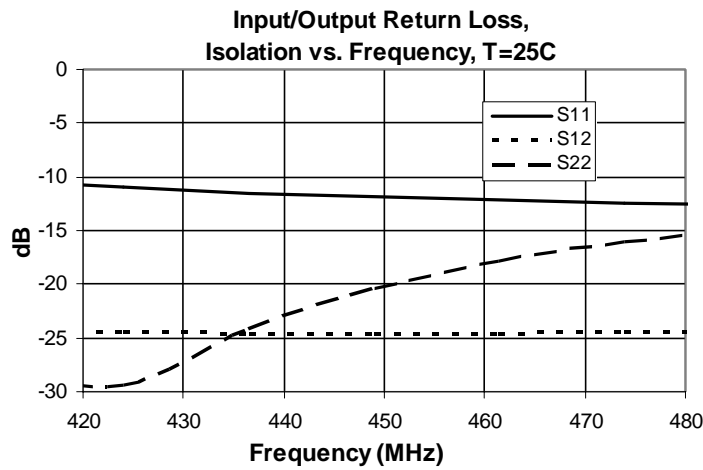
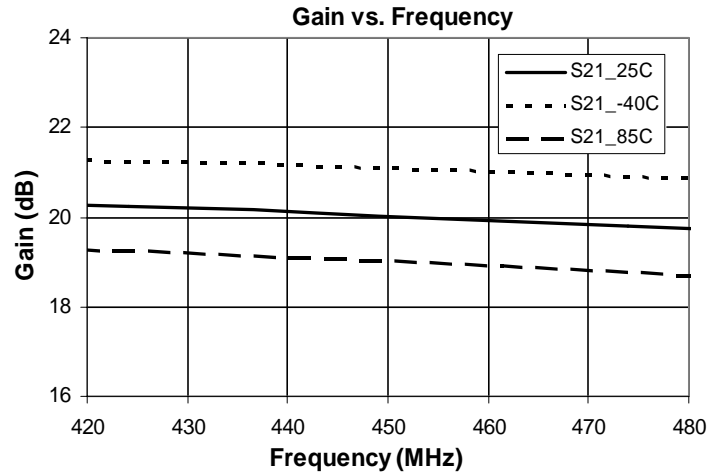
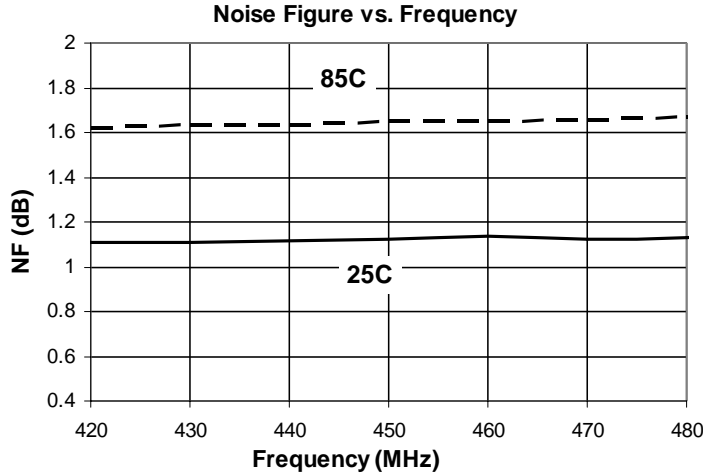
200 MHz Application Circuit Data, $V_s = 3.3V$, $I_D = 5.7mA$

Note: Tuned for NF



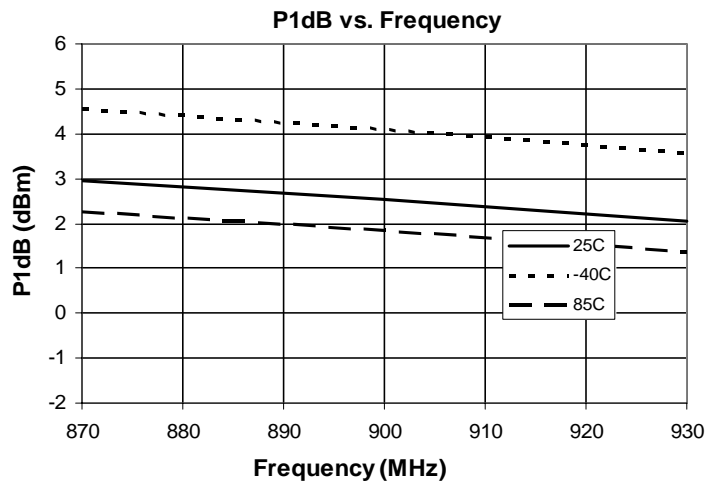
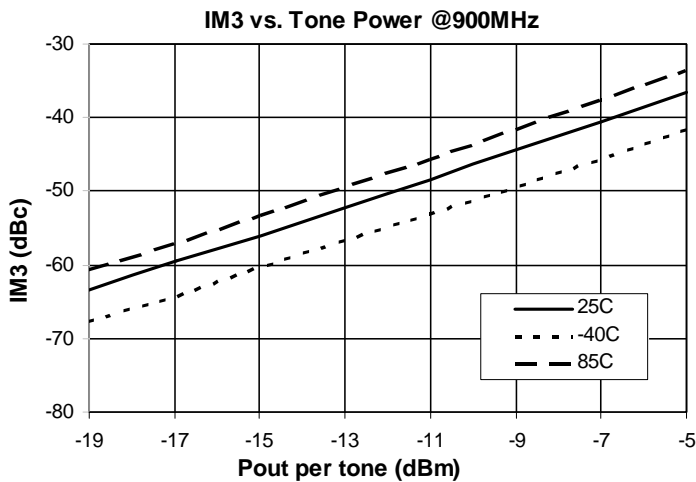
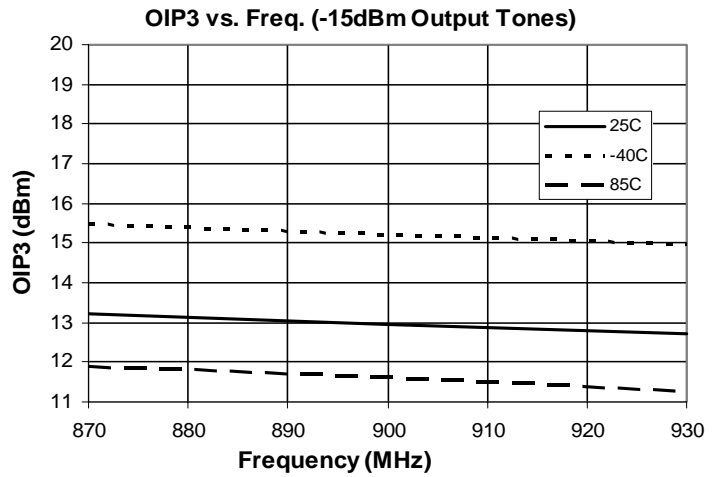
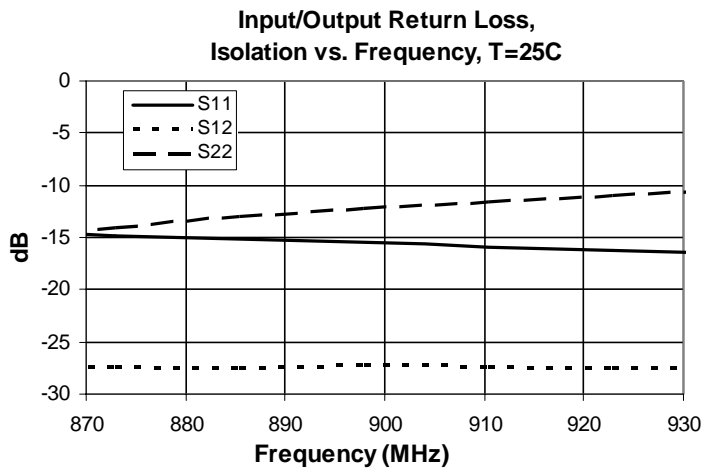
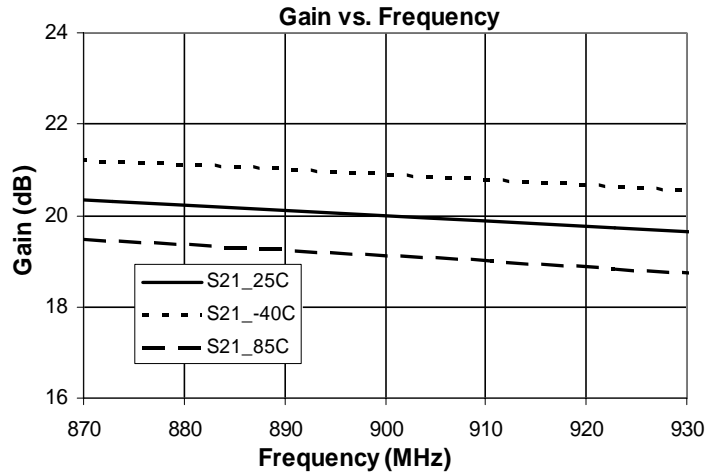
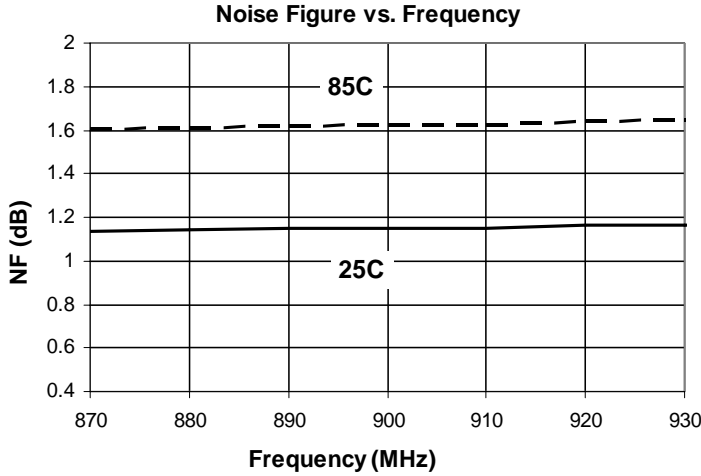
450 MHz Application Circuit Data, $V_s = 3.3V$, $I_D = 5.7mA$

Note: Tuned for NF

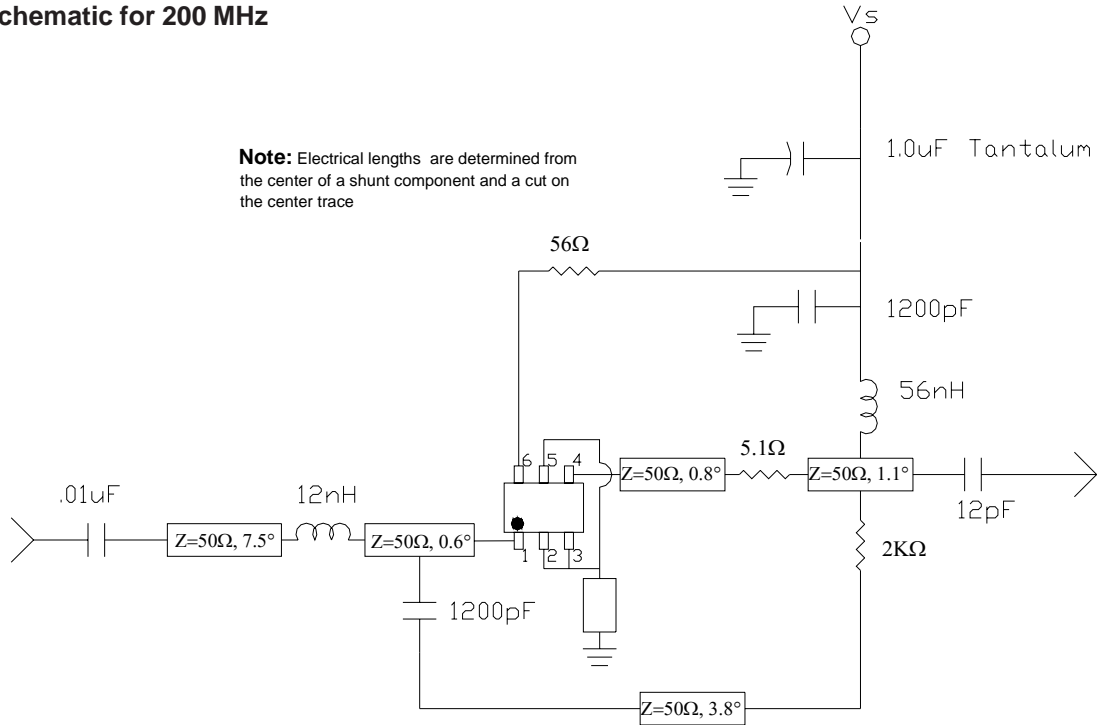


900 MHz Application Circuit Data, $V_s = 3.3V$, $I_D = 5.7mA$

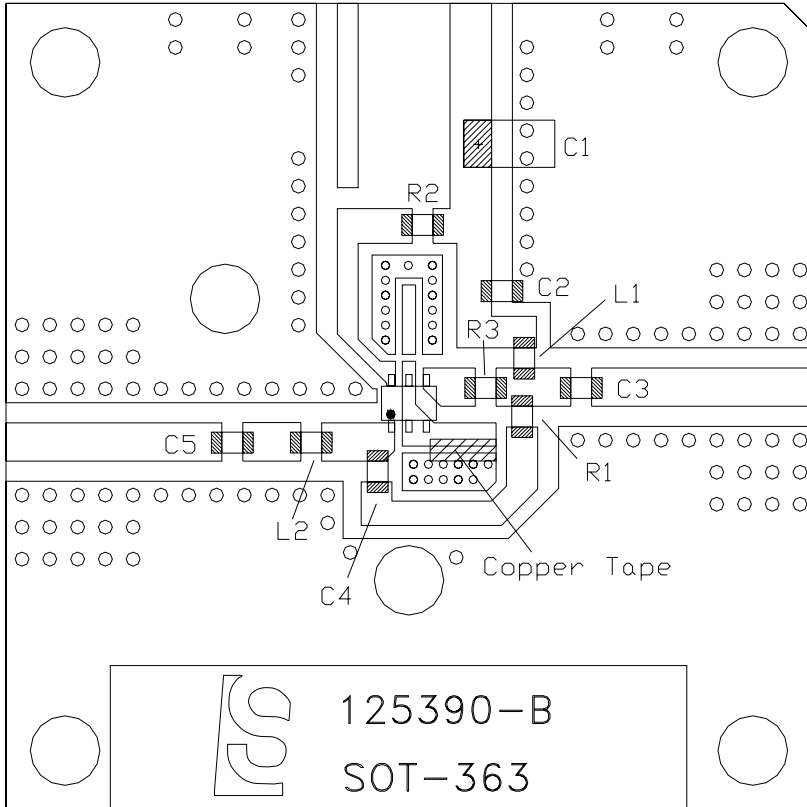
Note: Tuned for NF



Application Schematic for 200 MHz



Evaluation Board Layout for 200 MHz

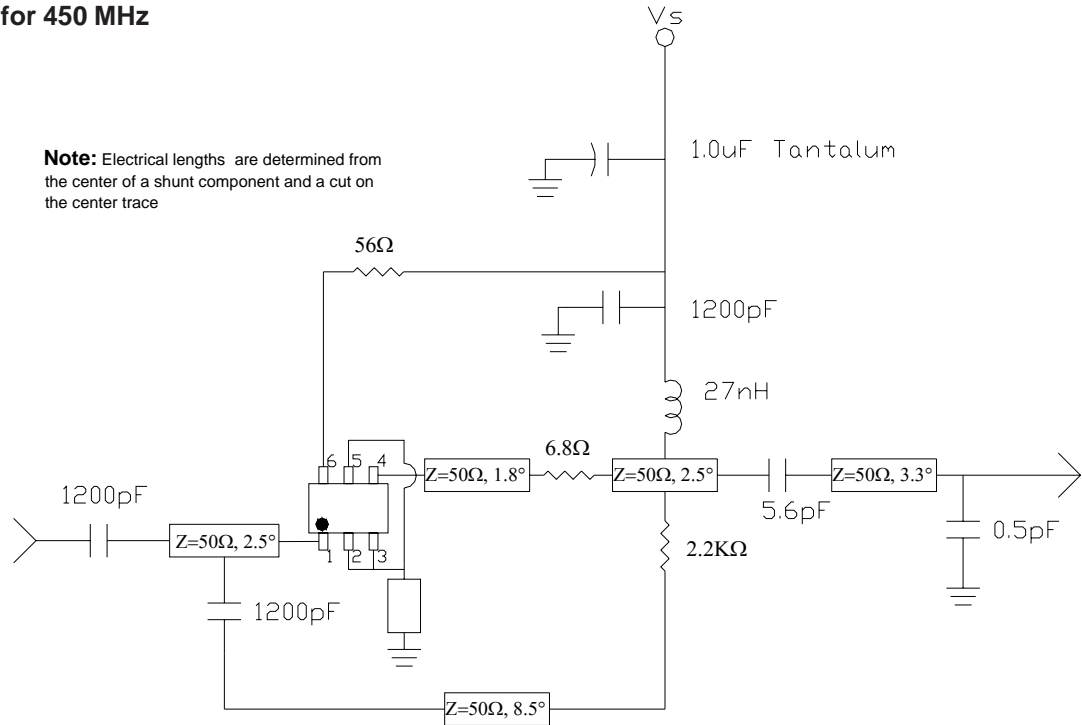


Bill of Materials

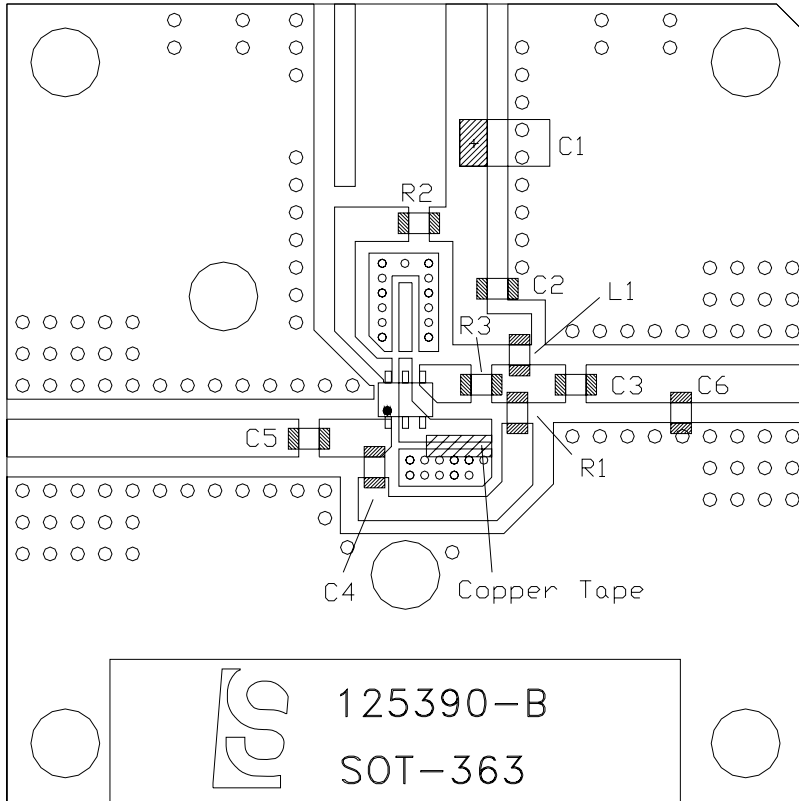
- C1 1.0uF Tantalum capacitor
- C2 1200pF 0603 ceramic capacitor
- C3 12pF 0603 ceramic capacitor
- C4 1200pF 0603 ceramic capacitor
- C5 .01uF 0603 ceramic capacitor
- L1 LL1608-FS56NJ Toko 56nH
- L2 LL1608-FS12NJ Toko 12nH
- R1 2KΩ 0603 res (5%)
- R2 56Ω 0603 res (5%)
- R3 5.1Ω 0603 res (5%)
- Connectors 2x PSF-S01-1mm GigaLane Co.
- Heat sink EEF-102059
- PCB 125390-B

Application Schematic for 450 MHz

Note: Electrical lengths are determined from the center of a shunt component and a cut on the center trace



Evaluation Board Layout for 450 MHz

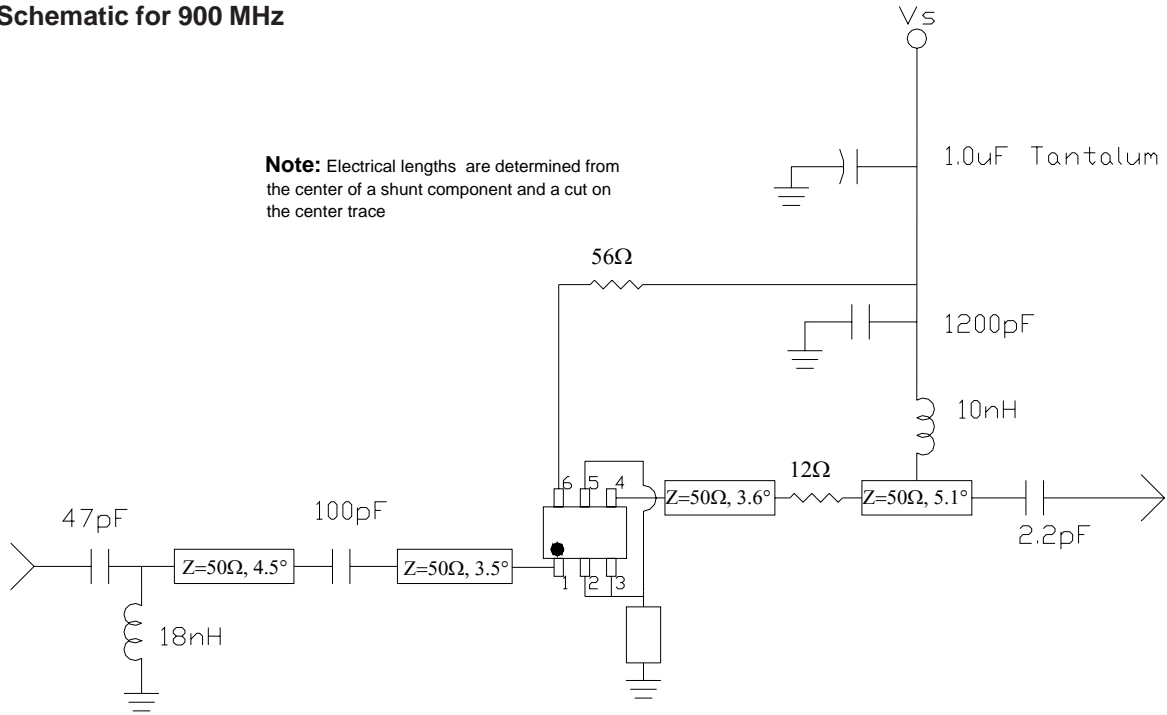


Bill of Materials

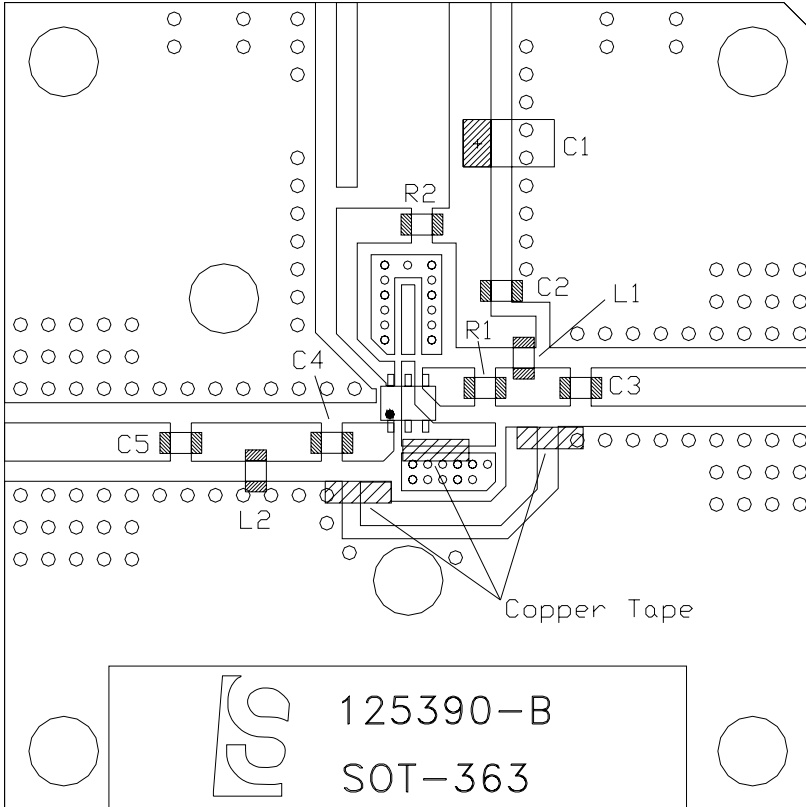
- C1 1.0uF Tantalum capacitor
- C2 1200pF ceramic 0603 capacitor
- C3 5.6pF ceramic 0603 capacitor
- C4 1200pF ceramic 0603 capacitor
- C5 1200pF ceramic 0603 capacitor
- C6 0.5pF ceramic 0603 capacitor
- L1 LL1608-FS27NJ Toko 27nH
- R1 2.2KΩ 0603 res (5%)
- R2 56Ω 0603 res (5%)
- R3 6.8Ω 0603 res (5%)

Connectors 2x PSF-S01-1mm GigaLane Co.
 Heat sink EEF-102059
 PCB 125390-B

Application Schematic for 900 MHz



Evaluation Board Layout for 900 MHz



Bill of Materials

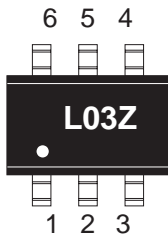
- C1 1.0uF Tantalum capacitor
- C2 1200pF ceramic 0603 capacitor
- C3 2.2pF ceramic 0603 capacitor
- C4 100pF ceramic 0603 capacitor
- C5 47pF ceramic 0603 capacitor
- L1 LL1608-FS10NJ Toko 10nH
- L2 LL1608-FS18NJ Toko 18nH
- R1 12Ω 0603 res (5%)
- R2 56Ω 0603 res (5%)

- Connectors 2x PSF-S01-1mm GigaLane Co.
- Heat sink EEF-102059
- PCB 125390-B

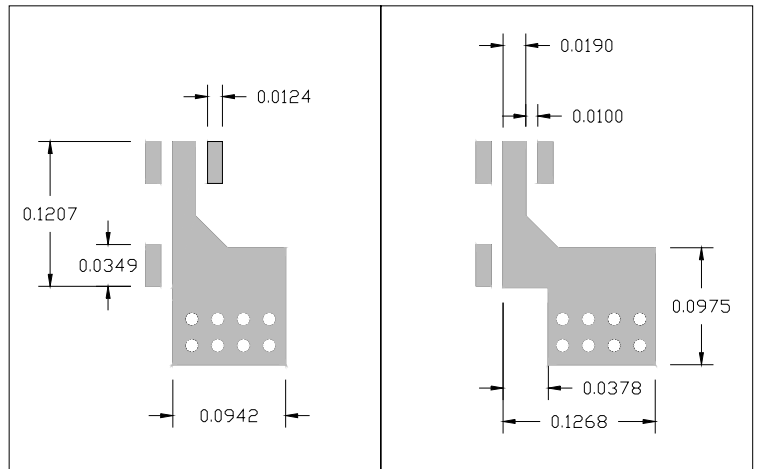
Pin #	Function	Description
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor and matching components as shown in the application schematics.
2, 5	GND	Connect to ground per application circuit drawing. Series feedback used to improve IRL.
3	Gnd	Gnd for active bias tied internally to pin 2 & 5
4	RF OUT/ V _D	RF output and bias pin. Bias should be supplied to this pin through an external RF choke. (See application circuits)
6	V _{PC}	V _{PC} is the bias control pin for the active bias network.

Part Number Ordering Information		
Part Number	Reel Size	Devices / Reel
SGL-0363Z	7"	3000

Part Identification



Suggested Pad Layouts



900MHz Layout

200MHz & 400MHz Layout

Nominal Package Dimensions

Dimensions in inches [millimeters]
 Refer to drawing posted at www.sirenza.com for tolerances.

