W55VG580

TV ENCODER

Document History

DATE	REVISION	COMMENTS
Aug 2002	A1	---
Feb 2004	A2	Remove “H” from W55VG580H Add W55VG580 bonding pad diagram and application circuit
May 2006	A5	Add package, QFN-32, and proof edit.

Winbond Electronics Corp.

Table of Contents-

1. GENERAL DESCRIPTION

The W55VG580 is a digital video encoder designed for digital video applications such as VCD players, DVD players, and video games. It digital video encoder converts 8-bit YCrCb (4:2:2) 8-bit data into analog composite video or Y/C video (S-video) signals. The W55VG580 supports video format is 525-line (M) NTSC/PAL orand 625-line (B, D, G, H, I, M, Nc) PAL video formats; CCIR 601 .

and square pixel input data; and interlaced and non-interlaced frames.

The W55VG580 can operates at in either master or slave mode. The data rate can be CCIR601 or square pixel. At In slave mode, the W55VG580 can auto auto-detect the input video format from the HSYNCN and VSYNCN pins and generates the corresponding video signals. At In master mode, it generates the required video timing, based on internally according to the various pin **and internal settings** In addition to slave and master modes, configuration.

The input YCrCb data are converted into YUV signals. The chroma data are then low passed by a 1.3 MHz filter and modulated by a color subcarrier. The W55VG580 operates with a 2X pixel rate input.

The W55VG580 has two DAC outputs which can output two composite video or Y/C S-video signal.

The W55VG580 can operate at has a power-down mode that is controlled by by selecting the SLEEP pin. The W55VG580 is designed for digital video applications such as VCD, DVD, and video games.

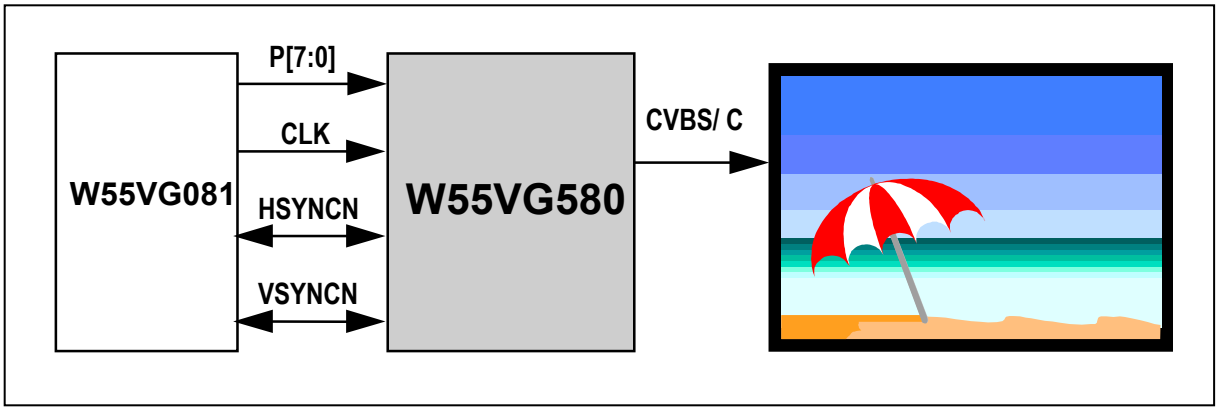
The W55VG580 operates at **twice** the input data rate. The input YCrCb data are first converted into YUV signals. Then, the chroma data are passed through a 1.3-MHz low-pass filter and modulated by a color subcarrier. The result is available on the two DAC outputs, which can output two composite video or one Y/C S-video signal.

2. FEATURES AND APPLICATIONS

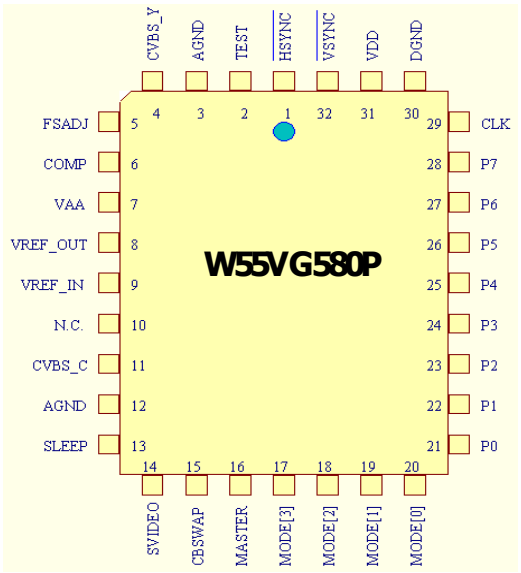
2.1 FEATURES

- Monolithic CMOS process
- Master clock rate 2X 2x pixel rate
- Two composite outputs or Y/C video output (S video)
- Power-down mode
- CCIR601 or square pixel input data rates
- Master/slave sync signal switchable (controlled by pin)
- Interlaced and non-interlaced operation
- Optional internal voltage reference

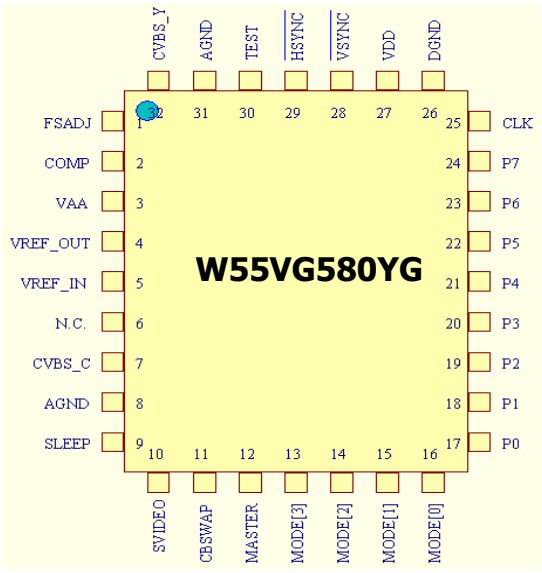
2.2 APPLICATIONS



3. PINOUT AND DESCRIPTION



PLCC



QFN-32

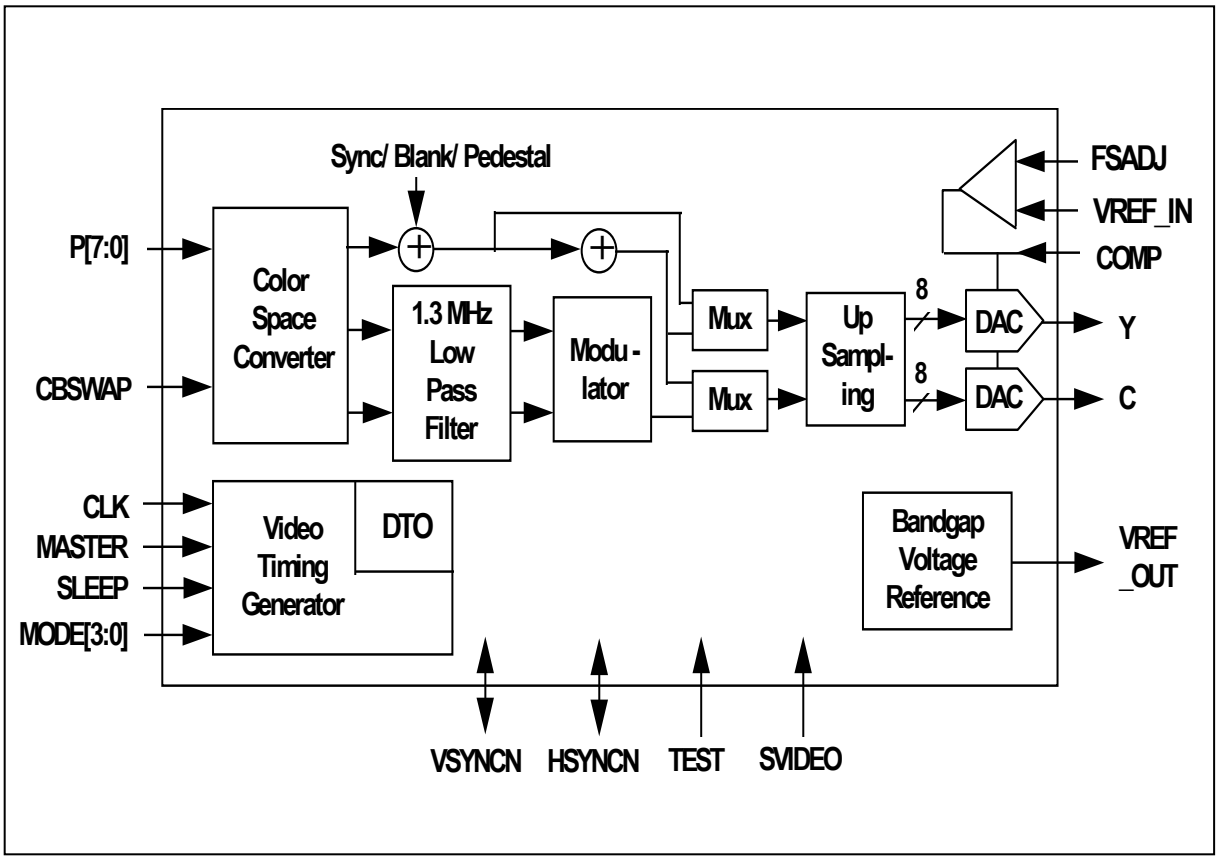
(All digital pins are TTL compatible)

PLCC PIN NO.	PIN NAME	I/O	DESCRIPTION
21-28	P[0:7]	I	YCrCb pixel inputs. They are latched on the falling edge of CLK. YCrCb input data conform to CCIR 601.
29	CLK	I	2XPixel clock input for 8-bit YCrCb data.
32	VSYNCN	I/O	Vertical sync input/output. VSYNCN is latched/output following the rising edge of CLK.
1	HSYNCN	I/O	Horizontal sync input/output. HSYNCN is latched/output following the rising edge of CLK.
16	MASTER	I	Master/slave mode select. A logical -high 1 for master mode operation. A logical 0 for slave mode operation.
15	CBSWAP	I	Cr and Cb pixel sequence set up pin. Logic high swap the Cr and Cb sequence.
14	SVIDEO	I	SVIDEO select input pin. A logic high selects Y/C output; A logical low selects composite video output.
13	SLEEP	I	Power save mode. Logic high 1 on this pin puts the chip into power-down mode.

Continued.

PLCC PIN NO.	PIN NAME	I/O	DESCRIPTION
17-20	Mode[3:0]	I	Mode configuration pin.
2	TEST	I	Test pin. This pin must be connected to DGND.
9	VREF_IN	I	Voltage reference input. An external reference voltage reference must supply typical 1.235 V to this pin. In either case, A 0.1-uF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close as possible to minimize the length of the load. This pin may be connected directly to VREF_OUT.
8	VREF_OUT	O	Voltage reference output. It generates a typical 1.2V voltage reference and may be used to drive VREF_IN pin directly.
5	FSADJ	---	Full-Scale adjust control pin. The full-Scale scale current of the D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground. The relationship is $RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$.
6	COMP	---	Compensation pin. A 0.1-uF ceramic capacitor must should be used to bypass this pin to VAA. The lead length must should be kept as short as possible to avoid noise.
4	CVBS_Y	O	Composite/Luminance output. This is a high-impedance current source output, and it can drive a 37.5-W load. The output format can be is selected by the PAL pin. The pin can drive a 37.5 W load. If unused , this pin must should be connected directly to GND.
11	CVBS_C	O	Composite/Chroma output. This is a high high-impedance current source Outputoutput, and it can drive a 37.5-W load. The output format can be is selected by the PAL pin. The pin can drive a 37.5 W load. If unused, this pin must should be connected directly to GND.
10	NC	---	No connection
31	VDD	---	Digital power pin
30	DGND	---	Digital ground pin
7	VAA	---	Analog power pin
3,12	AGND	---	Analog ground pin

4. BLOCK DIAGRAM



5. FUNCTIONAL DESCRIPTION

5.1 Input formatting

The input circuitry accepts 8-bit CCIR601 4:2:2 YCrCb data . The data are input via the P[7:0] inputs and latched on the falling edge of CLK.

The input YCrCb pixel sequence can be arranged by setting the CBSWAP pin and the YCSWAP mode register. If the CBSWAP pin and the YCSWAP mode register are all zero, the first pixel data latched by the CLK pin after the falling edge of HSYNCN is Cb. The sequence appears as Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 .... This can be swap by setting the CBSWAP pin and the YCSWAP mode register.

The input clock rate can be CCIR601 2X13.5MHz or square pixel rate . Color burst frequency is derived from the CLOCK input. Any jitter on the CLOCK pin may induce a color burst frequency error. A stable clock source is recommended.

The Y of the 16-bit YCrCb data has nominal range from 16-235 and Cr/Cb has a nominal range from 16-240, with 128 equal to zero. When the Y value is between 1-15, the internal circuit will clamp these values to 16. When the Y value is 0 and 255, the internal circuit will set the Y value as 38. When the Cr/Cb is between 1-15, the internal circuit will clamp these values to 16. When the Cr value is 0 and 255, the internal circuit will set the Cr value as 112. When Cb value is 0 and 255, the internal circuit will set the Cb value as 225. Thus when the external video source is reset to 0 or 255, the color at video output will appear blue.

5.2 Mode selection

There are 7Seven mode registers which can be are programmed by setting the four MODE [3:0] pins and the MASTER pin. The following table illustrates the arrangement of the 7 mode these registers.

PIN DESCRIPTION				
The MASTER pin	**MODE[3]**	**MODE[2]**	**MODE[1]**	**MODE[0]**
0 (slave)	YCSWAP	SETUP	PALSA	--
1 (master)	EFIELD	PAL625	INTERLACED	SQUARE

In slave mode, the MODE [3:1] pins control the YCSWAP, SETUP, and PALSA registers. The W55VG580 automatically detects the input video timing, so the EFIELD, PAL625, INTERLACE, and SQUARE registers are not necessary. In master mode, however, the MODE [3:0] pins control the EFIELD, PAL625, INTERLACED and SQUARE registers. The YCSWAP, SETUP, and PALSA registers can be programmed by switching the W55VG580 to slave mode, setting the desired value(s) on the appropriate pin(s), and then switching back to master mode. Note that, at power-on, the YCSWAP, SETUP, and PALSA are set to zero.Each register is described in the following table.

MODE REGISTER NAME	SET TO 0	SET TO 1	COMMENTS
EFIELD	The VSYNCN pin will outputs the field signal. Low at VSYNCN pin for even fields, high for odd fields.	The VSYNCN pin will output the normal vertical synchronization signal.	This is only used at in master mode.
PAL625	525-line operation will be select	The 625-line operation will be select	This is only used at in master mode
INTERLACED	Non-interlaced operation will be select	The interlace operation will be select	This is only used at in master mode
SQUARE	CCIR-601 timing is selected.	The square pixel timing is selected.	This is only used at in master mode
YCSWAP	Do not swap Y and Cr/Cb	Swap Y and Cr/Cb sequence	----
SETUP	Disable the 7.5 IRE setup	Enable the 7.5 IRE setup	----
PALSA	When the PAL625 register is set to high, PAL-BDGHI mode is selected. When the PAL625 register is set to low, NTSC mode is selected.	When the PAL625 register is set to high, PAL-Nc mode is selected. When the PAL625 register is set to low, PAL-M mode is selected.	----

At slave mode, the W55VG580 will automatically detect the input video timing. The EFIELD, PAL625, INTERLACE, and SQUARE register will not be necessary. At master mode, the MODE[3:0] pins will set EFIELD, PAL625, INTERLACED and SQUARE registers. The YCSWAP, SETUP, and PALSA registers can be programmed by switching the W55VG580 to slave mode, then back to the master mode. At power-on, the YCSWAP, SETUP, and PALSA are set to zero.

The Relationship between TV System and Bit allocation

BITS[4:0]={ PALSA, PAL625, SQUARE, INTERLACE }

FL: Line Rate

FP: Pixel Rate

FSC: Sub-carrier Frequency

BITS[4:0]	FORMAT	PIXEL X LINE	FL	FP	FSC
0	M/NTSC, 601, NI	858x262	15734.264	13500000	3579545.00
1	M/NTSC, 601, I	858x525	15734.264	13500000	3579545.00
2	M/NTSC, S, NI	780x262	15734.264	12272727	3579545.00
3	M/NTSC, S, I	780x525	15734.264	12272727	3579545.00
4	BDGHIN/PAL, 601, NI	864x312	15625.000	13500000	4433618.75
5	BDGHIN/PAL, 601, I	864x625	15625.000	13500000	4433618.75
6	BDGHIN/PAL, S, NI	944x312	15625.000	14750000	4433618.75
7	BDGHIN/PAL, S, I	944x625	15625.000	14750000	4433618.75
8	M/PAL, 601, NI	858x262	15734.264	13500000	3575611.49
9	M/PAL, 601, I	858x525	15734.264	13500000	3575611.49
A	M/PAL, S, NI	780x262	15734.264	12272727	3575611.49
B	M/PAL, S, I	780x525	15734.264	12272727	3575611.49
C	Nc/PAL, 601, NI	864x312	15625.000	13500000	3582056.25
D	Nc/PAL, 601, I	864x625	15625.000	13500000	3582056.25
E	Nc/PAL, S, NI	944x312	15625.000	14750000	3582056.25
F	Nc/PAL, S, I	944x625	15625.000	14750000	3582056.25

5.3 Color space conversion

The 8-bit 4:2:2 YCrCb data input are linearly interpolated to 4:4:4 format and then converted to YUV format.

5.4 Low-pass filter

The U/V signal is low-passed by a digital filter specified by CCIR 624.

5.5 Modulator

The U and V color color-difference signals are modulated by a sub-carrier frequency generated by an internal DTO. After modulation, they are summed together to produce the luminance signal.

5.6 Video timing

The W55VG580 can operates in master mode and or slave mode. This is done by setting controlled by the MASTER pin. When the MASTER pin is set to logical low, the W55VG580 operates at in slave mode. When The the MASTER pin is set to logical high, the W55VG580 operates at in master mode.

At In master mode, the W55VG580 automatically generates the required timing from the CLK input. The HSYNCN and VSYNCN pins are output following the rising edge of CLK. Coincident falling edges of on HSYNCN and VSYNCN indicates the beginning of an odd field. A falling edge of on VSYNC without a coincident falling edge of on HSYNCN indicates the beginning of an even field.

At In slave mode, the W55VG580 accepts external horizontal and vertical synchronization signals via the HSYNCN and VSYNCN pins and automatically detects the input video format. The W55VG580 then generates the detected video timing.

The W55VG580 automatically calculates the width of the horizontal sync pulse and the start and end of the color burst. The color burst is automatically disabled, and serration and equalization pulses automatically inserted, on the appropriate lines. Serration and equalization pulses are automatically inserted into appropriate lines.

5.7 Video and Burst Blanking

Video and burst information is automatically disabled according to the Rec. CCIR 624.

5.8 Power Down

When the SLEEP pin is logical high, the W55VG580 enters sleep mode. The clock input and DAC outputs are disabled.

5.9 Analog outputs

There are two 8-bit D/A converter outputs: CVBS_Y and CVBS_C. These two outputs are specified to drive a 37.5 5- load. When the SVIDEO pin is connected to high, the CVBS_Y will output luminance signal, and CVBS_C will outputs a signal which that can be interfaced to the an S-Video machine. When the SVIDEO pin is connected to low, both the CVBS_Y and CVBS_C will output composite videos.

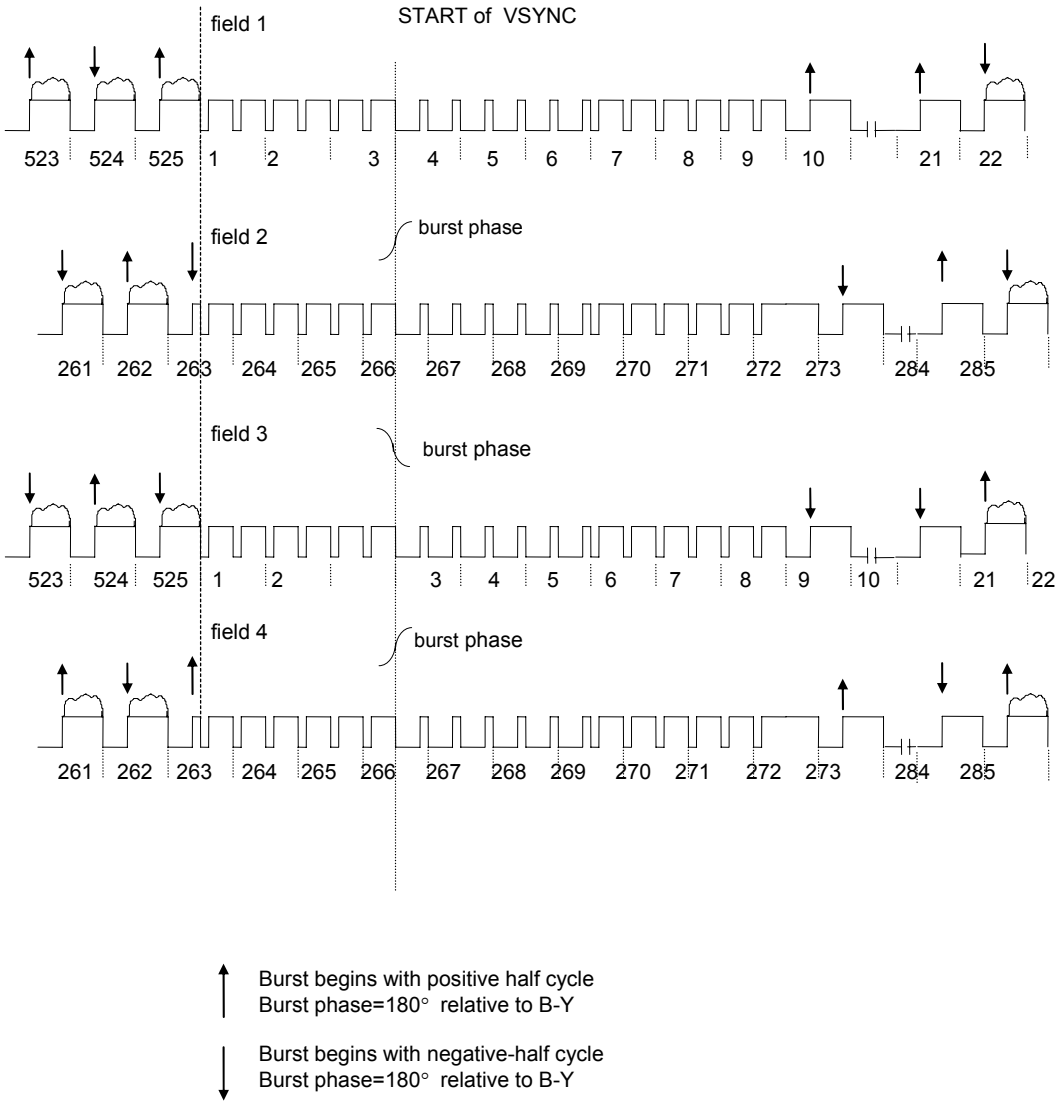


Figure 1. NTSC Interlace Video Timing

(SMPTE line conversion rather than CCIR-624 is used)

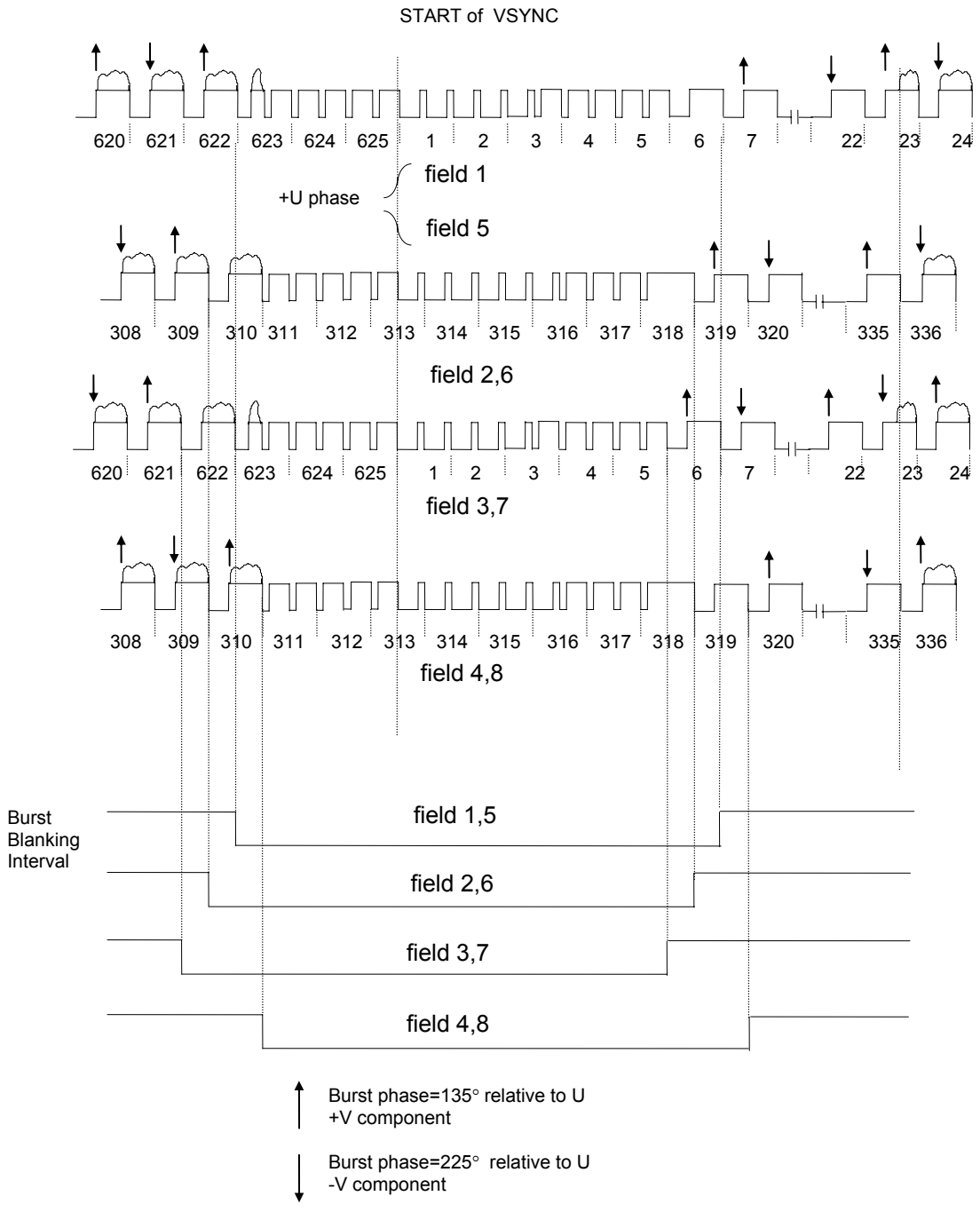


Figure 2. B,D,G,H,I/PAL Interlace Video Timing

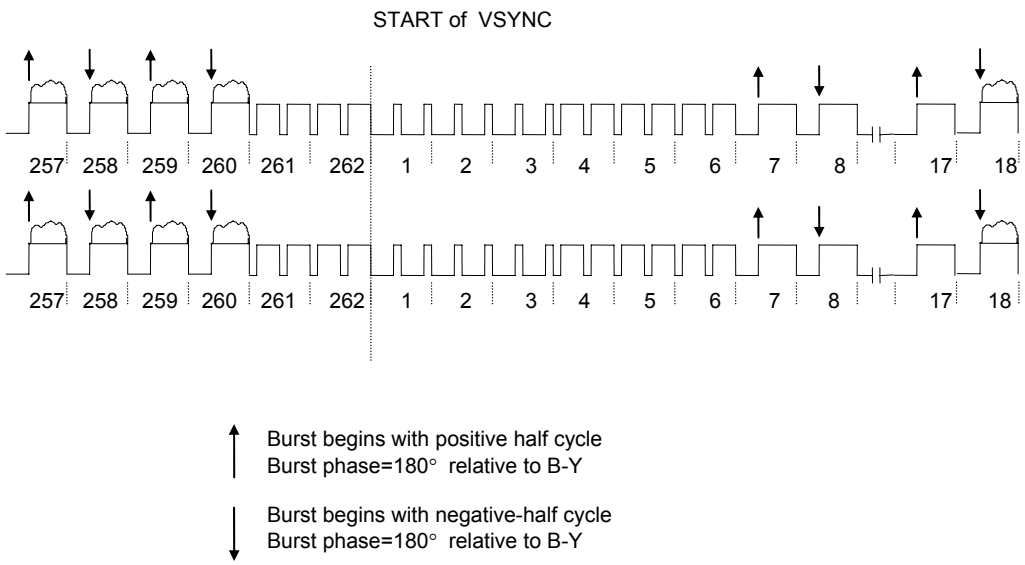


Figure 3. NTSC Non-interlace Video Timing

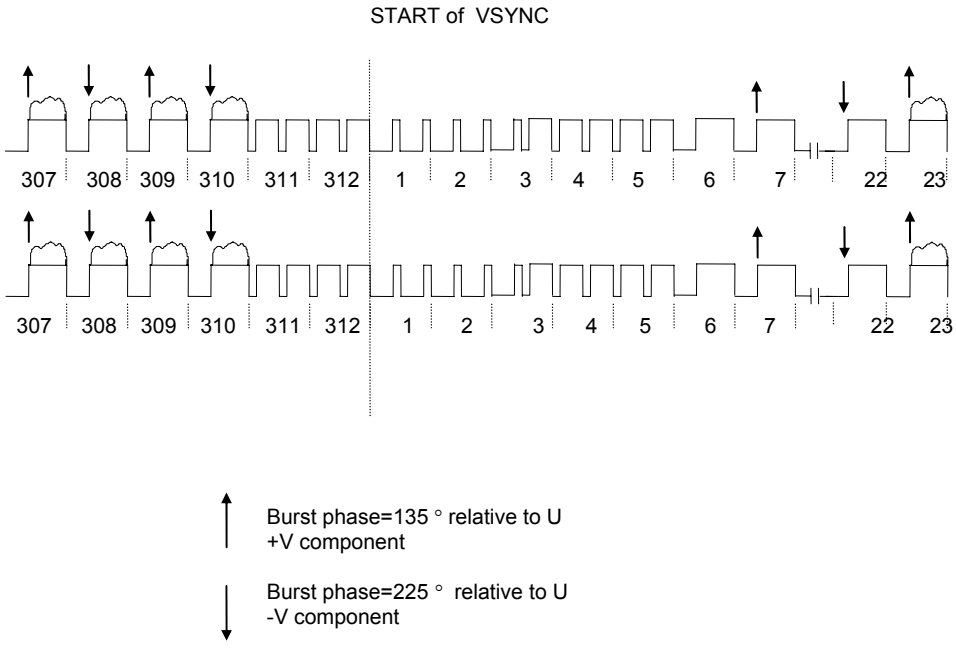


Figure 4. PAL Non-interlace Video Timing

6. ELECTRICAL CHARACTERISTICS

6.1 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0	--	70	C
DAC Output Load	RL	50	--	--	
External Voltage Reference	VREF_IN	1.14	1.235	1.26	V

6.2 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply (Measured to ground)	VAA	--	--	7	V
Ambient Operating Temperature	TA	-55	--	125	C
Voltage on Any Signal Pin	--	GND-0.5	--	VAA+0.5	V
Storage Temperature	TS	-65	--	+150	C
Junction Temperature	TJ	--	--	+150	C
Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latch up.					

6.3 DC Characteristics

(Recommended operating conditions using external voltage reference with RSET= 67 , VREFIN= 1.235V, NTSC CCIR 601 operation and clock frequency= 27 MHz at 25 C, +5V)

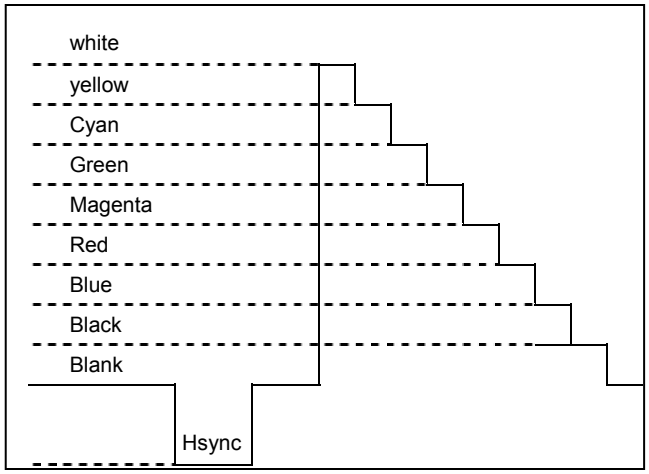
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VAA Supply Current	IAA@ 70 C IAA@ 0 C	-	100 100	tbd tbd	mA mA
Video D/A Resolution	-	8	8	8	Bits
Integral Nonlinearity	INL	-	-	+/- 1	LSB
Differential Nonlinearity	DNL	-	-	+/- 1	LSB
Maximum Output Current	-	-	-	26.04	mA
Output Compliance	VOC	0	-	1.5	V
Video level Error					
Using External Reference	-	-	-	5	%
Using Internal Reference	-	-	-	10	%
Full-Scale DAC Output	-	-	182.5	-	IRE
Digital Inputs	-	-	-	-	
Input High Voltage	VIH	2.0	-	VAA+0.5	V
Input Low Voltage	VIL	GND-0.5	-	0.8	V
Input High current (Vin=2.4V)	IIH	-	-	1	uA
Input Low current (Vin=0.4V)	IIL	-	-	-1	uA
Digital Outputs					
Output High Voltage (IOH=-400uA)	VOH	2.4	-		V
Output Low Voltage (IOL=3.2mA)	VOL	-	-	0.4	V
Three-State Current	IOZ	-	-	50	uA
VREF_IN Input Current	IREF_IN	-	10	-	uA
VREF_OUT Output Voltage	VREF_OUT	1.064	1.18	1.298	V
VREF_OUT current	IREF_OUT	-	10	-	uA

6.4 AC Characteristics

(Recommended operating conditions using external voltage reference with RSET=67 , VREFIN=1.235V, NTSC CCIR 601 operation and clock frequency=27 MHz at 25 C, +5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Luminance Bandwidth	-	-	Fin/4	-	MHz
Chrominance Bandwidth	-	-	1.3	-	MHz
Differential Gain	-	-	1	-	%
Differential Phase	-	-	1	-	
SNR	-	-	60	-	dB
Hue Accuracy	-	-	1.5	3	
Color Saturation Accuracy	-	-	1.5	3	%
Analog Output Delay	5	-	30	-	ns
Analog Output Rise Time	-	-	3	-	ns
Analog Output Settling Time	-	-	30	-	ns
Pixel/Control Setup Time	1	0	-	-	ns
Pixel/Control Hold Time	2	6	-	-	ns
Control Output Delay Time	3	-	15	-	ns
CLOCK Frequency	Fin	24.54	27	29.5	MHz
CLOCK Pulse Width Low Time	-	10	-	-	ns
CLOCK Pulse Width High Time	-	10	-	-	ns
Pipeline Delay	4	-	28	-	Clocks

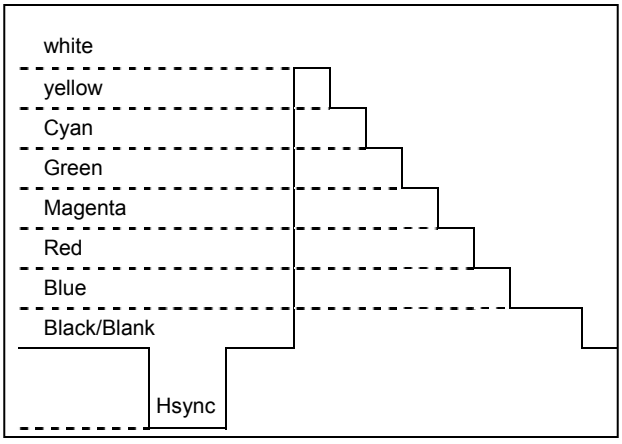
Level	HSYNC	BLANK	mA	V	IRE
White	1	1	20.42	1.021	100
Yellow	1	1	18.81	0.944	
Cyan	1	1	16.34	0.817	
Green	1	1	14.91	0.745	
Magenta	1	1	12.56	0.628	
Red	1	1	11.13	0.556	
Blue	1	1	8.58	0.429	
Black	1	1	7.20	0.360	7.5
Blank	1	0	6.13	0.306	0
Sync	0	0	0.41	0.02	-40



Note: 37.5Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

Figure 5. NTSC Y (Luminance) Output Waveform

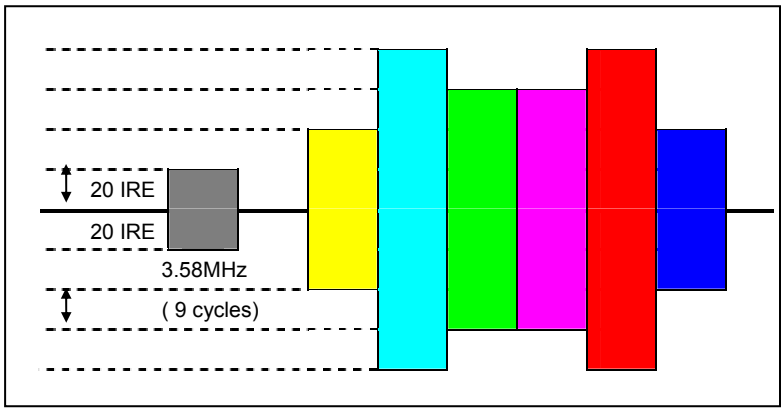
Level	HSYNC	BLANK	mA	V	IRE
White	1	1	20.82	1.041	100
Yellow	1	1	19.19	0.960	
Cyan	1	1	16.54	0.827	
Green	1	1	14.91	0.745	
Magenta	1	1	12.06	0.623	
Red	1	1	10.72	0.536	
Blue	1	1	8.17	0.408	
Black/ Blank	1	1	6.53	0.327	0
Sync	0	0	0.41	0.020	-43



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIRCCIR 624 levels and tolerance are assumed.

Figure 6. PAL-BDGHI Y (Luminance) Output Waveform

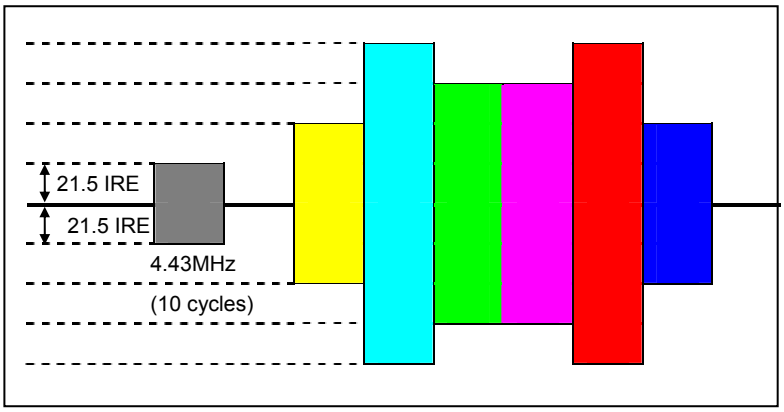
Color	mA	V
Cyan/Red	21.44	1.071
Green/magenta	20.93	1.047
Yellow/Blue	28.99	0.950
Peak Burst	15.92	0.794
Blank	13.07	0.653
Peak Burst	10.21	0.510
Yellow Blue	7.15	0.357
Green/Magenta	5.21	0.260
Cyan/Red	4.7	0.235



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

Figure 7. NTSC C (Chroma) Output Waveform

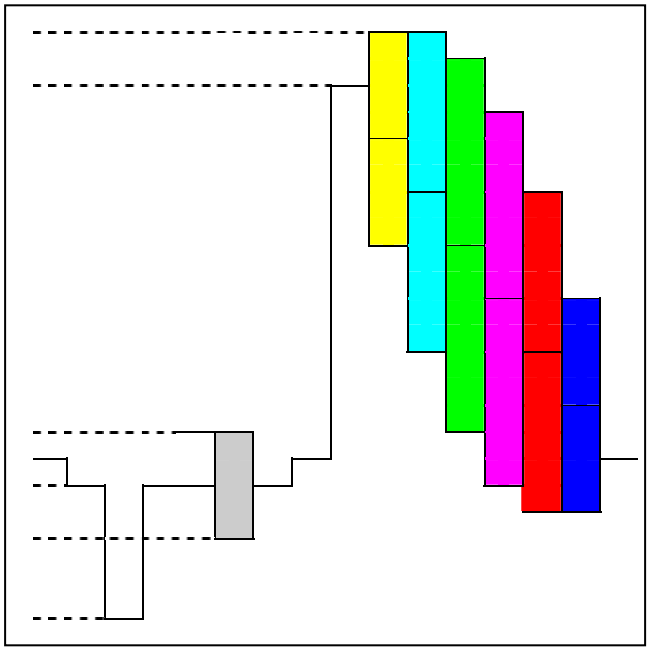
Color	mA	V
Cyan/Red	22.15	1.107
Green/magenta	21.54	1.077
Yellow/Blue	19.50	0.975
Peak Burst	16.13	0.806
Blank	13.07	0.653
Peak Burst	10.00	0.500
Yellow Blue	6.64	0.332
Green/Magenta	4.59	0.230
Cyan/Red	3.98	0.199



Note: 37.5 Ω load is used. VREF_IN=1.235V RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIR 624 levels and tolerance are assumed.

Figure 8. PAL-BDGHI C (Chroma) Output Waveform

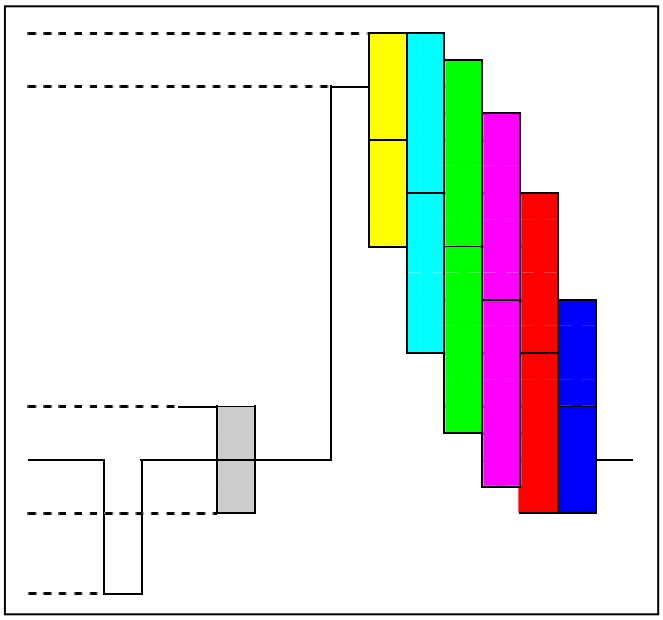
Color/Level	HSYNC	BLANK	mA	V	IRE
Peak Chroma	1	1	24.80	1.240	134
White	1	1	20.42	1.021	100
Peak Burst	1	1	8.99	0.449	20
Black	1	1	7.20	0.360	7.5
Blank	1	0	6.13	0.306	0
Peak Burst	1	0	3.27	0.164	-20
SYNC	0	0	0.41	0.020	-40



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

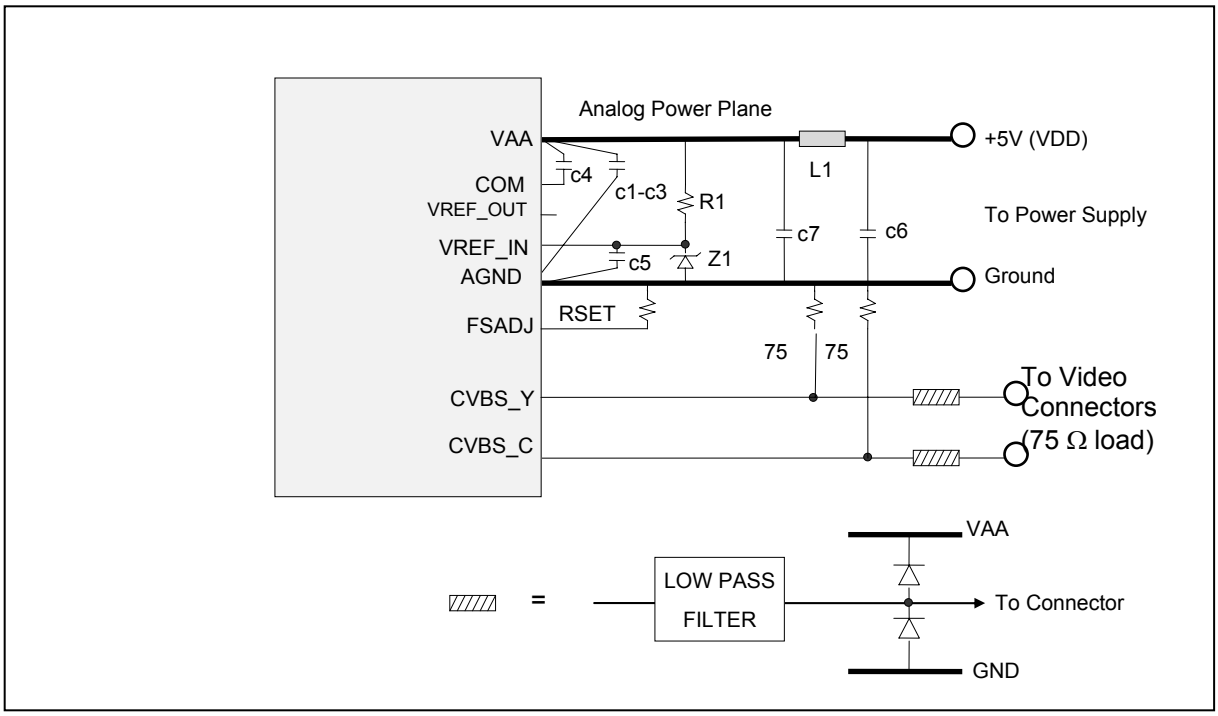
Figure 9. NTSC Composite Output Waveform

Color/Level	HSYNC	BLANK	mA	V	IRE
Peak Chroma	1	1	25.61	1.281	133
White	1	1	20.82	1.041	100
Peak Burst	1	1	9.59	0.480	21.5
Black/Blank	1	0	6.53	0.327	0
Peak Burst	1	0	3.47	0.174	-21.5
SYNC	0	0	0.41	0.02	-43



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIR 624 levels and tolerance are assumed.

Figure 10. PAL-BDGHI Composite Output Waveform



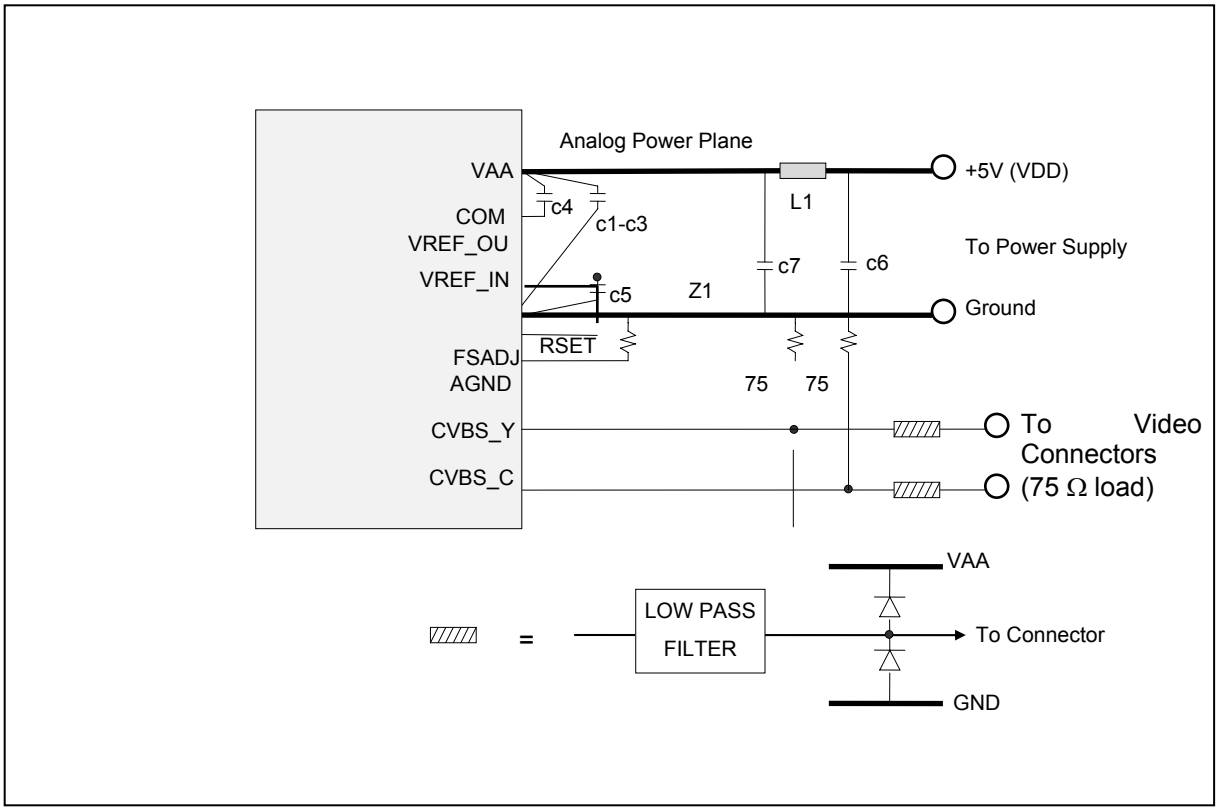
PART NUMBER	VALUE	VENDOR NUMBER
c1-c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
R1	1KW (5%)	
RSET	1% Metal Film	Dale CMF-55C
Z1	1.2V Zener Diode	LM358BZ-1.2

Note: 1. The vendor number is are only for reference.

2. RSET is determined by (Iout=full scale output current)

$$RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$$

Figure 11. Typical connection diagram and part list(using external voltage reference)



PART NUMBER	VALUE	VENDOR NUMBER
c1-c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
RSET	1% Metal Film	Dale CMF-55C

Note: 1. The vendor number is are only for reference.

2. RSET is determined by (Iout=full scale output current)

$$RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$$

Figure 12. Typical connection diagram and part lis (using internal voltage reference)

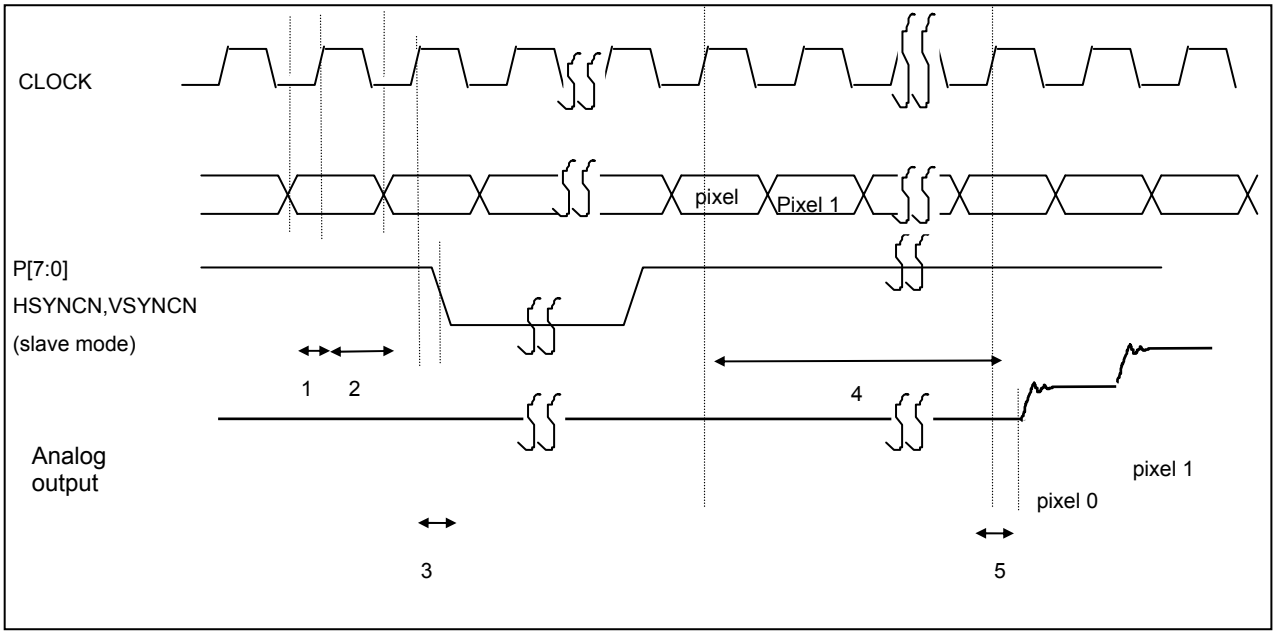


Figure 13. Video Input and Output Timing

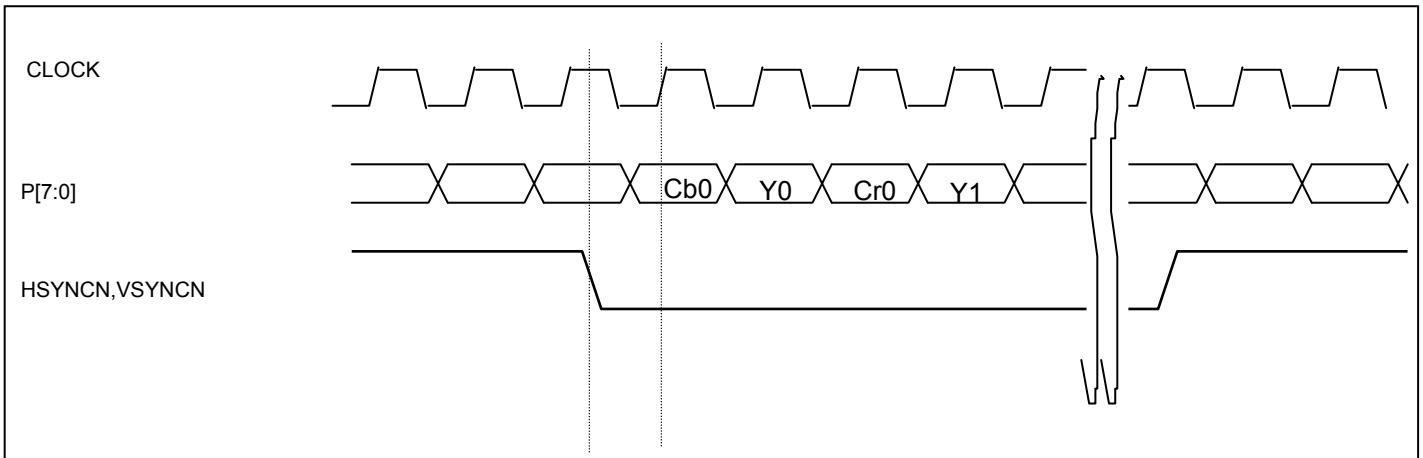
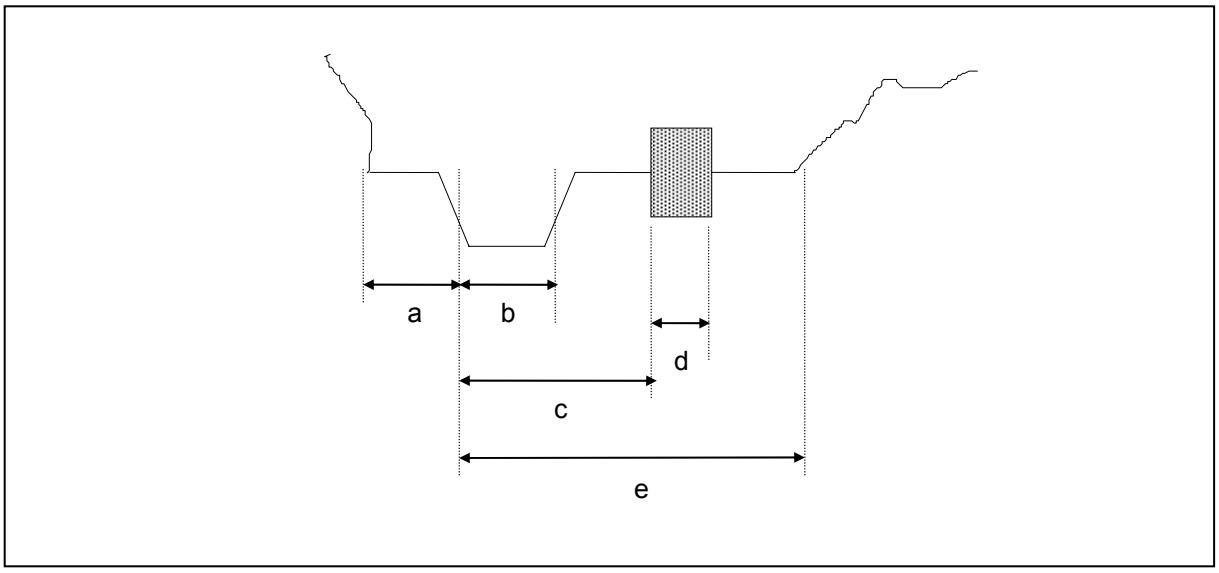


Figure 14. pixel sequence at power on reset
(The pixel sequence can be swap changed by setting the CBSWAP pin and the MODE[3] pin at in slave mode)

OPERATING MODE	ACTIVE PIXELS	TOTAL PIXELS	CLK FREQUENCY (MHZ)
NTSC/PAL-M CCIR601CCIR 601	720 x 240	858 x 262	27
PAL-B,D,G,H,I,Nc	720 x 288	864 x 313	27
NTSC/PAL-M Square pixel	640 x 240	780 x 262	24.545454
PAL-B,D,G,H,I,Nc Square pixel	768 x 288	944 x 312	29.5

Table1. Field Resolution and clock Rates for Various Modes of Operation



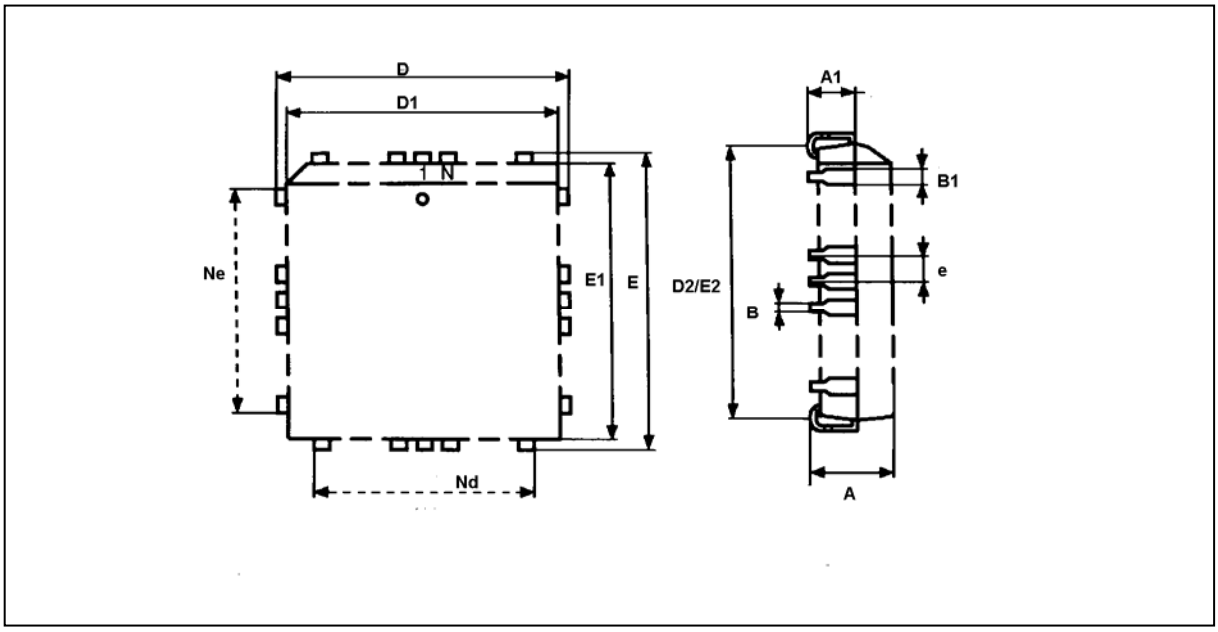
OPERATION MODE	FRONT PORCH (E)	HORIZONTAL SYNC WIDTH (B)	START OF BURST (C)	DURATION OF BURST (D)	BACK PORCH (E)
NTSC CCIR601CCIR 601	20	63	72	34	127
PAL-M CCIRCCIR 610	20	63	78	34	127
PAL-B CCIR601CCIR 601	20	63	76	30	142
PAL-Nc CCIR601CCIR 601	20	63	76	34	142
NTSC SQUARE	18	58	65	31	115
PAL-M SQUARE	18	58	71	31	115
PAL-B SQUARE	22	69	83	33	155
PAL-Nc SQUARE	22	69	83	37	155
Notes: (1) The unit is the number of luminance pixels.					

Table 2. Various Video Timing

7. PACKAGE INFORMATION

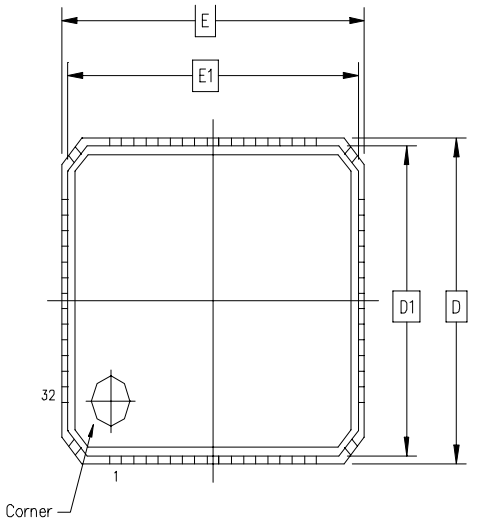
PART NO.	PACKAGE	AMBIENT TEMPERATURE RANGE
W55VG580P	PLCC-32	0 °C ~70 °C
W55VG580YG	QFN-32	0 °C ~70 °C
W55VG580H	Chip form	0 °C ~70 °C
W44VG580W	Wafer form	0 °C ~70 °C

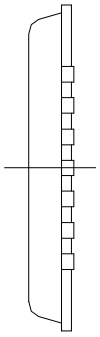
plcc

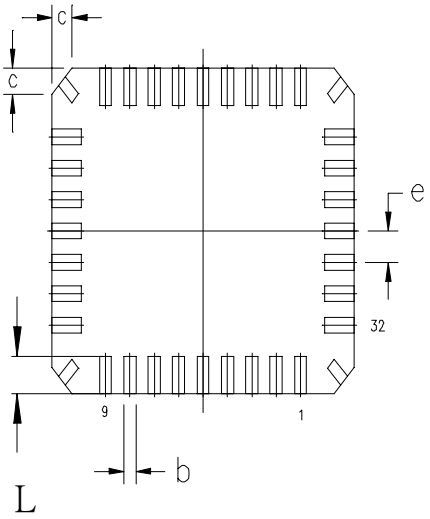


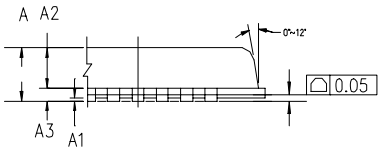
SYMBOL	INCHES			MM		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.1		0.14	2.54		3.56
A1	0.06		0.095	1.52		2.41
B	0.013		0.021	0.33		0.53
B1	0.026		0.032	0.66		0.81
D	0.485		0.495	12.32		12.57
D1	0.447		0.455	11.35		11.56
D2	0.39		0.43	9.91		10.92
E	0.585		0.595	14.86		15.11
E1	0.547		0.555	13.89		14.1
E2	0.49		0.53	12.54		13.46
e		0.05			1.27	
N					32	
Nd					7	
Ne					9	

QFN-32





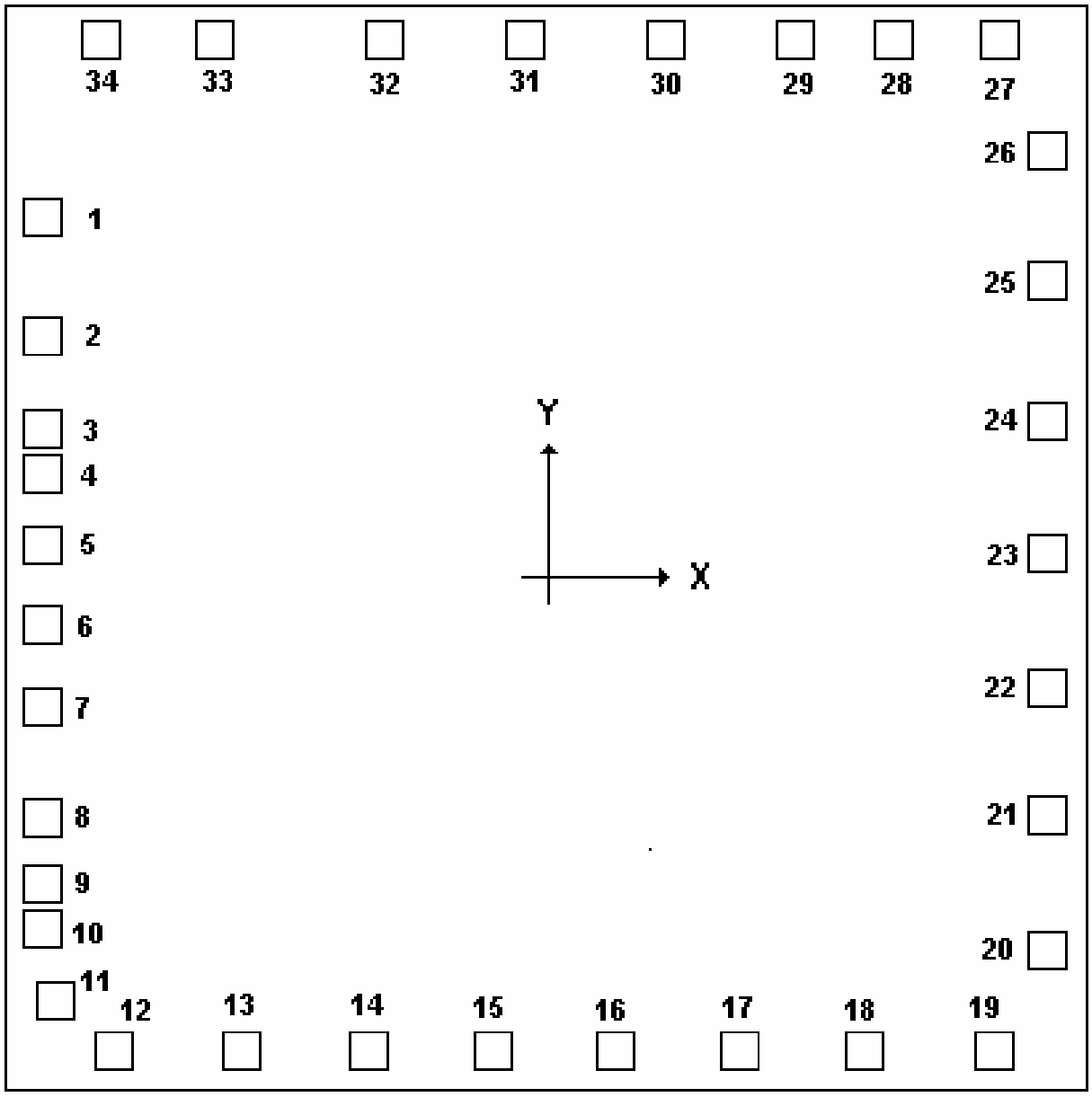




Cotrol Dimensions :Millmeters

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	---	1.00	0.0314	---	0.0394
A1	0.00	0.02	0.05	0.0000	0.0007	0.0019
A2	0.65	---	0.69	0.0255	---	0.0271
A3	0.203 REF.			0.0079 REF.		
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
C	0.24	0.42	0.60	0.0094	0.0165	0.0236
D	5.20 BSC			0.2047 BSC		
D1	4.95 BSC			0.1948 BSC		
E	6.20 BSC			0.2440 BSC		
E1	5.95 BSC			0.2342 BSC		
e	0.50 BSC			0.0196 BSC		
L	0.50	0.60	0.70	0.0196	0.0236	0.0275

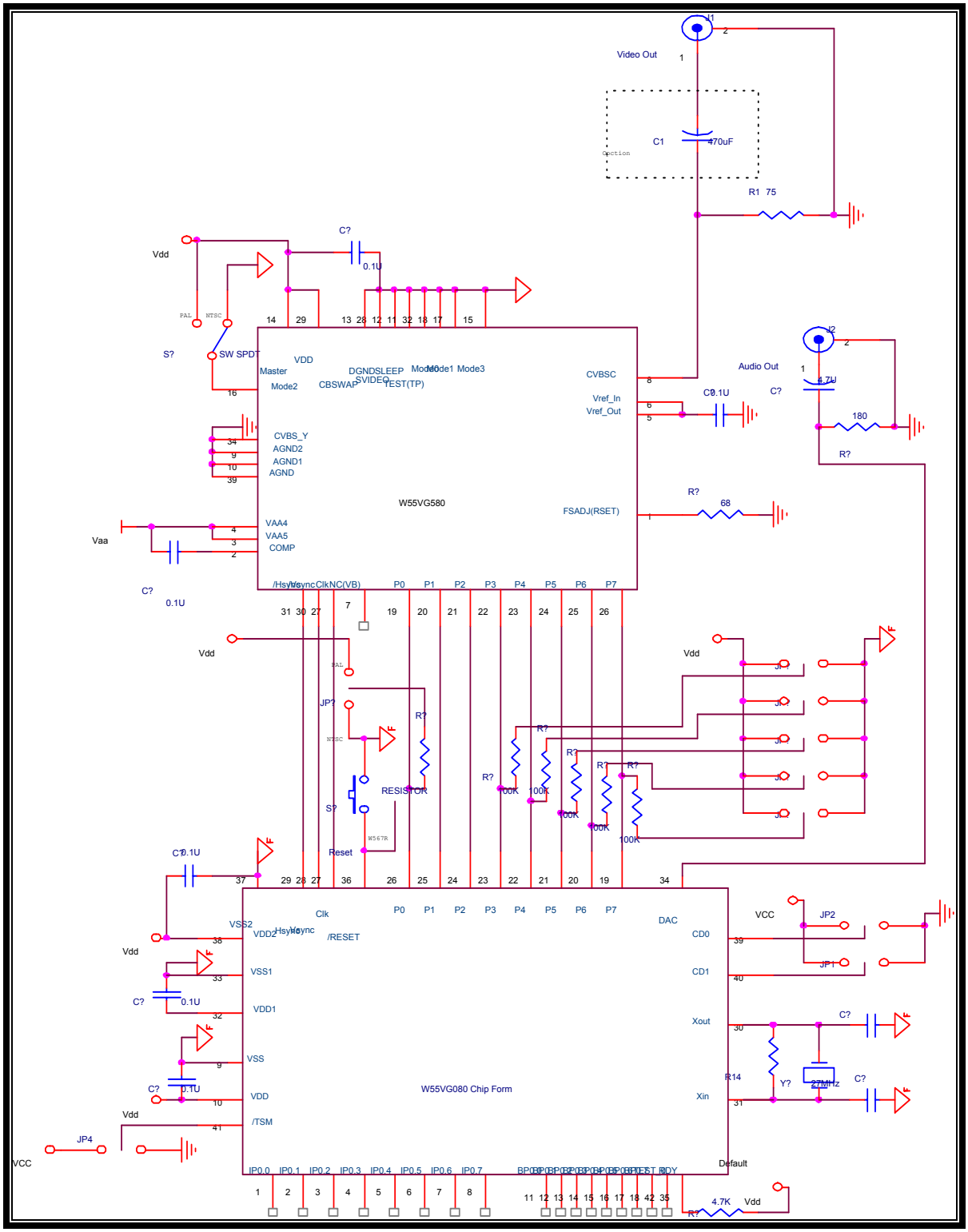
W55VG580H Bonding Pad Diagram



Window: (xl = -1435.00, yl = -1485.00), (xh = 1435.00, yh = 1485.00). Windows size: width = 2870.00, length = 2970.00

PAD NO.	PAD NAME	X(μM)	Y(μM)	PAD NO.	PAD NAME	X(μM)	Y(μM)
1	FSADJ	-1338.56	855.24	18	MODE <0>	828.54	-1342.30
2	COMP	-1338.56	538.31	19	P<0>	1156.74	-1342.30
3	VAA	-1338.56	297.44	20	P<1>	1287.84	-1063.60
4	VAA	-1338.56	212.44	21	P<2>	1287.84	-713.23
5	VREF_OUT	-1338.56	-6.37	22	P<3>	1287.84	-364.45
6	VREF_IN	-1338.56	-212.14	23	P<4>	1287.84	-14.08
7	NC	-1338.56	-451.27	24	P<5>	1287.84	334.70
8	CVBS_C	-1338.56	-711.12	25	P<6>	1287.84	685.08
9	AGND	-1338.56	-898.11	26	P<7>	1287.84	1033.85
10	AGND	-1338.56	-983.11	27	CLK	1155.92	1313.03
11	SLEEP	-1293.56	-1211.20	28	DGND	883.02	1313.03
12	SVIDEO	-1135.86	-1342.30	29	VDD	636.54	1313.03
13	CBSWAP	-807.66	-1342.30	30	VSYNCN	288.47	1313.03
14	MASTER	-481.06	-1342.30	31	HSYNCN	-76.41	1313.03
15	MODE <3>	-152.86	-1342.30	32	TEST	-442.89	1313.03
16	MODE <2>	173.74	-1342.30	33	AGND	-882.55	1313.03
17	MODE <1>	501.94	-1342.30	34	CVBS_Y	-1192.35	1313.03

8. APPLICATION CIRCUIT



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