



Data Book

AU6369

**USB 2.0 Single-Slot
Flash Memory Card Reader
Technical Reference Manual**

Product Specification

Official Release

Revision 3.02W

Public

Sep 2005



Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Dec 2004	2.00W	Official release
Apr 2004	2.01W	To modify the "4.2 sample schematics"
May 2005	2.02W	To modify "3.0 Power Switch Feature"
Sep 2005	3.02W	<ol style="list-style-type: none">1. Add 64 LQFP package information2. To modify "5.2 Recommended Operating Conditions"3. Moved "3.0 Power Switch Feature" to "5.6 Power Switch Feature"4. Removed the schematics. Please contact our sales if you need it.



Copyright Notice

Copyright 1997 - 2004
Alcor Micro Corp.
All Rights Reserved.

Trademark Acknowledgements

The company and product names mentioned in this document may be the trademarks or registered trademarks of their manufacturers.

Disclaimer

Alcor Micro Corp. reserves the right to change this product without prior notice. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without prior notice.

Contact Information:

Web site: <http://www.alcormicro.com/>

Taiwan

Alcor Micro Corp.
4F, No 200 Kang Chien Rd., Nei Hu,
Taipei, Taiwan, R.O.C.
Phone: 886-2-8751-1984
Fax: 886-2-2659-7723

Santa Clara Office

2901 Tasman Drive, Suite 206
Santa Clara, CA 95054
USA
Phone: (408) 845-9300
Fax: (408) 845-9086

Los Angeles Office

9070 Rancho Park Court
Rancho Cucamonga, CA.91730
USA
Phone: (909) 483-9900
Fax: (909) 944-0464



Table of Contents

1	Introduction	6
	1.1 Description	6
	1.2 Features	6
2	Application Block Diagram	7
3	Pin Assignment	8
4	System Architecture and Reference Design	20
	4.1 AU6369Block Diagram	20
5	Electrical Characteristics	21
	5.1 Absolute Maximum Ratings	21
	5.2 Recommended Operating Conditions	21
	5.3 General DC Characteristics	21
	5.4 DC Electrical Characteristics for 5 volts operation	22
	5.5 USB Transceiver Characteristics	22
	5.6 Power Switch Feature	26
6	Mechanical Information	27
7	Abbreviations	29



List of Figures

2.1	Block Diagram	7
3.1	48 Pin (SD/MS) Assignment Diagram	8
3.2	64 Pin (SD/MS/xD) Assignment Diagram	11
3.3	64 Pin (CF) Assignment Diagram	14
3.4	64 Pin (xD/SMC) Assignment Diagram	17
4.1	AU6369 Block diagram	20
5.1	Card Detect Power-on Timing	26
6.1	48 LQFP Mechanical Information Diagram	27
6.2	64 LQFP Mechanical Information Diagram	28

List of Tables

3.1	48 Pin (SD/MS) Descriptions	9
3.2	64 Pin (SD/MS/xD) Descriptions	12
3.3	64 Pin (CF) Descriptions	15
3.4	64 Pin (xD/SMC) Descriptions	18
5.1	Absolute Maximum Ratings	21
5.2	Recommended Operating Conditions	21
5.3	General DC Characteristics	21
5.4	DC Electrical Characteristics of 3.3V I/O Cells	22
5.5	Recommended Operation Conditions	22
5.6	Static characteristic : Digital in	22
5.7	Static characteristic : Analog I/O pins (DP/DM)	24
5.8	Dynamic characteristic : Analog I/O pins (DP/DM)	25



1.0 Introduction

1.1 Description

The AU6369 is a highly integrated single chip memory card reader controller. It supports USB v2.0 high-speed transmission to the entire popular storage media interface on one chip, such as, Compact Flash (CF), Secure Digital (SD), Multi Media Card (MMC), Micro Drive (MD), Memory Stick (MS, MS Pro, MS Duo), Digital photo (xD) and Smart Media Card (SMC).

The AU6369 supports USB v2.0 and USB v1.0 Storage Class specification. It can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6369, users can transfer digital data between flash memory card and PC or these electronic devices.

The integration of various mixed mode makes component AU6369 is the most powerful and most effective solution for single-slot flash memory reader.

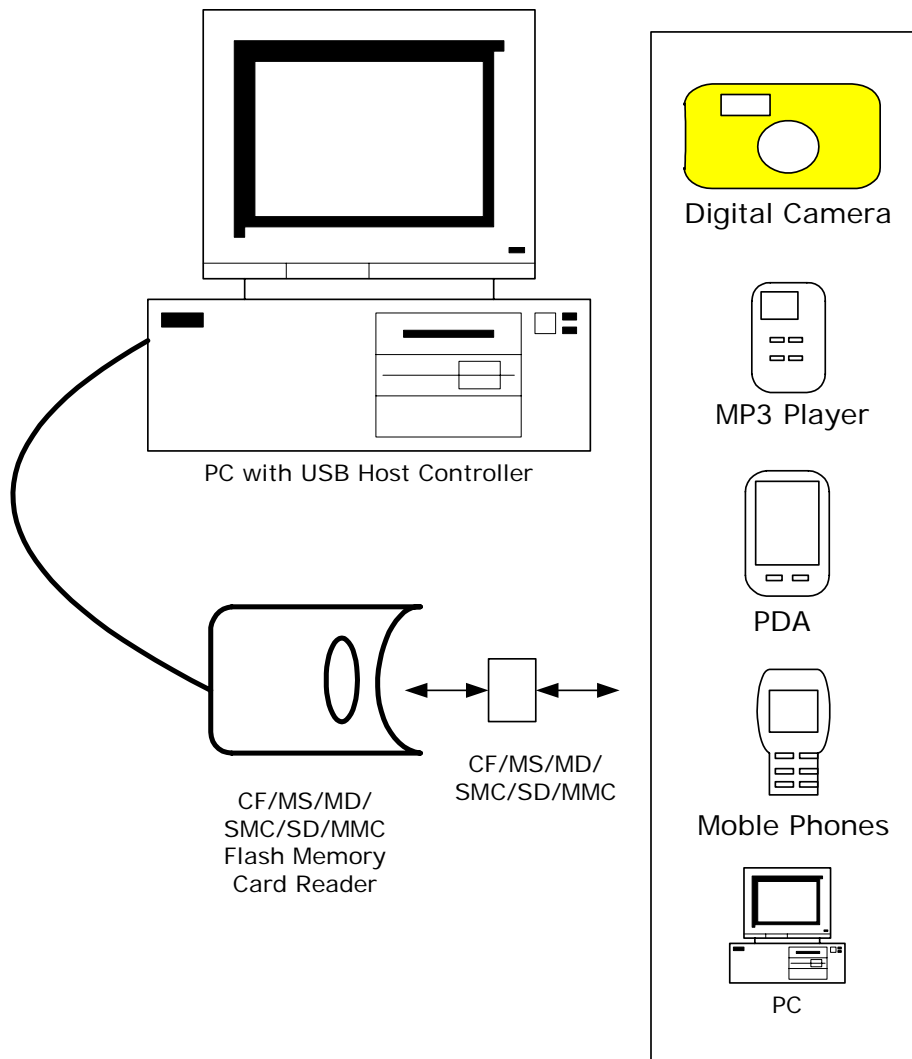
1.2 Features

- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial interface Engine
- Support CF/MD, SD/MMC, MS/MS PRO/MS ROM/MS Duo and xD/SMC specification
- Work with default driver from Windows ME, Windows XP, and Mac OS X. Windows 98, Windows 2000 are supported by vendor AP from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support auto-detecting slot with card inserted on Win 2000 without driver.
- Support LED for bus activity indication.
- CPU Runs at 30MHz, built-in 480MHz PLL

2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6369. By connecting the card reader to a desktop or notebook PC through USB bus, AU6369 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram





3.0 Pin Assignment

The AU6369 is packed in 48pin/64pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 3.1 48 Pin (SD/MS) Assignment Diagram

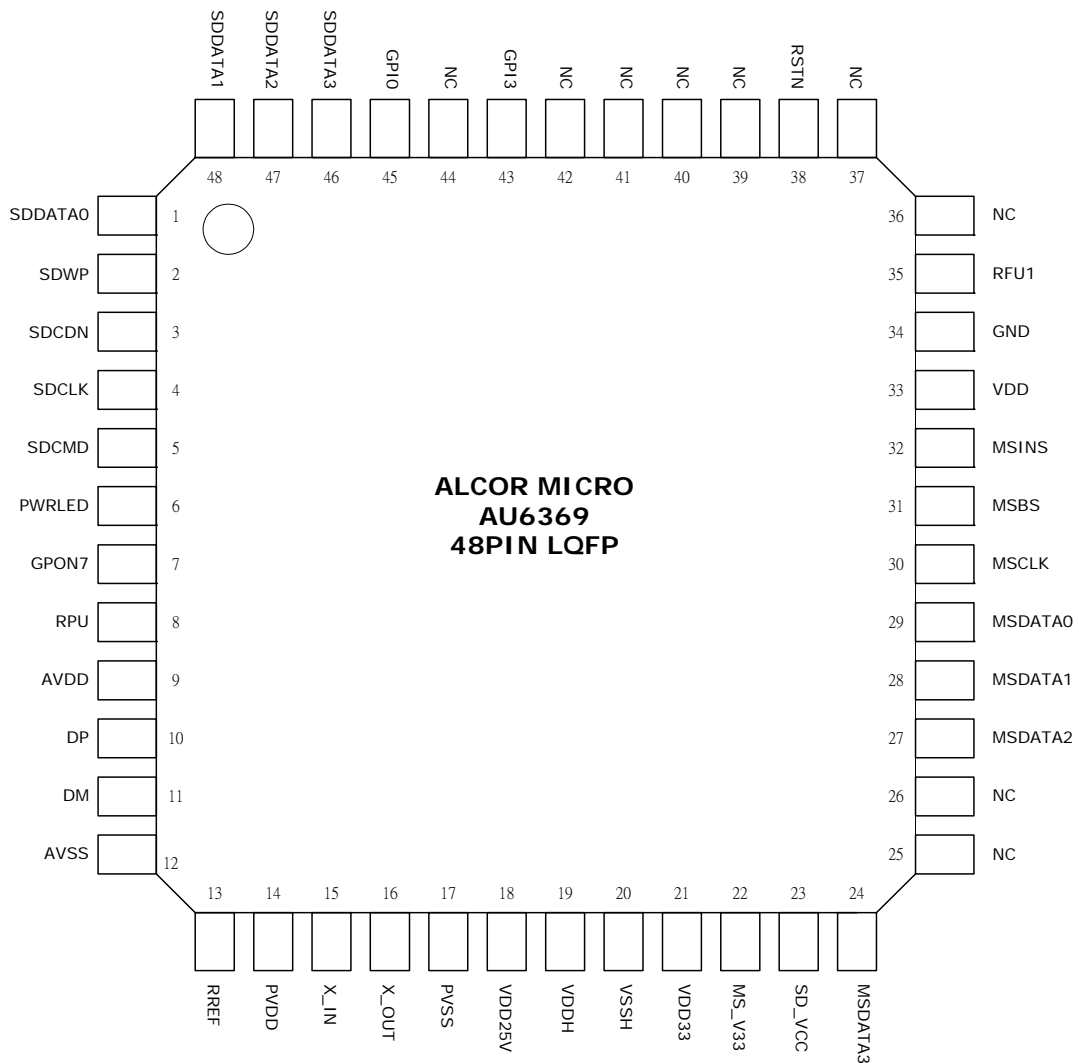




Table 3.1 48 Pin (SD/MS) Descriptions

Pin #	Pin Name	I/O	Description
1	SDDATA0	I/O	SD Data0
2	SDWP	I	SD Write Protect
3	SDCDN	I	SD Card Detect
4	SDCLK	O	SD CLK
5	SDCMD	I/O	SD CMD
6	PWRLED	O	Power LED; (Normal:"0"; Suspend"1")
7	GPON7	O	Data transferring LED; (Data transferring:"0"; Standby:"1")
8	RPU	I	Connected with an 1.5k pull up resistor to 3.3 VDD
9	AVDD	I	Analog Power 3.3V
10	DP	I/O	USB DP
11	DM	I/O	USB DM
12	AVSS	PWR	Analog Ground
13	RREF	I	Connected an 1k resistor to GND for impedance match
14	PVDD	I	OSC Power 3.3V
15	X_IN	I	12 MHz crystal input.
16	X_OUT	O	12 MHz crystal output.
17	PVSS	PWR	OSC Ground
18	VDD25V	O	Core Power 2.5V
19	VDDH	I	IO Power 3.3V
20	VSSH	PWR	IO Ground
21	VDD33	I	Switch Power 3.3V
22	MS_V33	O	MS Card Power
23	SD_VCC	O	SD Card Power
24	MSDATA3	I/O	MS Data3
25	NC		
26	NC		
27	MSDATA2	I/O	MS Data2
28	MSDATA1	I/O	MS Data1
29	MSDATA0	I/O	MS Data0
30	MSCLK	O	MS CLK
31	MSBS	O	MS BS
32	MSINS	I	MS Card Detect (Insert:"0"; Extraction:"1"; Default:"1")
33	VDD	I	Core power 2.5V
34	GND	PWR	Core Ground
35	RFU1	I	External pull up with 470K to 3.3V.
36	NC		
37	NC		
38	RSTN	I	Chip Reset (Reset:"0"; Normal:"1"), pull up with RC
39	NC		
40	NC		
41	NC		



42	NC		
43	GPI3	I	Reserved
44	NC		
45	GPI0	I	Always pull high
46	SDDATA3	I/O	SD Data3
47	SDDATA2	I/O	SD Data2
48	SDDATA1	I/O	SD Data1



Figure 3.2 64 Pin (SD/MS/xD) Assignment Diagram

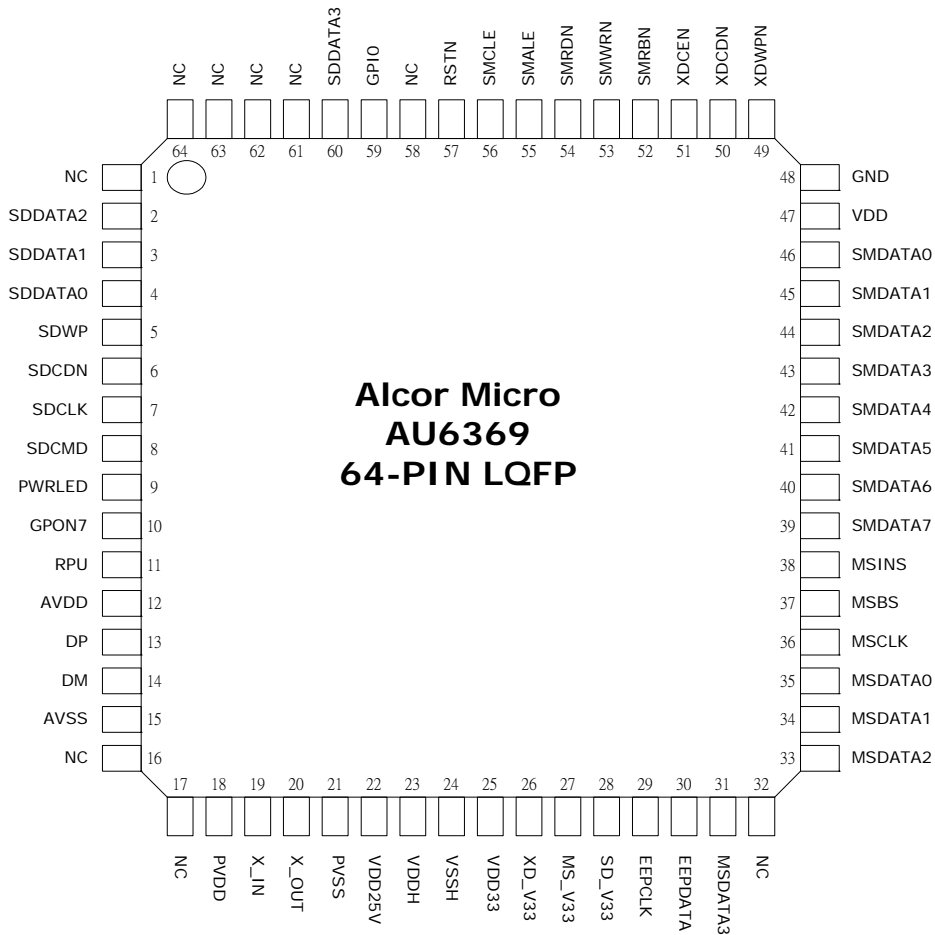




Table 3.2 64 Pin (SD/MS/xD) Descriptions

Pin #	Pin Name	I/O	Description
1	NC		
2	SDDATA2	I/O	SD Data2
3	SDDATA1	I/O	SD Data1
4	SDDATA0	I/O	SD Data0
5	SDWP	I	SD Write Protect
6	SDCDN	I	SD Card Detect
7	SDCLK	O	SD CLK
8	SDCMD	I/O	SD CMD
9	PWRLED	O	Power LED; (Normal:"0"; Suspend"1")
10	GPON7	O	Card insert LED; (Card inserted:"0";
11	RPU	I	Connected with an 3.9k pull up resistor to 3.3 VDD
12	AVDD	I	Analog Power 3.3V
13	DP	I/O	USB DP
14	DM	I/O	USB DM
15	AVSS	PWR	Analog Ground
16	NC		
17	NC		
18	PVDD	I	OSC Power 3.3V
19	X_IN	I	12 MHz crystal input.
20	X_OUT	O	12 MHz crystal output.
21	PVSS	PWR	OSC Ground
22	VDD25V	O	Core Power 2.5V
23	VDDH	I	IO Power 3.3V
24	VSSH	PWR	IO Ground
25	VDD33	I	Switch Power 3.3V
26	XD_V33	O	XD Card Power
27	MS_V33	O	MS Card Power
28	SD_V33	O	SD Card Power
29	EEPCLK	O	EEPROM Clock
30	EEPDATA	I/O	EEPROM Data
31	MSDATA3	I/O	MS Data3
32	NC		
33	MSDATA2	I/O	MS Data2
34	MSDATA1	I/O	MS Data1
35	MSDATA0	I/O	MS Data0
36	MSCLK	O	MS CLK
37	MSBS	O	MS BS
38	MSINS	I	MS Card Detect (Insert:"0"; Extraction:"1"; Default:"1")
39	SMDATA7	I/O	SM Data7
40	SMDATA6	I/O	SM Data6
41	SMDATA5	I/O	SM Data5
42	SMDATA4	I/O	SM Data4
43	SMDATA3	I/O	SM Data3



44	SMDATA2	I/O	SM Data2
45	SMDATA1	I/O	SM Data1
46	SMDATA0	I/O	SM Data0
47	VDD	I	Core power 2.5V
48	GND	PWR	Core Ground
49	XDWPN	O	XD WP
50	XDCDN	I	XD CD
51	XDCEN	O	XD CE
52	SMRBN	I	External pull up with 470K to 3.3V.
53	SMWRN	O	SM WR
54	SMRDN	O	SM RD
55	SMALE	O	SM ALE
56	SMCLE	O	SM CLE
57	RSTN	I	Chip Reset (Reset: "0"; Normal: "1"), pull up with RC
58	NC		
59	GPIO	I	Always pull high
60	SDDATA3	I/O	SD Data3
61	NC		
62	NC		
63	NC		
64	NC		



Figure 3.3 64 Pin (CF) Assignment Diagram

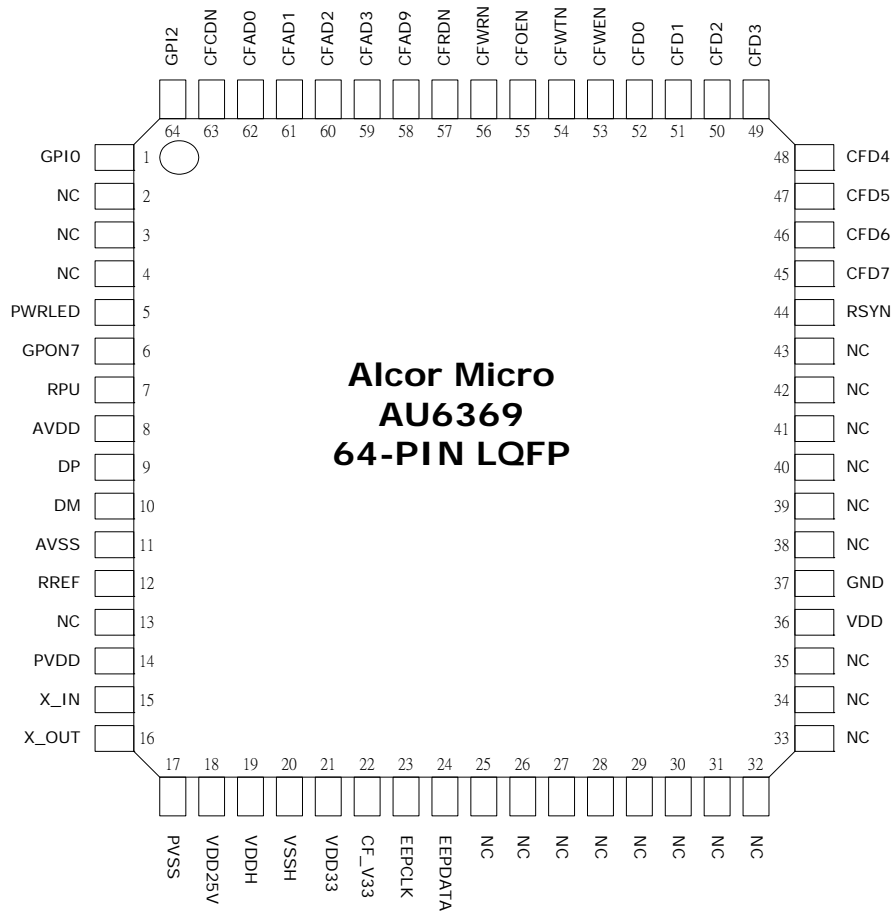




Table 3.3 64 Pin (CF) Descriptions

Pin #	Pin Name	I/O	Description
1	GPI0	I	Always pull high
2	NC		
3	NC		
4	NC		
5	PWRLED	O	Device LED
6	GPON7	O	Card operating LED
7	RPU	I	Connected with an 1.5k pull up resistor to 3.3 VDD
8	AVDD	I	Analog Power 3.3V
9	DP	I/O	USB DP
10	DM	I/O	USB DM
11	AVSS	PWR	Analog Ground
12	RREF	I	Connected an 1k resistor to GND for impedance match
13	NC		
14	PVDD	I	OSC Power 3.3V
15	X_IN	I	12 MHz crystal input.
16	X_OUT	O	12 MHz crystal output.
17	PVSS	PWR	OSC Ground
18	VDD25V	O	Core Power 2.5V
19	VDDH	I	IO Power 3.3V
20	VSSH	PWR	IO Ground
21	VDD33	I	Switch Power 3.3V
22	CF_V33	O	CF card power
23	EEPCLK	O	EEPROM serial clock.
24	EEPDATA	I/O	EEPROM for PID,VID customization.
25	NC		
26	NC		
27	NC		
28	NC		
29	NC		
30	NC		
31	NC		
32	NC		
33	NC		
34	NC		
35	NC		
36	VDD	I	Core power 2.5V
37	GND	PWR	Core Ground
38	NC		
39	NC		
40	NC		
41	NC		
42	NC		
43	NC		
44	RSTN	I	Chip Reset ("0":Reset; "1":Normal), pull up



			with RC
45	CFD7	I/O	CF Data7
46	CFD6	I/O	CF Data6
47	CFD5	I/O	CF Data5
48	CFD4	I/O	CF Data4
49	CFD3	I/O	CF Data3
50	CFD2	I/O	CF Data2
51	CFD1	I/O	CF Data1
52	CFD0	I/O	CF Data0
53	CFWEN	O	CF WEN
54	CFWTN	I	CF WTN
55	CFOEN	O	CF OEN
56	CFWRN	O	CF WRN
57	CFRDN	O	CF RDN
58	CFAD9	O	CF Address9
59	CFAD3	O	CF Address3
60	CFAD2	O	CF Address2
61	CFAD1	O	CF Address1
62	CFAD0	O	CF Address0
63	CFCDN	I	CF CDN
64	GPI2	I	USB current value description ("1": 100mA[Default]; "0": 250mA)



Figure 3.4 64 Pin (xD/SMC) Assignment Diagram

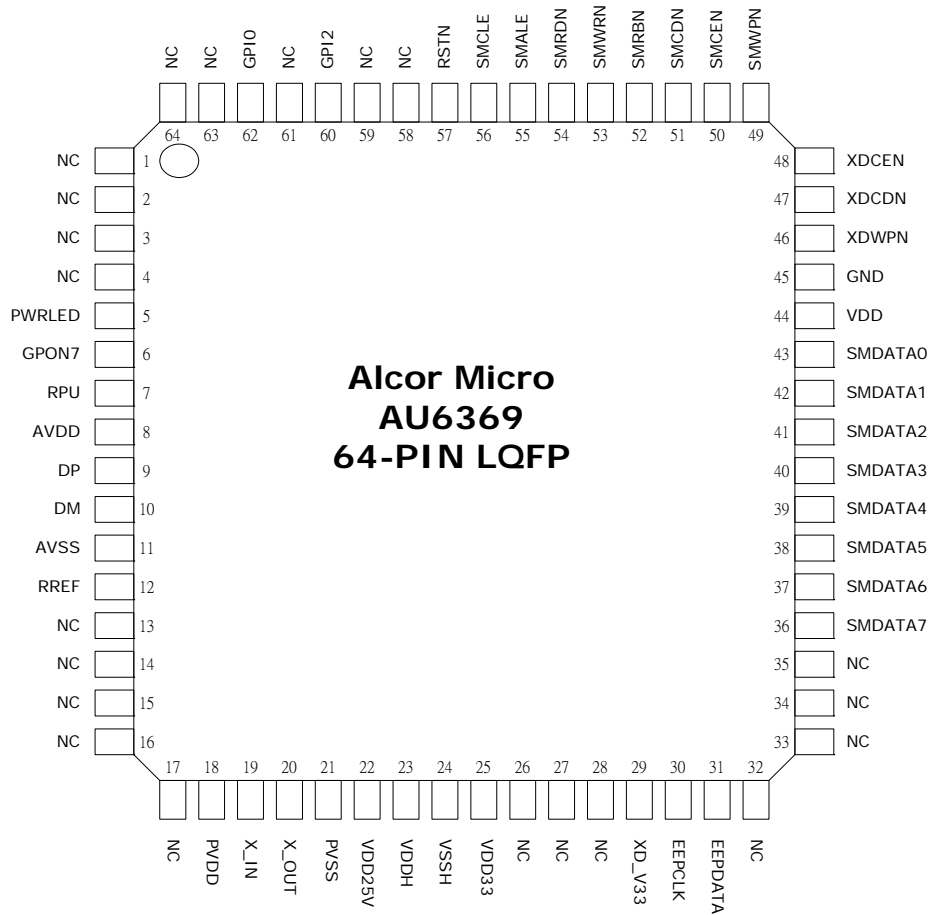




Table 3.4 64 Pin (xD/SMC) Descriptions

Pin #	Pin Name	I/O	Description
1	NC		
2	NC		
3	NC		
4	NC		
5	PWRLED	O	Power LED; (Normal:"0"; Suspend"1")
6	GPON7	O	Card insert LED; (Card inserted:"0";
7	RPU	I	Connected with an 1.5k pull up resistor to 3.3 VDD
8	AVDD	I	Analog Power 3.3V
9	DP	I/O	USB DP
10	DM	I/O	USB DM
11	AVSS	PWR	Analog Ground
12	RREF	I	Connected an 1k resistor to GND for impedance match
13	NC		
14	NC		
15	NC		
16	NC		
17	NC		
18	PVDD	I	OSC Power 3.3V
19	X_IN	I	12 MHz crystal input.
20	X_OUT	O	12 MHz crystal output.
21	PVSS	PWR	OSC Ground
22	VDD25V	O	Core Power 2.5V
23	VDDH	I	IO Power 3.3V
24	VSSH	PWR	IO Ground
25	VDD33	I	Switch Power 3.3V
26	NC		
27	NC		
28	NC		
29	XD_V33	O	XD Card Power
30	EEPCLK	O	
31	EEPDATA	I/O	
32	NC		
33	NC		
34	NC		
35	NC		
36	SMDATA7	I/O	
37	SMDATA6	I/O	
38	SMDATA5	I/O	
39	SMDATA4	I/O	
40	SMDATA3	I/O	
41	SMDATA2	I/O	
42	SMDATA1	I/O	
43	SMDATA0	I/O	
44	VDD	I	Core power 2.5V

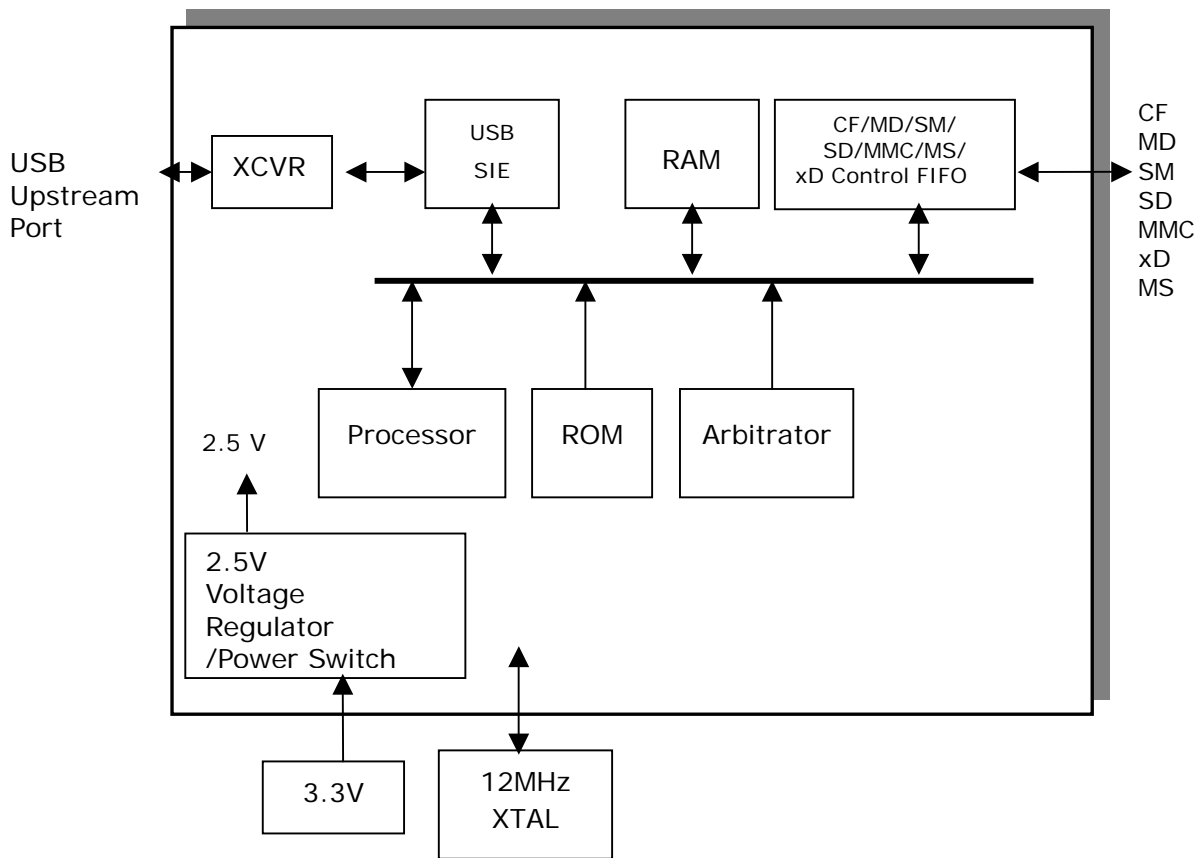


45	GND	PWR	Core Ground
46	XDWPN	O	
47	XDCDN	I	
48	XDCEN	O	
49	SMWPN	I	
50	SMCEN	O	
51	SMCDN	I	
52	SMRBN	I	External pull up with 470K to 3.3V.
53	SMWRN	O	
54	SMRDN	O	
55	SMALE	O	
56	SMCLE	O	
57	RSTN	I	Chip Reset (Reset:"0"; Normal:"1"), pull up with RC
58	NC		
59	NC		
60	GPI2	I	USB current value : 100mA(1)/250mA(0) for USBIF qualification (Pull-High)
61	NC		
62	GPI0	I	Always pull high
63	NC		
64	NC		

4.0 System Architecture and Reference Design

4.1 AU6369 Block Diagram

Figure 4.1 AU6369 Block Diagram





5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power Supply	-0.3 to V _{CC} +0.3	V
V _{IN}	Input Voltage	-0.3 to 3.6	V
V _{OUT}	Output Voltage	-0.3 to V _{CC} +0.3	V
T _{STG}	Storage Temperature	-40 to 150	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	3.0	3.3	3.6	V
V _{DD}	Digital Supply	2.25	2.5	2.75	V
V _{IN}	Input Voltage	0	3.3	5.2	V
T _{OPR}	Operating Temperature	0	25	125	°C

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IN}	Input current	no pull-up or pull-down	-10	±1	10	μA
I _{OZ}	Tri-state leakage current		-10	±1	10	μA
C _{IN}	Input capacitance	Pad Limit		2.8		ρF
C _{OUT}	Output capacitance	Pad Limit		2.8		ρF
C _{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V _{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V _{il}	Input low voltage	LVTTTL			0.8	V
V _{ih}	Input high voltage		2.0			V
V _{ol}	Output low voltage	I _{ol} = 2~16mA			0.4	V
V _{oh}	Output high voltage	I _{oh} = 2~16mA	2.4			V
R _{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R _{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I _{in}	Input leakage current	V _{in} = V _{CC} or 0	-10	±1	10	μA
I _{oz}	Tri-state output leakage current		-10	±1	10	μA



5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply voltage		3.0	3.3	3.6	V
VCC	Digital supply voltage		2.25	2.5	2.75	V
I _{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
I _{CC(susp)}	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V _{IL}	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage		2.0			V
Output levels						
V _{OL}	Low-level output voltage				0.2	V
V _{OH}	High-level output voltage		VCC-0.2			V



AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V



Input Levels (single-ended receivers)						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V



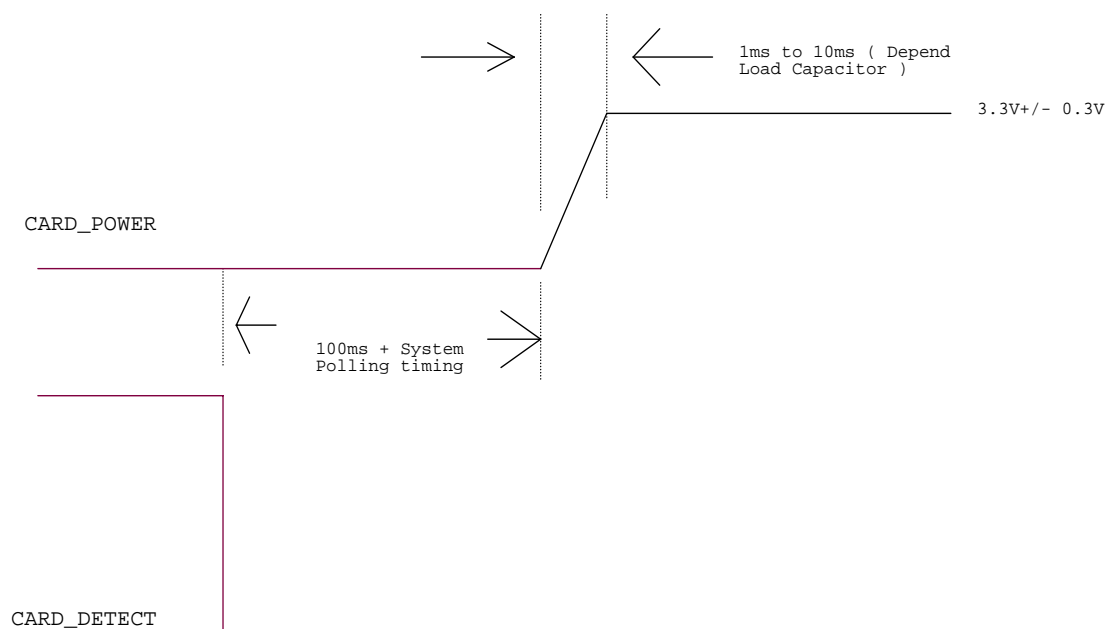
5.6 Power Switch Feature

AU6369 integrates a 3.3V to 2.5V voltage regulator and power switch to replace all MOS chips for flash card power supply.

Card Power Output Current Range

- For MS/SD
 - ◆ MAX: 100mA
- For XD/SMC
 - ◆ MAX: 70mA
- For CF
 - ◆ MAX: 250mA
- Card power output voltage range
 - ◆ MS/XD/SD/SMC/CF: $3.3V \pm 0.3V$
- AU6369 will turn off all of Card Power in suspend mode

Figure 5.1 Card Detect Power-on Timing



6.0 Mechanical Information

Figure 6.1 48 LQFP Mechanical Information Diagram

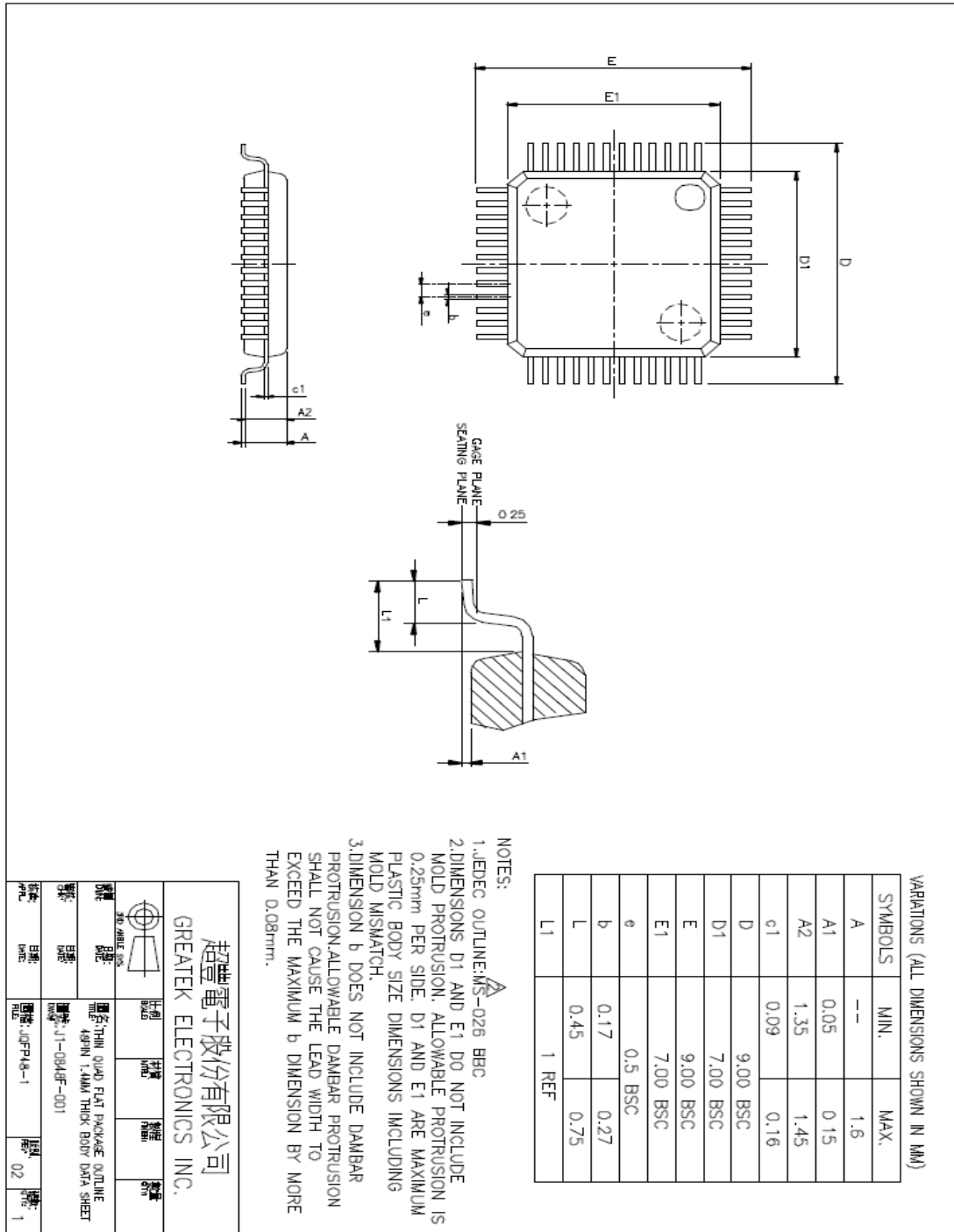
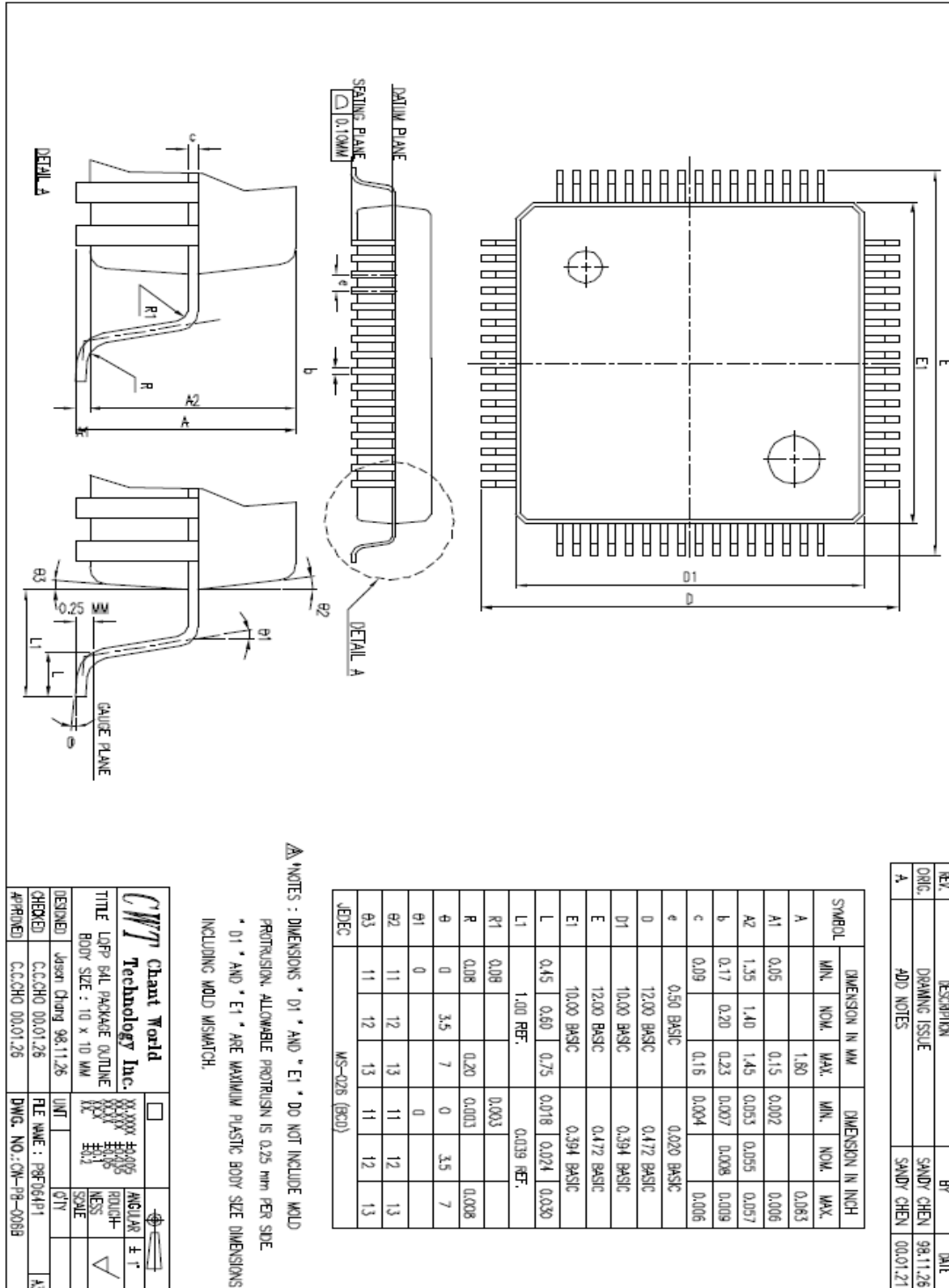


Figure 6.2 64 LQFP Mechanical Information Diagram





7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
CF	Compact Flash
MD	Micro Drive
SMC	SmartMedia Card
MS	Memory Stick
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface



【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.