



# AU6371-JEL

**USB2.0 Single LUN  
Multiple Flash Card Reader Controller**

Technical Reference Manual



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**USB2.0 Single LUN**

**Multiple Flash Card Reader Controller**



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# 1. Introduction

## 1.1 Description

The AU6371 is a highly integrated single chip media USB card reader controller that supports all popular form factor digital cards, such as CF, MD, SMC, SD, MMC, MS, MS Pro, MS Duo and XD. In addition to the small form factor and low BOM cost the solution also implement high performance operation a sophisticated DMA engine.

With the compliance with USB Storage Class V1.0, AU6371 not only exhibits wide acceptance in various OS platforms, its multiple slot design further enables the solution adapters become the content exchange center for mobile media. It can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6371, users can transfer digital data between flash memory card and PC or these electronic devices.

The AU6371 used 48 pin package specifically designed for small foot print application, such as Note book and printer.

In addition to its high performance and outstanding compatibility, the solution of AU6371 comes with a user-friendly utility to enhance users' experience. Moreover, AU6371 integrates power switch to reduce the overall BOM cost.

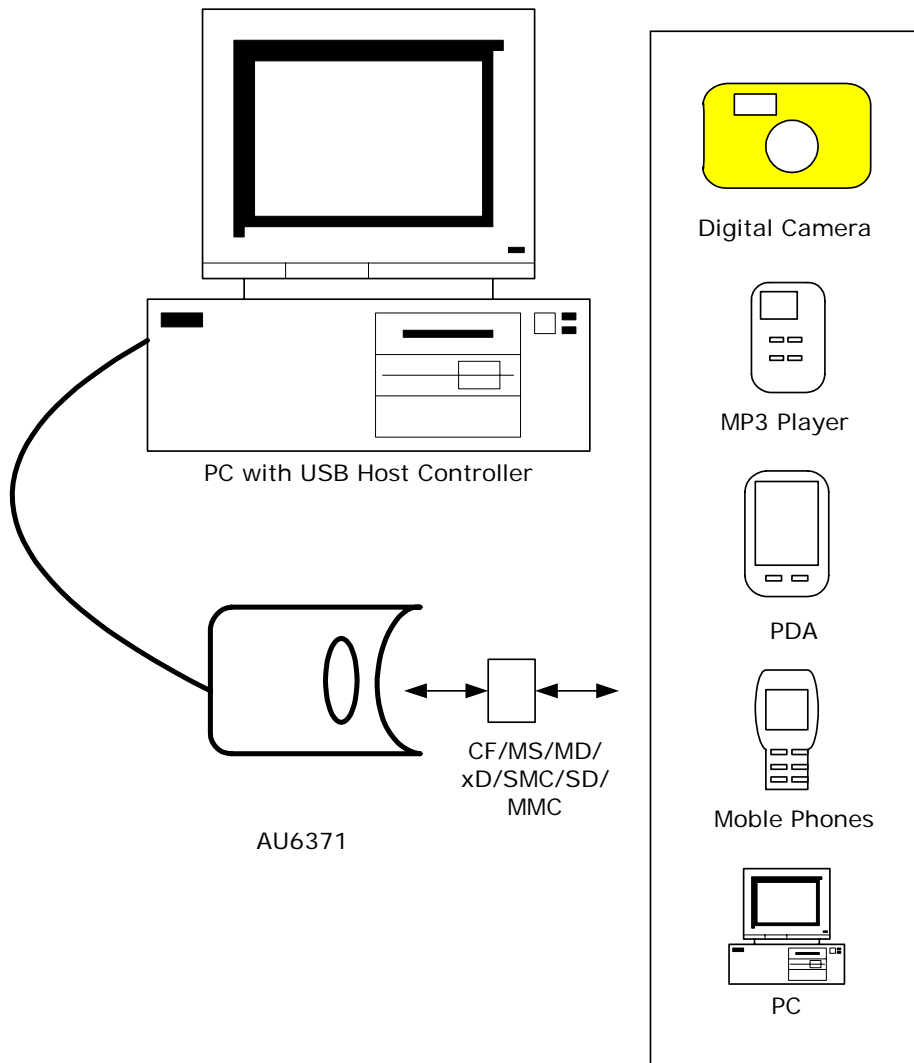
## 1.2 Features

- Supports USB 2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Supports CF/MD/SD/MMC/MS/MS\_Pro/MS\_Duo/xD/SMC compatible flash card in 48 pin package
- Supports the latest flash card specification: CF 4.0 (with True IDE PIO mode 6), SD 2.0 (SDHC), MMC 4.2 (8-bit), MS Pro parallel mode (4-bit), xD 1.2, SMC2003.
- A built-in DMA engine for data transmission performance enhancement
- Work with default driver from Windows ME/2000/XP and Mac OS X; Vendor device driver from Alcor Micro are available to run under Windows 98/2000(SP1/SP2) and Mac OS 9
- Ping-pong FIFO implementation for concurrent bus operation
- Supports multiple sector burst transfer for optimized performance
- Supports Dynamic Icon Utility to enhance user experience
- Supports LED for bus activities indication
- Power switch integrated to reduce production BOM cost
- Support power saving mode for notebook when no card inserted.

## 2. Application Block Diagram

The following application drawing demonstrates a typical card reader block diagram using AU6371. By connecting one card reader to a desktop or notebook PC through USB bus, the AU6371 becomes a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Block Diagram







### 3. Pin Assignment

The AU6371 is delivered in 48pin LQFP form factor. Documented below is a figure shows signal names of each pin and a table in the following page describes each pin in more details.

Figure 3.1 Pin Assignment Diagram

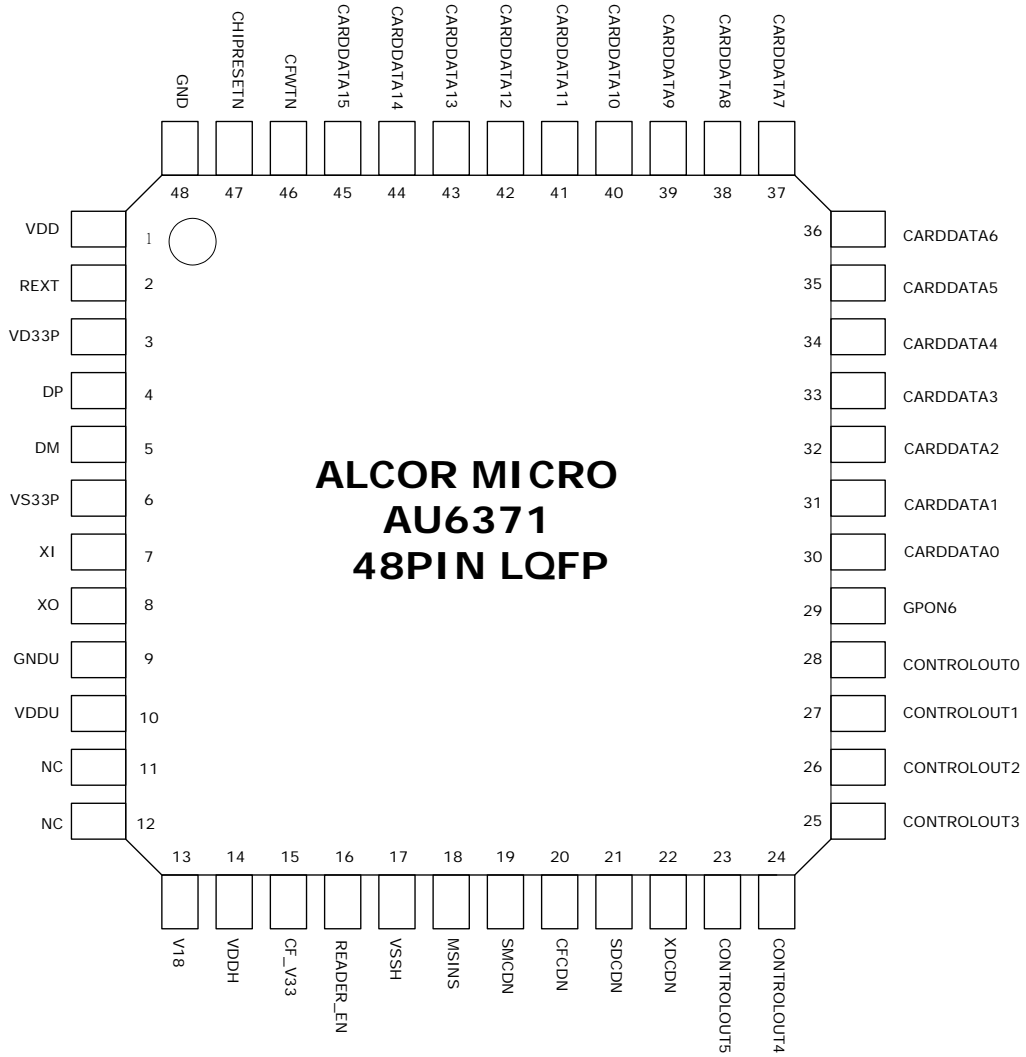




Table 3.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	VDD	I	Core Power 1.8V
2	REXT	O	External Resistor to Ground
3	VD33P		3.3V Power
4	DP	I/O	USB DP
5	DM	I/O	USB DM
6	VS33P		Ground Power
7	XI	I	12 MHz crystal input.
8	XO	O	12 MHz crystal output.
9	GNDU		UTMI Gound
10	VDDU		UTMI Power 1.8 V
11	NC		
12	NC		
13	V18	O	Core Power 1.8V
14	VDDH	I	3.3V for IO pad
15	CF_V33	O	Card Power 3.3V
16	READER_EN	I	Reader function enable("1" : Card reader function enable; "0" : Card only mode)
17	VSSH	IO	Power Ground
18	MSINS	I	MS Card detect
19	SMCDN	I	SMC Card detect
20	CFCDN	I	CF Card detect
21	SDCDN	I	SD Card detect
22	XDCDN	I	XD Card detect
23	CONTROLOUT5	O	CFRESETN and SMWRN/XDWRN
24	CONTROLOUT4	O	CFWRN and SMRDN/XDRDN
25	CONTROLOUT3	O	CFRDN and XDCEN/SMCEN
26	CONTROLOUT2	O	CFAD2 and SMALE/XDALE
27	CONTROLOUT1	O	CFAD1, MSCLK and SMCLE/XDCLE
28	CONTROLOUT0	O	CFAD0, SDCLK and MSBS
29	GPON6	O	LED indicator for card operation

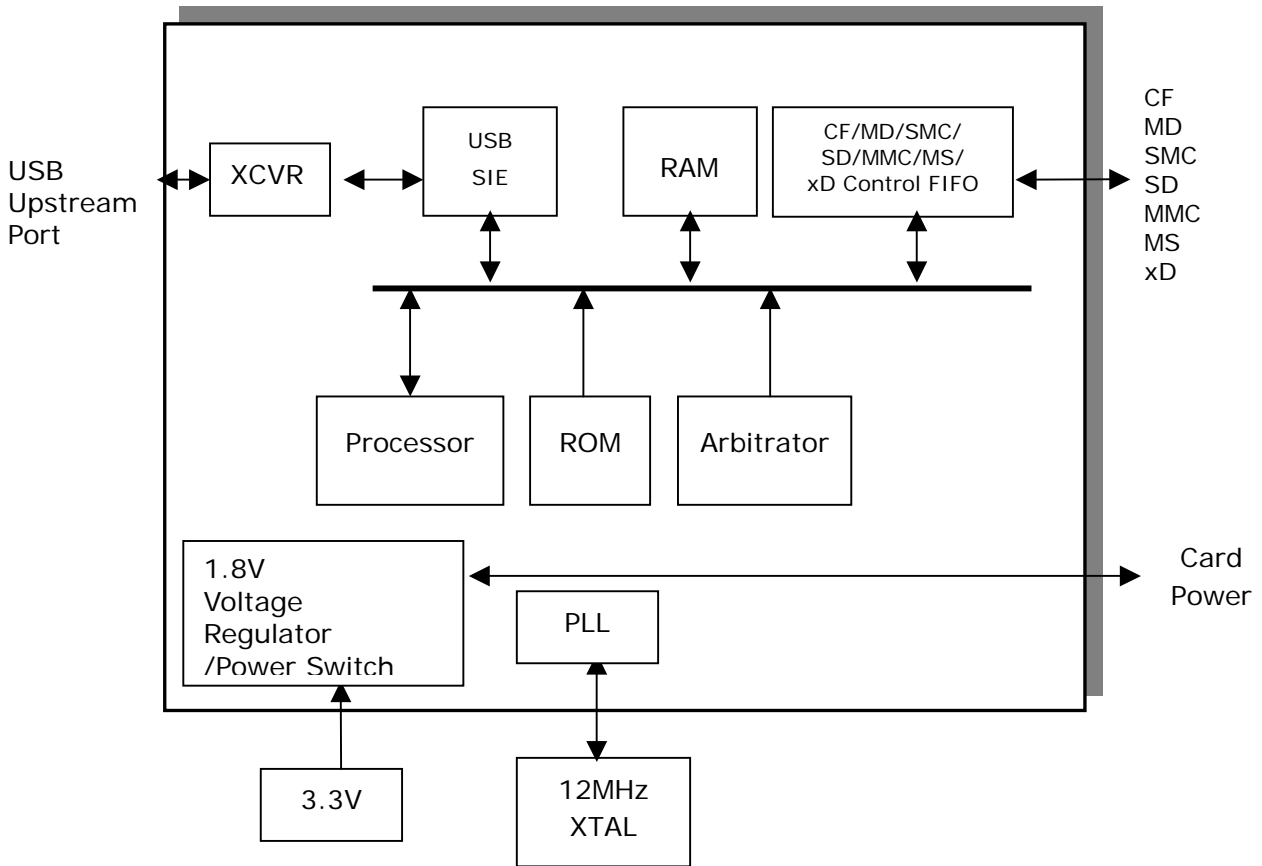


Pin #	Pin Name	I/O	Description
30	CARDDATA0	I/O	CFDATA0, MSDATA0, and SDCMD
31	CARDDATA1	I/O	CFDATA1, MSDATA1, XDWPN, and SMWPN
32	CARDDATA2	I/O	CFDATA2, MSDATA2, and SDWP
33	CARDDATA3	I/O	CFDATA3, MSDATA3, SMRBN, and XDRBN
34	CARDDATA4	I/O	CFDATA4 and SDDATA0
35	CARDDATA5	I/O	CFDATA5 and SDDATA1
36	CARDDATA6	I/O	CFDATA6 and SDDATA2
37	CARDDATA7	I/O	CFDATA7 and SDDATA3
38	CARDDATA8	I/O	CFDATA8, XDDATA0, and SDDATA4
39	CARDDATA9	I/O	CFDATA9, XDDATA1, and SDDATA5
40	CARDDATA10	I/O	CFDATA10, XDDATA2, and SDDATA6
41	CARDDATA11	I/O	CFDATA11, XDDATA3, and SDDATA7
42	CARDDATA12	I/O	CFDATA12 and XDDATA4
43	CARDDATA13	I/O	CFDATA13 and XDDATA5
44	CARDDATA14	I/O	CFDATA14 and XDDATA6
45	CARDDATA15	I/O	CFDATA15 & XDDATA7
46	CFWTN	I	CF WAITN
47	CHIPRESETN	I	Chip Reset (low active to reset the whole chip), must be pull up with RC.
48	GND	I	Core Power Gound

# 4. System Architecture and Reference Design

## 4.1 AU6371 Block Diagram

Figure 4.1 AU6371 Block Diagram





## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
$V_{DDH}$	Power Supply	-0.3 to 3.6	V
$V_{IN}$	Input Signal Voltage	-0.3 to $V_{DDH} + 0.3$	V
$T_{STG}$	Storage Temperature	-40 to 150	°C

### 5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$V_{DDH}$	Power Supply	3.0	3.3	3.6	V
$V_{DD}$ $V_{18}$	Digital Supply	1.62	1.8	1.98	V
$V_{IN}$	Input Signal Voltage	-0.3		$V_{DDH} + 0.3$	V
$T_{OPR}$	Operating Temperature	0		85	°C

### 5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{IN}$	Input current	No pull-up or pull-down	-10	±1	10	μA
$I_{OZ}$	Tri-state leakage current		-10	±1	10	μA
$C_{IN}$	Input capacitance	Pad Limit		2.8		ρF
$C_{OUT}$	Output capacitance	Pad Limit		2.8		ρF
$C_{BID}$	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

### 5.4 DC Electrical Characteristics of 3.3V I/O Cells

**Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells**

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
$V_{DDH}$	Power supply	3.3V I/O	3.0	3.3	3.6	V
$V_{il}$	Input low voltage	LVTTL			0.8	V
$V_{ih}$	Input high voltage		2.0			V
$V_{ol}$	Output low voltage	$ I_{ol}  = 2\sim 16\text{mA}$			0.4	V
$V_{oh}$	Output high voltage	$ I_{oh}  = 2\sim 16\text{mA}$	2.4			V
$R_{pu}$	Input pull-up resistance	PU=high, PD=low	55	75	110	$K\Omega$
$R_{pd}$	Input pull-down resistance	PU=low, PD=high	40	75	150	$K\Omega$
$I_{in}$	Input leakage current	$V_{in} = V_{DDH}$ or 0	-10	$\pm 1$	10	$\mu A$
$I_{oz}$	Tri-state output leakage current		-10	$\pm 1$	10	$\mu A$

## 5.5 USB Transceiver Characteristics

**Table 5.5 Electrical characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VD33	Analog supply Voltage		3.0	3.3	3.6	V
VDDU VDDA	Digital supply Voltage		1.62	1.8	1.98	V
$I_{cc}$	Operating supply current	High speed operating at 480 MHz			55	mA

**Table 5.6 Static characteristic : Digital pin**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V <sub>IL</sub>	Low-level input voltage				0.8	V
V <sub>IH</sub>	High-level input voltage		2.0			V
Output levels						
V <sub>OL</sub>	Low-level output voltage				0.2	V
V <sub>OH</sub>	High-level output voltage		VDDH-0.2			V

**Table 5.7 Static characteristic : Analog I/O pins (DP/DM)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels ( differential receiver )						
V <sub>HSDIFF</sub>	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V <sub>HSCM</sub>	High speed data signaling common mode voltage range		-50		500	mV
V <sub>HSSQ</sub>	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V <sub>HSDSC</sub>	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V <sub>HSOI</sub>	High speed idle level output voltage(differential)		-10		10	mV
V <sub>HSOL</sub>	High speed low level output voltage(differential)		-10		10	mV
V <sub>HSOH</sub>	High speed high level output voltage(differential)		-360		400	mV
V <sub>CHIRPJ</sub>	Chirp-J output voltage ( differential )		700		1100	mV
V <sub>CHIRPK</sub>	Chirp-K output voltage ( differential )		-900		-500	mV
Resistance						
R <sub>DRV</sub>	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω

		Overall resistance including external resistor	40.5	45	49.5	
Termination						
$V_{TERM}$	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS)						
Input Levels (differential receiver)						
$V_{DI}$	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
$V_{CM}$	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						
$V_{SE}$	Single ended receiver threshold		0.8		2.0	V
Output levels						
$V_{OL}$	Low-level output voltage		0		0.3	V
$V_{OH}$	High-level output voltage		2.8		3.6	V

**Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
$t_{HSR}$	High-speed differential rise time		500			ps
$t_{HSF}$	High-speed differential fall time		500			ps
Full-Speed Mode						
$t_{FR}$	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FF}$	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FRMA}$	Differential rise/fall time matching ( $t_{FR} / t_{FF}$ )	Excluding the first transition from idle mode	90		110	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V



### 5.6 Power Switch Feature

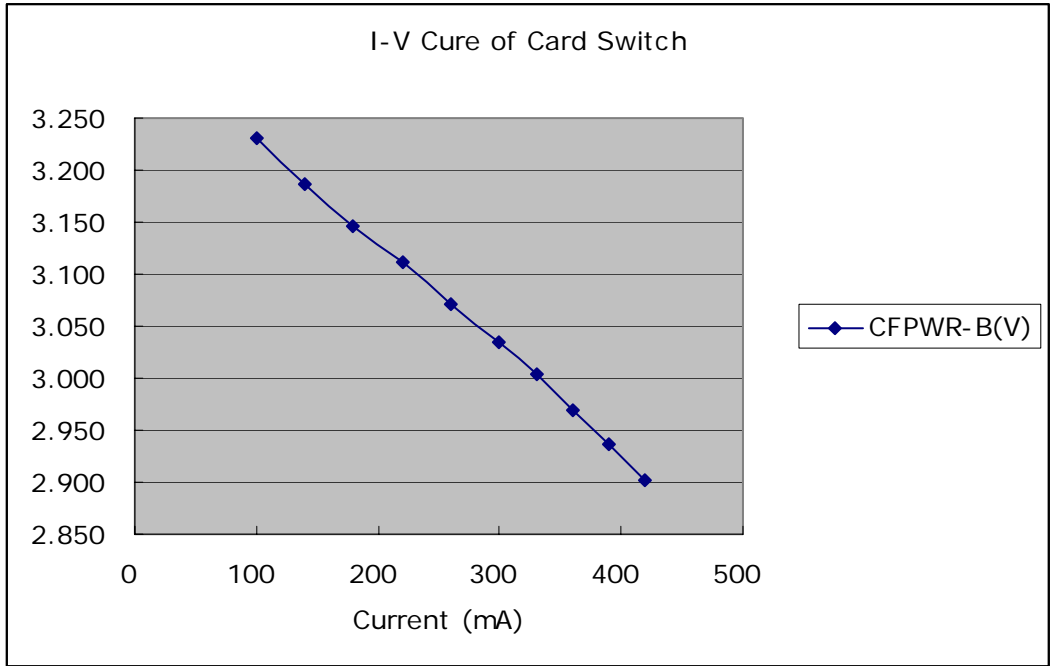


Figure 5.1 Built-in card power switch I-V curve

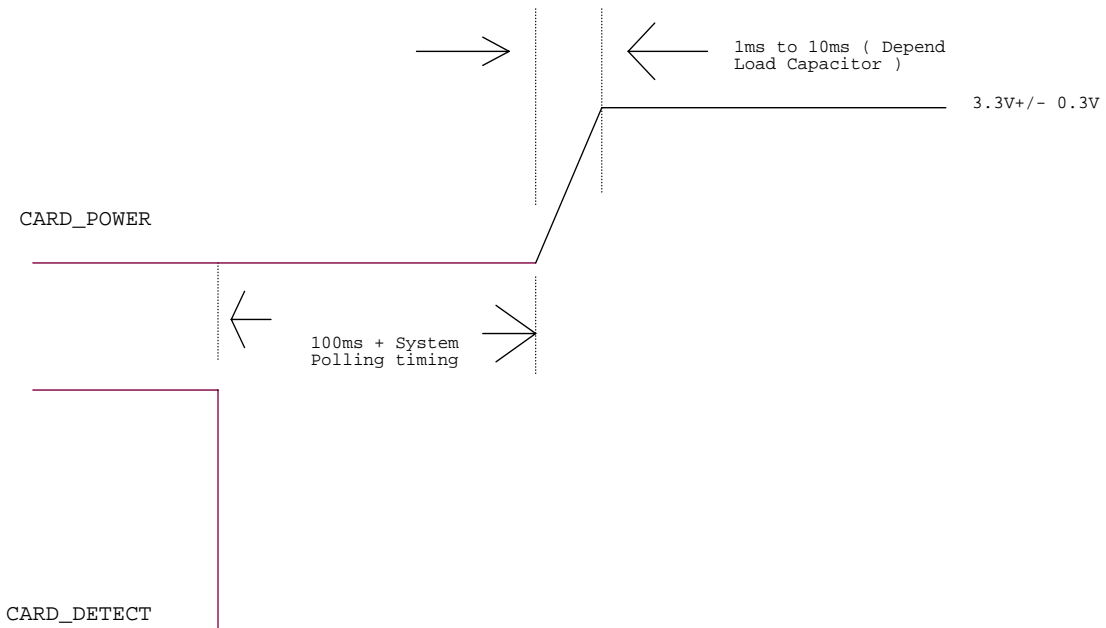
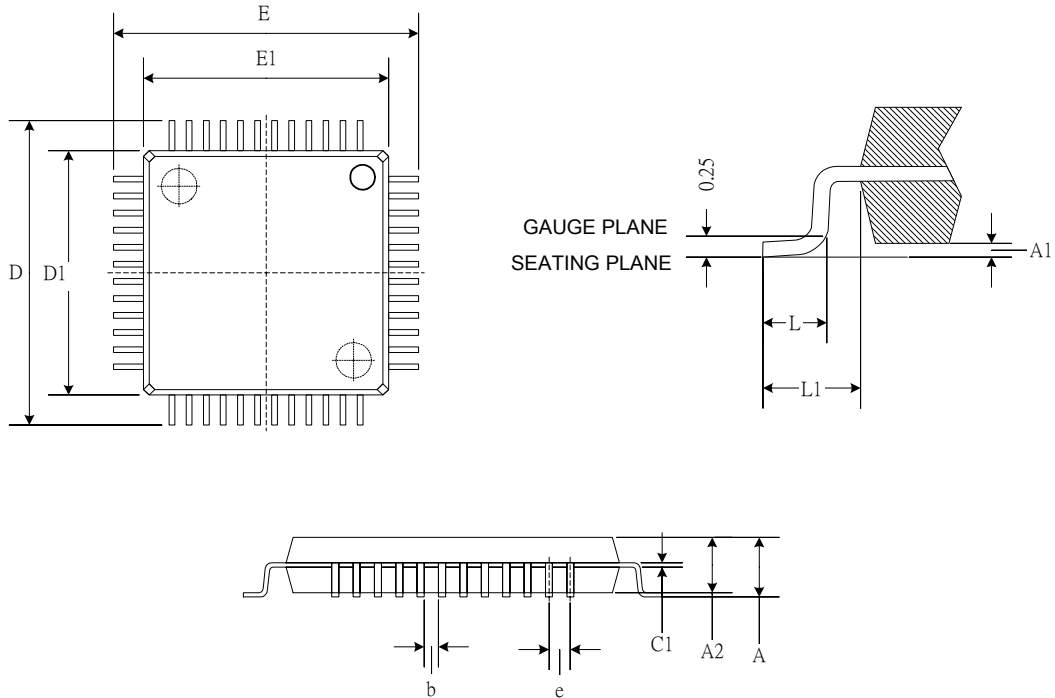


Figure 5.2 Card Detect Power-on Timing

## 6. Mechanical Information

Figure 6.1 Mechanical Information Diagram



SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm



## 7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

<b>SIE</b>	Serial Interface Engine
<b>CF</b>	Compact Flash
<b>MD</b>	Micro Drive
<b>SMC</b>	SmartMedia Card
<b>MS</b>	Memory Stick
<b>SD</b>	Secure Digital
<b>MMC</b>	Multimedia Card
<b>UTMI</b>	USB Transceiver Macrocell Interface

## About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.