



Data Book

AU6390

**USB2.0 to ATA/ATAPI Bridge
Controller**

Technical Reference Manual

Product Specification

Preliminary Release

Revision 0.9W

Confidential

Aug 2005



Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
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1.0 Introduction

1.1 Description

AU6390 is a single chip for USB2.0 high-speed transmission controller, which is designed as a bridge between USB host and ATA/ATAPI storage device, such as hard disk, CD-ROM, CD-R/W, DVD-ROM, DVD-R/W, etc. With AU6390, users can transfer huge digital data between ATA/ATAPI storage device and PC or other electronic devices. Furthermore, AU6390 can perform speed negotiation in PIO mode 0~4 and Ultra DMA mode 2/4 with the down-streaming storage device to achieve the best performance and compatible capability.

1.2 Features

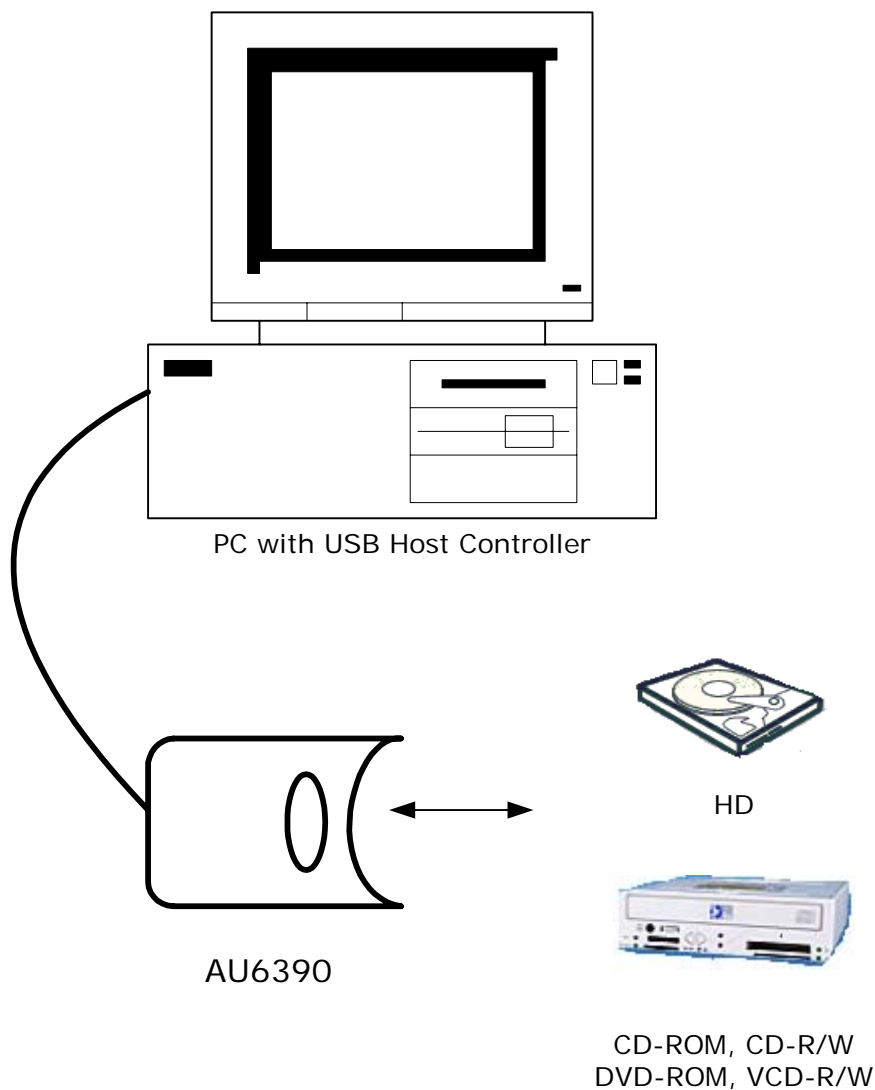
- Support USB V2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Support ATA/ATAPI-6 specification Revision 1.0
 - PIO mode 0~4
 - UDMA mode 2/4
- Support for a single ATA/ATAPI device configured either as master or slave device
- Support 48-bit addressing for LBA hard drives
- Support partition segment for a single ATA/ATAPI device
- Alcor DMA engine integrated for performance enhancement
- Work with default driver from Windows ME/2000/XP and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- LEDs for USB awake/suspend and data transferring
- 3.3V operation self-powered device
- 48pin LQFP package



2.0 Application Block Diagram

Following is the application diagram of a typical removable USB2.0 ATA/ATAPI product. Users can exchange the digital content between ATA/ATAPI device and PC (Notebook).

2.1 Block Diagram





3.0 Pin Assignment

The AU6390 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 3.1 Pin Assignment Diagram

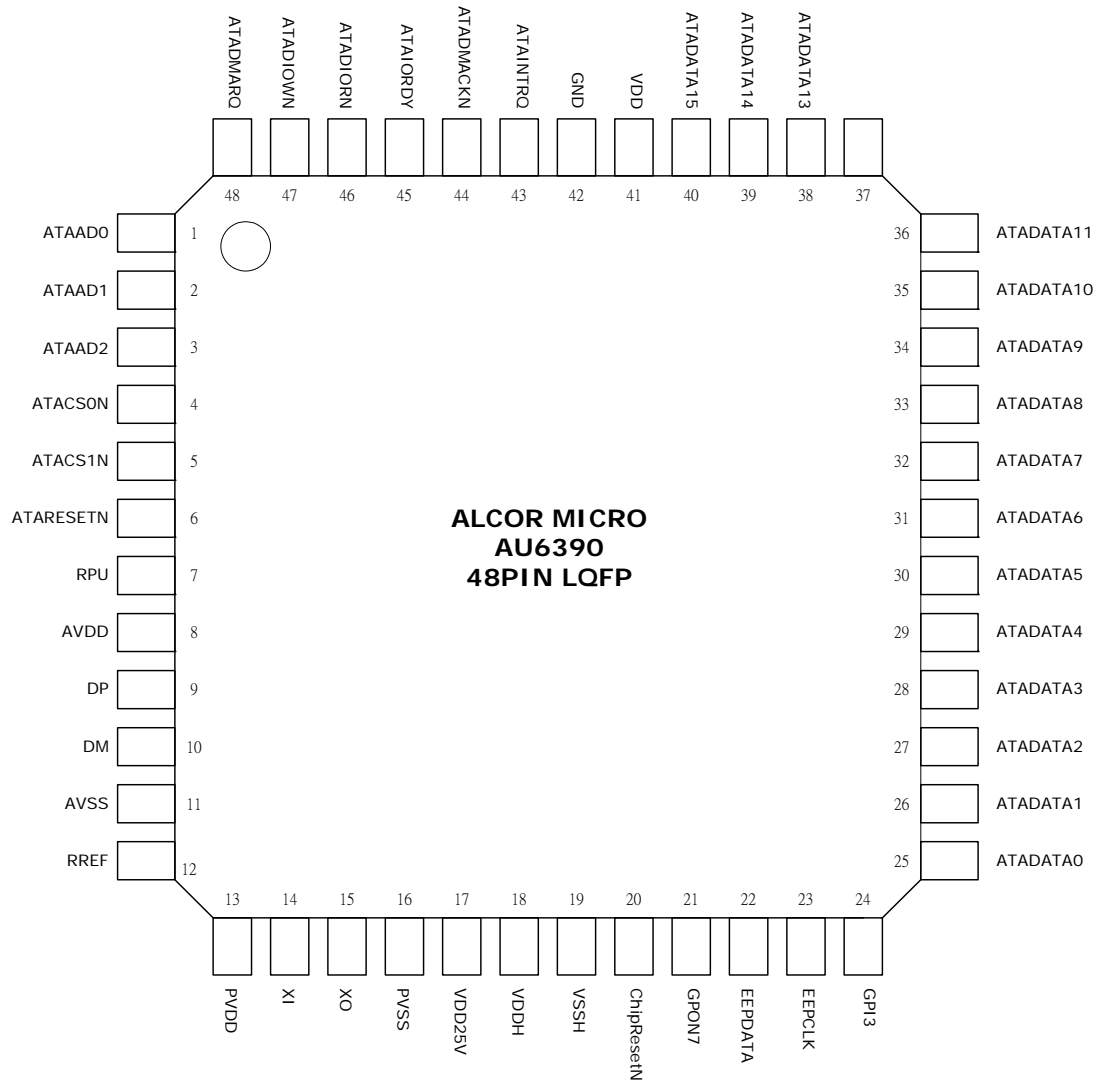




Table 3.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	ATAAD0	O	ATA Address select 0
2	ATAAD1	O	ATA Address select 1
3	ATAAD2	O	ATA Address select 2
4	ATACSON	O	ATA Chip Select 0
5	ATACS1N	O	ATA Chip Select 1
6	ATARESETN	O	ATA Reset
7	RPU	I	Connected with an 1.5k pull up resistor to AVDD
8	AVDD	I	Analog power 3.3V
9	DP	I/O	USB DP
10	DM	I/O	USB DM
11	AVSS	PWR	Analog ground
12	RREF	I	Connected an 1k resistor to A GND for impedance match
13	PVDD	I	OSC power 3.3V
14	XI	I	12 MHz crystal input.
15	XO	O	12 MHz crystal output.
16	PVSS	PWR	OSC ground
17	VDD25V	O	2.5V output connect to core power
18	VDDH	I	3.3V for IO pad
19	VSSH	PWR	IO ground 3.3V
20	ChipResetN	I	Chip Reset, must be pull up with RC.
21	GPON7	O	Device LED
22	EEPDATA	I/O	EEPData
23	EEPCLK	I/O	EEPCLK
24	GPI3	I	General Purpose Input.

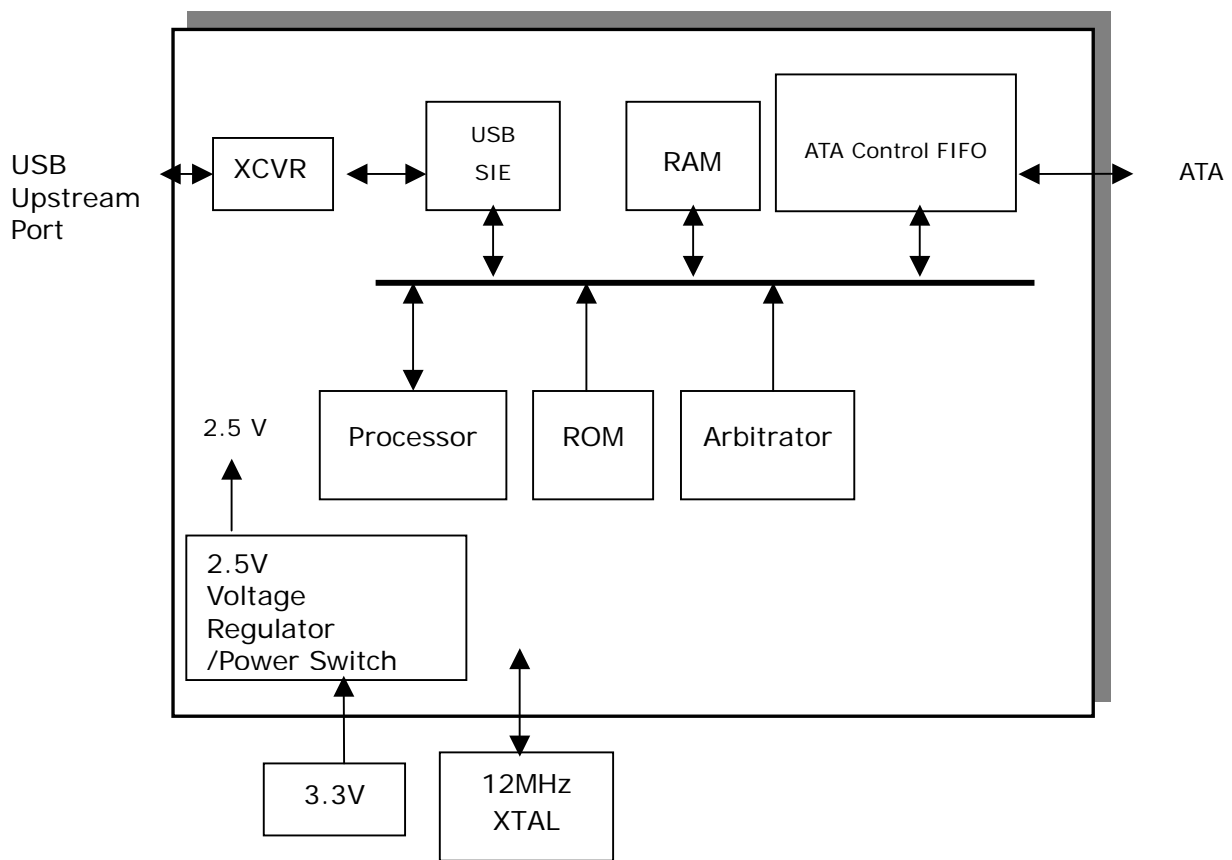


Pin #	Pin Name	I/O	Description
25	ATADATA0	I/O	ATA Data Bus
26	ATADATA1	I/O	ATA Data Bus
27	ATADATA2	I/O	ATA Data Bus
28	ATADATA3	I/O	ATA Data Bus
29	ATADATA4	I/O	ATA Data Bus
30	ATADATA5	I/O	ATA Data Bus
31	ATADATA6	I/O	ATA Data Bus
32	ATADATA7	I/O	ATA Data Bus
33	ATADATA8	I/O	ATA Data Bus
34	ATADATA9	I/O	ATA Data Bus
35	ATADATA10	I/O	ATA Data Bus
36	ATADATA11	I/O	ATA Data Bus
37	ATADATA12	I/O	ATA Data Bus
38	ATADATA13	I/O	ATA Data Bus
39	ATADATA14	I/O	ATA Data Bus
40	ATADATA15	I/O	ATA Data Bus
41	VDD	PWR	Core power 2.5V
42	GND	PWR	Core ground
43	ATAINTRQ	I	ATA Interrupt request
44	ATADMACKN	O	ATA Control Signal DMACKN
45	ATAIORDY	I	ATA Control Signal IORDY
46	ATADIORN	O	ATA Control Signal DIORN
47	ATADIOWN	O	ATA Control Signal DIOWN
48	ATADMARQ	I	ATA Control Signal DMARQ

4.0 System Architecture and Reference Design

4.1 AU6390 Block Diagram

Figure 4.1 AU6390 Block Diagram





5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power Supply	-0.3 to V _{CC} +0.3	V
V _{IN}	Input Voltage	-0.3 to 3.6	V
V _{OUT}	Output Voltage	-0.3 to V _{CC} +0.3	V
T _{STG}	Storage Temperature	-40 to 150	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	3.0	3.3	3.6	V
V _{DD}	Digital Supply	2.25	2.5	2.75	V
V _{IN}	Input Voltage	0	3.3	5.2	V
T _{OPR}	Operating Temperature	0	25	125	°C

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IN}	Input current	no pull-up or pull-down	-10	±1	10	μA
I _{OZ}	Tri-state leakage current		-10	±1	10	μA
C _{IN}	Input capacitance	Pad Limit		2.8		ρF
C _{OUT}	Output capacitance	Pad Limit		2.8		ρF
C _{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$ I_{ol} = 2 \sim 16\text{mA}$			0.4	V
V_{oh}	Output high voltage	$ I_{oh} = 2 \sim 16\text{mA}$	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	$K\Omega$
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	$K\Omega$
I_{in}	Input leakage current	$V_{in} = V_{CC}$ or 0	-10	± 1	10	μA
I_{oz}	Tri-state output leakage current		-10	± 1	10	μA



5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply voltage		3.0	3.3	3.6	V
VCC	Digital supply voltage		2.25	2.5	2.75	V
I _{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
I _{CC(susp)}	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V _{IL}	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage		2.0			V
Output levels						
V _{OL}	Low-level output voltage				0.2	V
V _{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C ~ 115°C



Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						



V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

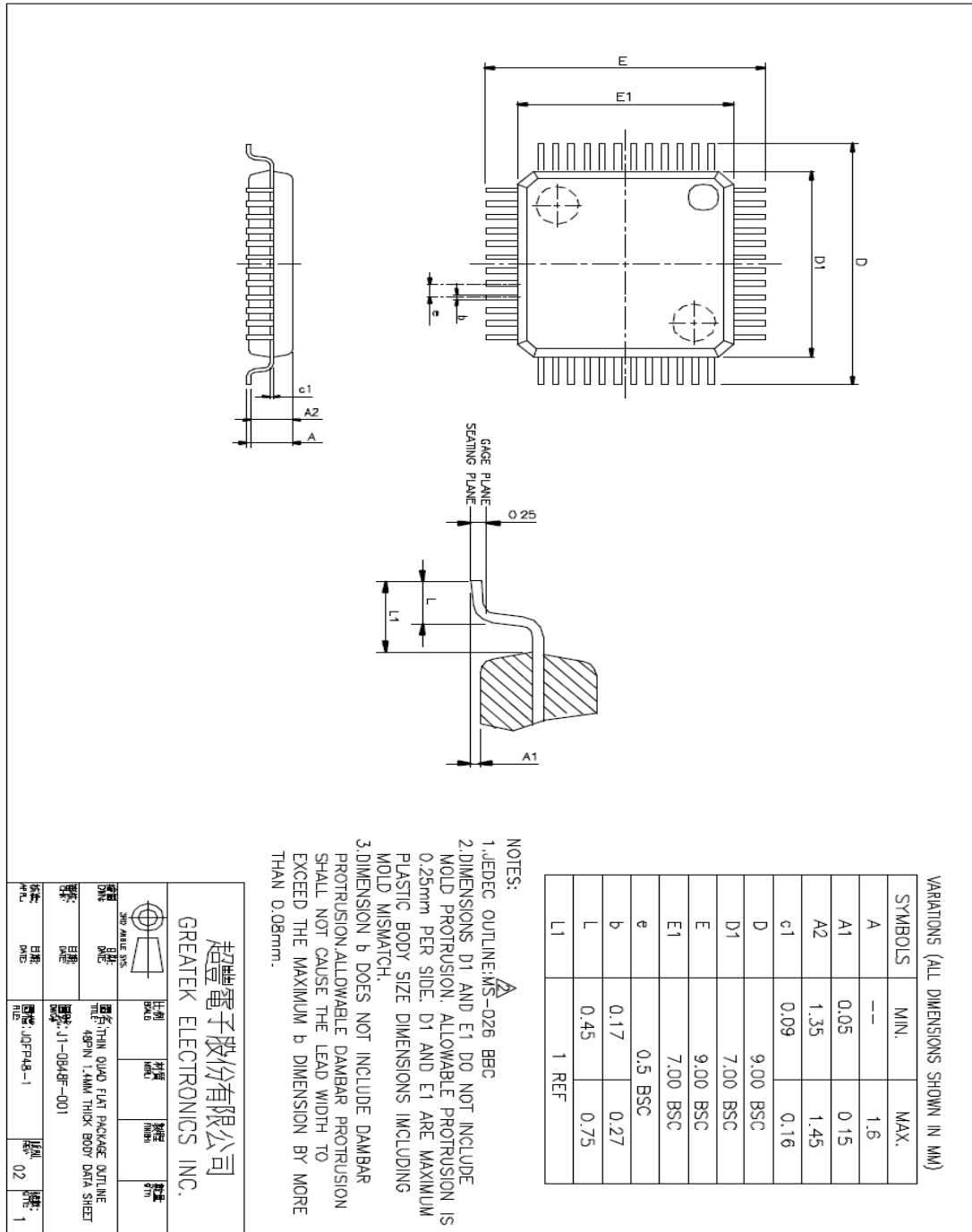
AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram





7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
ATA	Advanced Technology Attachment
UTMI	USB Transceiver Macrocell Interface



【MEMO】

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